Publication Number 29-266F01R07

MODEL 70
MAINTENANCE MANUAL

CONSISTS OF:

GENERAL DESCRIPTION		
	Model 70 General Description	29-266R01A12
	Chassis and Power Supply Expansion Information Specification	11-115R02A12
PROCESSOR		
	Model 70 Maintenance Specification	01-051F01R01A21
MEMORY		
	8KB (Series 5) Memory Maintenance Specification	02-211R02A21
SELECTOR CHANNEL		
	Selector Channel Installation Specification	02-232M01R03A20
	Selector Channel Maintenance Specification	02-232M01R01A21
MEMORY PROTECT		
	Memory Protect Installation Specification	02-236R02A20
	Memory Protect Maintenance Specification	02-236A21
	Memory Protect Programming Specification	02-236A22
DRAWINGS		
	Processor Schematic	01-051M01R16D08
	Series 5 Memory Schematic	02-211R07D08
	Selector Channel Schematic	02-232M01R03D08
	Memory Protect Schematic	02-236R04D08
	Display Panel Schematic	09-051R09D08
	Power Supply Schematic	34-012R03D08
	Power Supply Schematic	34-012M01D08
	Power Supply Schematic	34-017R06D08
	Power Supply Schematic	34-020R03D08
	Cable Information	01-051R04C12
	Selector Channel Component Locator	35-391M02R03E03
	15" Chassis Schematic - Field 1	17-166B08
	15" Chassis Schematic - Field 0	17-214B08

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August 1974

MOD 70 BOARD INTERCHANGEABILITY

		I/O		ROM		ALU*	MCTL*
	EC =	35-390R08 25-280	-M01R03 25-280R02	35-388R07 25-278R03	-M01R03 25-278R03	35-389R07 25-279R02	35-387R08 25-277R02
A	37						R09
	38	R09	R04				
	42	R10	R05				
	47						R10
	49	R11	R06				
	50						R11
	51	R12	R07				
B	52 NOTE 1	R13	R08	R08	R04		
	58					R08	R12
	59						R13
	62						
	64	R14	R09				
	69	R15	R10				
	72						R14
	82				R05		
	103			R09	R05		
C	85 NOTE 2		R11		R06	R09	R15
	104	R16	R11	R10	R06		
	105			R11	R07		
	106			R12	R08		
	107						R16
	108 NOTE 3			R13	R09		
	109			R14	R10		

NOTES: 1. I/O and ROM changes must be coordinated.
2. I/O and ROM changes must be coordinated
3. This change requires back panel modification.
See ECN 1478: raises back panel 11-115F01 to R04.

*ALU and MCTL interchangeable on all rev. levels.

QUICK REFERENCE INDEX

To aid in quickly locating a particular section, the index marks on the edge of this page are aligned with similar marks on the first page of each section.

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MODEL 70
GENERAL DESCRIPTION

1. INTRODUCTION

The Model 70 combines advanced circuitry and packaging designs to give the user a price/performance optimized machine. The Model 70 is completely upward compatible with INTERDATA Model 3, 4 and 5 Processors user instructions, interrupt handling, input/output formats and control sequencing. Because of this compatability, the Model 70 can use the wide range of existing software and peripheral devices.

The Model 70 offers a comprehensive set of 113 instructions making the system both easy to program and efficient to operate. Through multi-function instructions and direct core addressing, coding and debugging time is reduced to a minimum.

Memory is addressable to the eight-bit byte level. Memory is expandable from the basic 8,192 bytes to 65,536 bytes. All memory is directly addressable with the primary instructions, no paging or indirect addressing is required. Sixteen 16-bit General Registers can be used as Accumulators, fifteen of which can also be used as Index Registers. Register-to-Register instructions permit operations between any of the sixteen General Registers, eliminating redundant loads and stores.

The Protect Mode of the Model 70 enables Memory Protect and detection of Privileged instructions, and can be activated under program control. This mode is invaluable in process control, data communication, and time-sharing operations to guarantee that a running program cannot interfere with the integrity of the system.

The Model 70 also provides a flexable Input/Output system in addition to conventional means of programmed I/O. In the Automatic I/O Service Mode, the Processor acknowledges all I/O interrupts and automatically performs much of the overhead prior to activating the Interrupt Service Routine. In conjunction with the Automatic I/O Service, an I/O Channel can perform data transfers and signal counting without interrupting the running program until the specified sequence is completed.

Up to four Direct Memory Access Channels can be added to a Model 70 Memory System. These channels operate over the common Memory Bus, on a cycle stealing basis, through a Direct Memory Access Port which is build into the Processor. Two types of Direct Memory Access Channels can be used with the Model 70 System: The Selector Channel, which permits direct data transfer between any standard oriented INTERDATA device controller and memory; and the Direct Memory Access Channel custom designed by the user for special applications.

2. SCOPE

This specification is intended to enable the digital technician to understand the INTERDATA documentation system. Number Notation, the Part Numbering System, and the Drawing System are described. Illustrations are provided to help understand these systems. Other publications which may be of interest to Model 70 users are shown in Table 1.

TABLE 1. RELATED PUBLICATIONS

Title	Publication Number
Universal Clock Instruction Manual	29-265
Users Handbook	29-261
Model 70 Maintenance Manual	29-266*
Multiplexor Bus Buffer Instruction Manual	29-267
8 Line Interrupt Module Instruction Manual	29-268

*This General Description is a part of 29-266

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3. BLOCK DIAGRAM

A Model 70 simplified block diagram is shown in Figure 1. The Model 70 is a 16-bit digital computer. The Processor logic is contained on four PC boards:

Part No.	Description	Card File Position
35-387	Memory Control	4
35-390	I/O Board	5
35-389	ALU Board	6
35-388	ROM Board	7

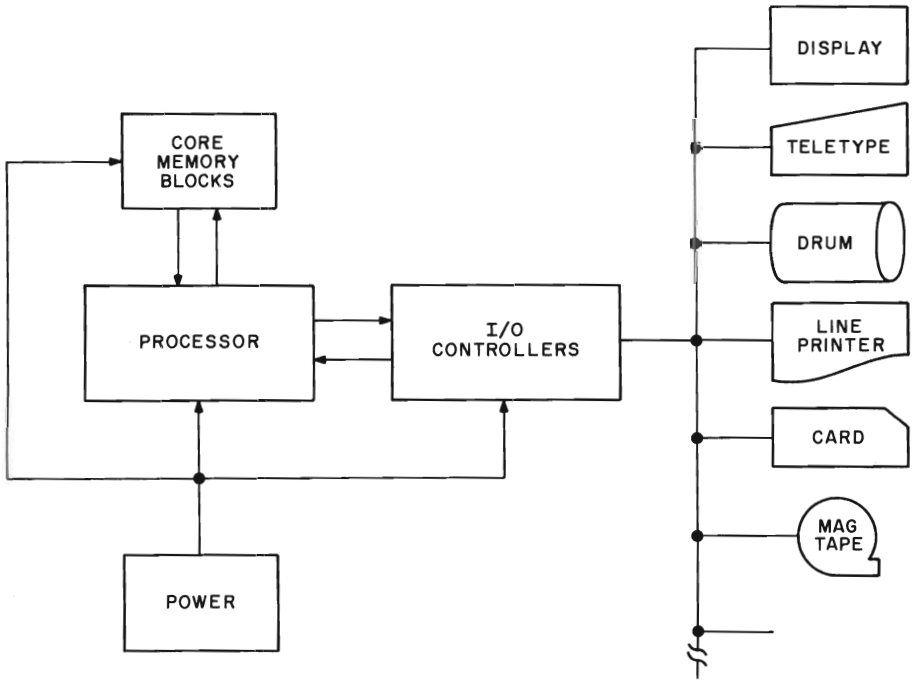


Figure 1. Model 70 Simplified Block Diagram

4. DOCUMENTATION

This section describes the style and conventions used with INTERDATA documentation.

4.1 Number Notation

The most common form of number notation used in INTERDATA documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 2 lists the hexadecimal characters employed.

TABLE 2. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

To differentiate between decimal and hexadecimal numbers, hexadecimal numbers are preceded by the letter "X", and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are: X'1234', X'2EC6', X'A340, X'EEFA', and X'10B9'.

4.2 Part Numbering System

INTERDATA parts, drawings, and publications employ a common numbering system. The part number and drawing numbers for drawings which describe the part are related. The publication number is also often related to the part number of the device or program described. Figure 2 shows the format used for INTERDATA part numbers. The fields are described in the following paragraphs.

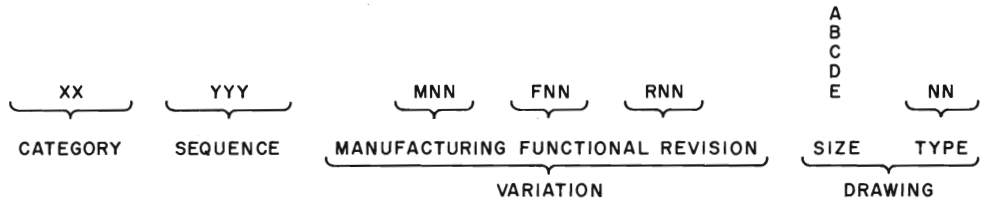


Figure 2. Part Number Format

4.2.1 Category Field. The two-digit Category number indicates the broad class or category to which a part belongs. Typical examples of category number assignments are:

01 - Basic Hardware Systems

02 - Basic Hardware Expansions

03 - Basic Software Systems

04 - Basic Software Expansions

05 - Major Application Programs

06 - Self-contained Utility Programs

07 - Subroutines of General Utility

10 - Spare Parts Packages

12 - Card File Assemblies

13 - Panels

17 - Wire and Cables

19 - Integrated Circuits

20 - Transistors

27 - Peripheral Equipment

29 - Manuals

34 - Power Supplies

35 - Assembled Printed Circuit Boards

36 - Electro-Mechanical Devices

4.2.2 Sequence Field. The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 2 are minimum lengths (insignificant zeros must be added to maintain these minimums).

4.2.3 Manufacturing Variation Field. The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

NOTE

A part number must contain a Category number and a Sequence number. All other fields are optional.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

An important exception to the meaning of the M Field exists for categories related to software. Here the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they could be in symbolic form. Thus, there are many ways to represent the same identical program. These ways are identified by the M Field numbers as follows:

M01 - Symbolic Punched Cards

M02 - Relative Binary Punched Cards

M03 - Absolute Binary Punched Cards

M04 - Symbolic Magnetic Tape

M05 - Relative Binary Magnetic Tape

M06 - Absolute Binary Magnetic Tape

M07 - Symbolic Punched Paper Tape

M08 - Relative Binary Punched Paper Tape

M09 - Absolute Binary Punched Paper Tape

M10 - Bootstrap Binary Object Punched Paper Tape

M11 - Read-Only-Memory (ROM) Absolute Binary Object Punched Paper Tape

M12 - ROM Wiring and Test Set (ROMWATS) Wiring Punched Paper Tape

M13 - ROMWATS Check Punched Paper Tape

M14 - Eight-bit Paper Tape

4.2.4 Functional Variation Field. The optional Functional Variation Field consists of the letter "F" followed by two digits. The F Field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For example, a power supply may be strapped internally to operate on either 110 vac or 220 vac. Except for this strap, all power supplies of this type are identical. The strapping option is easily described by a note on the assembly and test specification drawings. Therefore, this is a functional variation.

4.2.5 Revision Field. The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. R Field changes often reflect improvements. A part with a revision level HIGHER than the one specified will work. A part with a revision level LOWER than specified should not be used.

4.2.6 Drawing Field. The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A - $8\frac{1}{2}$" X 11"
B - 11" X 17"
C - 17" X 22"
D - 22" X 34"
E - 34" X 44"

The two digits indicate the drawing type as follows:

01 - Parts List
02 - Machine Details
03 - Assembly Details
05 - Art Details
06 - Wire Run List
08 - Schematic
09 - Test Specification
10 - Purchase Specification
11 - Bill of Material
12 - Information
13 - Program Listing
14 - Abstracts
15 - Program Description
16 - Operating Instructions
17 - Program Design Specification
18 - Flow Charts
19 - Product Specification
20 - Installation Specification
21 - Maintenance Specification
22 - Programming Specification

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4.2.7 Examples. The following list provides some examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060 The 60th printed-circuit board assigned a part number under this system.

35-060M01 A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.

35-060F01 A printed-circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.

35-060R01 A revised 35-060 printed-circuit board. Probably supercedes the 35-060.

35-060A01 The $8\frac{1}{2}$ by 11 inch parts list for a 35-060.

35-060B08 The 11 by 17 inch schematic for a 35-060.

06-072 The 72nd utility program assigned a part number.

06-072A13 An $8\frac{1}{2}$ by 11 inch listing of the 06-072 program.

06-072M03 An absolute binary deck of punched cards for the 06-072 program.

06-072A12 An $8\frac{1}{2}$ by 11 inch information drawing on the 06-072 program. Probably a part of the program.

29-060 The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

4.3 Drawing System

This section describes the drawings provided with INTERDATA equipment. Note that drawings provided with peripheral devices and other purchased items may vary from the system described in this Section.

A digital system may be divided into a collection of functionally independent circuits such as core memory, Processor, and I/O device controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each functional circuit is described electrically by a detailed functional schematic. Each schematic contains a variety of information including type and location of discrete integrated circuits (IC's), pin connections, all interconnections within the schematic connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register mnemonic name has a maximum of three letters, excluding "I, O, Q, and Z'.
2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant position, and continuing to N-1 on the right, where N is the number of bits in the register.
3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The IC's, mounted directly on the logic board, are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. Refer to Figure 3.

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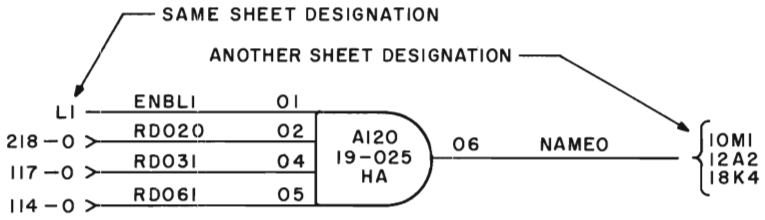


Figure 3. Example of a High Speed AND Gate.

The designations, numbers, and references shown in Figure 3 are:

A120 - This indicates the component location on the logic board. Figure 4 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connectors (Conn 0 and Conn 1) are on the right, the components are numbered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is A01 and the first capacitor is C1. Test points are lettered bottom to top from A-Y (omitting I, O, L, E).

19-025- The number 19 is the category number of ICs, and the 025 is the sequence number of the component.

HA - Indicates this component is a high speed AND gate. Some other common designations used are:

P - Power Gate
HP - High Speed Power Gate
G - Gate
HG - High Speed Gate
HGOC - High Speed Gate, Open Collector
B - Buffer
HB - High Speed Buffer

L1 - This input lead is from area L1 on the same schematic sheet.

10M1, 12A2, 18K4 - Indicate outputs to another logic schematic sheet.

218-0, 117-0, 114-0 - Indicate inputs from Connector 0.

Note that the pin numbers (01, 02, 04, 05, and 06) correspond directly to the actual IC pin numbers.

Figure 4 also shows the locations of the header connectors (Conn 0 and Conn 1) and the cable connectors (Conn 2 and Conn 3). All logic boards always contain Header Connectors 0 and 1, however, any combination (either, both, or none) of cable connectors (Conn 2 and Conn 3) may be provided.

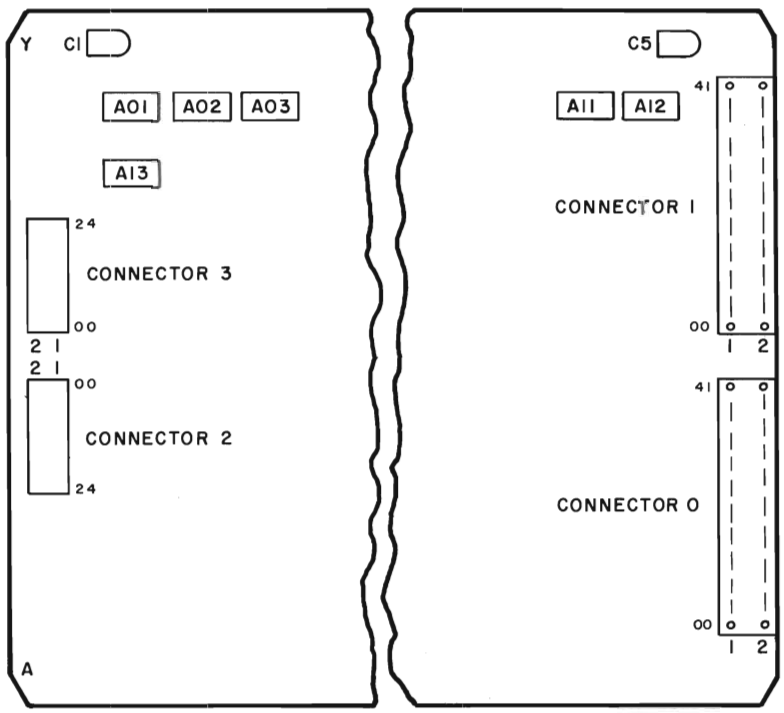


Figure 4. Example of a Logic Board Layout

Figure 5 provides the pin numbering scheme for the header and cable connectors. Header connectors always have 2 rows of pins and 42 positions. Cable connectors always have 2 rows of pins but may vary in the number of positions. The number of positions may only vary in increments of five positions (10 contacts). For instance, if 24 positions are desired, five blocks of five positions each (25 positions) must be used.

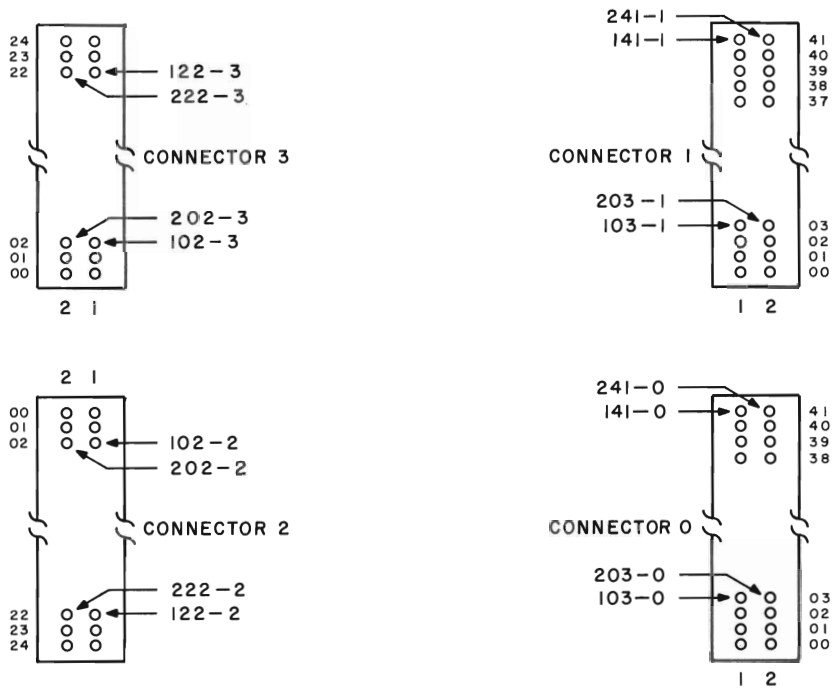


Figure 5. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually a collector where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules are observed.

1. All mnemonic names are a maximum of six characters.
2. All decimal digits and upper case letters except the letters "I, O, Q, and Z" are permitted.
3. No other characters permitted.
4. Where possible, mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a mnemonic exists.
5. Mnemonic names are not repeated within a schematic.
6. Every mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop would have the "1" state indicator, while the reset side would have the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion.
7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same mnemonic name. For example, assume a signal NAME1. NAME1 may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

Sometimes a net fans-out to many sheets in a schematic. It is also possible for a net to fan-out to sheets in different schematics. In these situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 3 is on a schematic, sheet 20. The output, NAME0, appears on sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 3, the ENBL1 may, however, have many other terminations in addition to the one shown. Generally then, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that in the Model 70 schematics, signals are co-ordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the Back Panel Map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 3, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figure 6 is a typical schematic sheet with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic Digital System and some of the more common expansions are commonly included in the rear of the appropriate Digital System Maintenance Manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.

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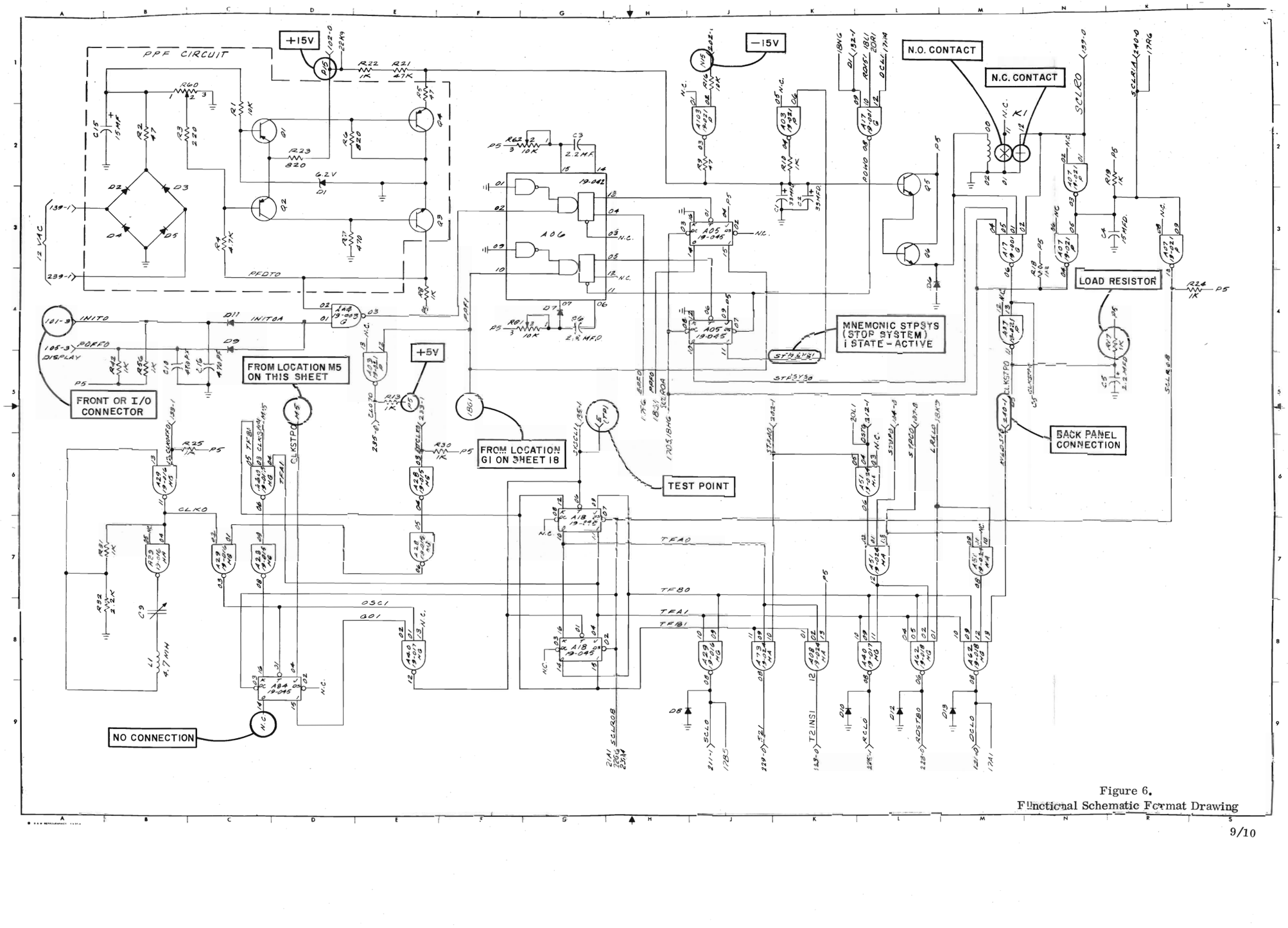


Figure 6.
Functional Schematic Format Drawing

MODEL 70 CHASSIS AND POWER SUPPLY EXPANSION INFORMATION SPECIFICATION

1. INTRODUCTION

The INTERDATA Model 70 Digital System features a highly modular structure which permits configurations to suit the user's exact needs. It provides the means for convenient expansion as the user's requirements grow. This document describes the Processor and System Expansion Chassis, Power Supply Mounting, Filler and Display Panel mounting, and the interconnecting cables. Integrated circuit boards are discussed with respect to cabling and location only. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals. Note that the following discussion assumes that the equipment is mounted in standard INTERDATA cabinets.

2. MECHANICAL COMPONENTS

This section is intended to familiarize the reader with the mechanical components that are discussed here (i.e. Cabinet Uprights, Chassis Support Rails, Filler Panels). Figures 1 through 4 provide the dimensions and mounting configurations for the Rack, Chassis Support Rails, and Filler/Display Panels. Note in Figure 4, that while 3 1/4", 7", and 10 1/2' Filler Panels and the Display Panel mount the same way (via retaining brackets), the smaller 1 3/4" Filler Panel mounts with spring clips.

3. POWER SUPPLY MOUNTING

The Power Supply mounts in the rear of the cabinet, behind the Processor or Expansion Chassis. It is attached to the right mounting upright (looking from rear). Either of two Power Supplies may be supplied with the Model 70 System.

34-012 Power Supply. This supply mounts to the upright via two mounting blocks and two nylon spacers. The mounting blocks mount to the upright with four 10-32 Hex Socket Cap Screws. See Figure 5.

WARNING

Before hinging out the power supplies, the rack levelling feet should be lowered. After the levellers are in contact with the floor surface, up to three power supplies may be hinged out at one time.

34-017 Power Supply. The 34-017 supply attaches to the mounting upright via four 10-32 X $\frac{1}{2}$ Lg PHPS screws. See Figure 6.

When either power supply is in the installed operating position, it is secured to the left rear upright by two 10-32 screws. The power supply cable connects to terminal lugs at the right rear (looking from rear) of its respective Processor or Expansion Chassis via faston lugs and a connector for fan A.C. power. Refer to Figure 7. There is adequate slack provided in the cable to allow the Power Supply to hinge out freely. In order to prevent the cable from being pinched between the Power Supply and the Chassis Support Rails, a service loop is required. A maximum of five power supplies may be mounted in one rack.

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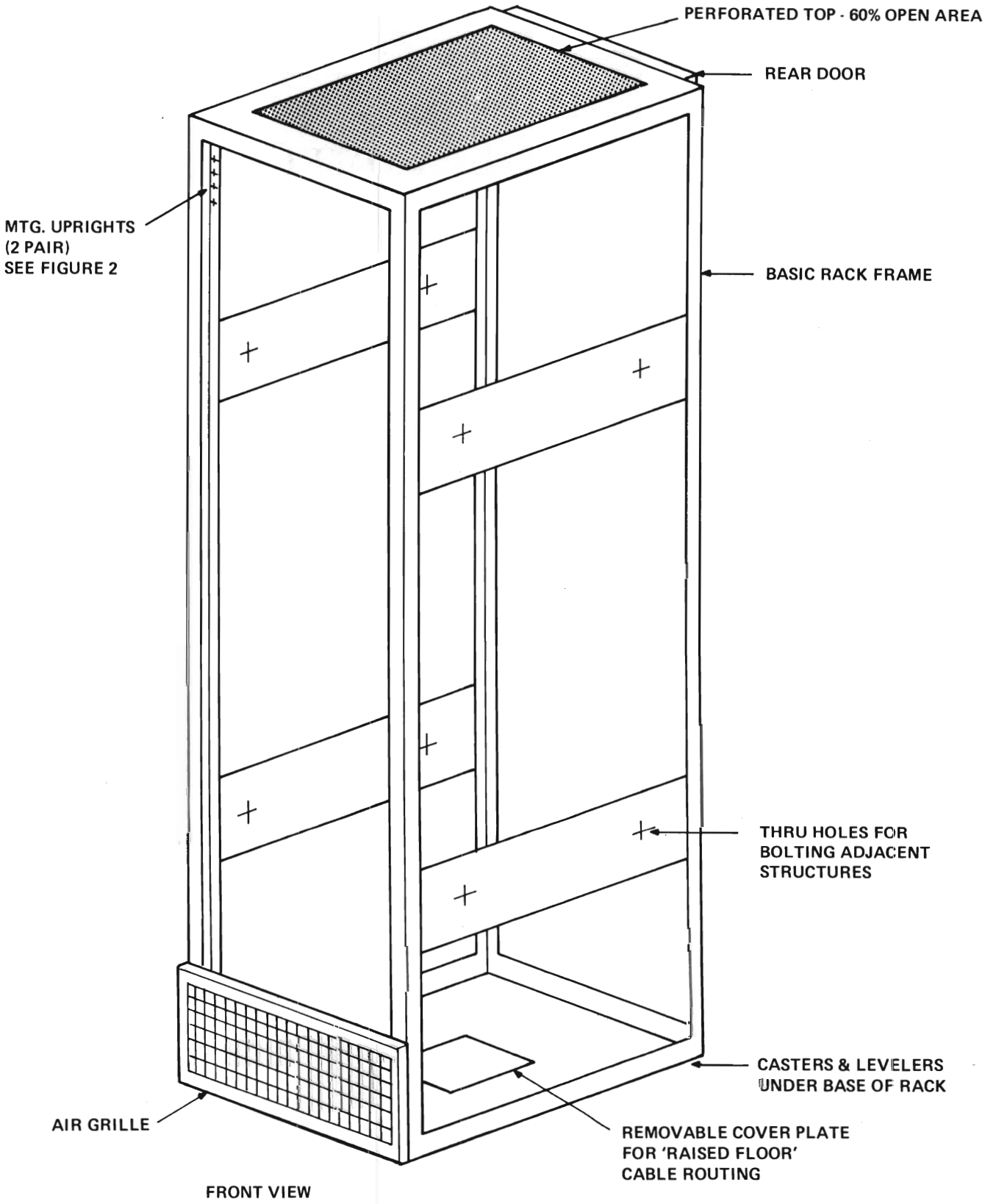


Figure 1. Basic Cabinet

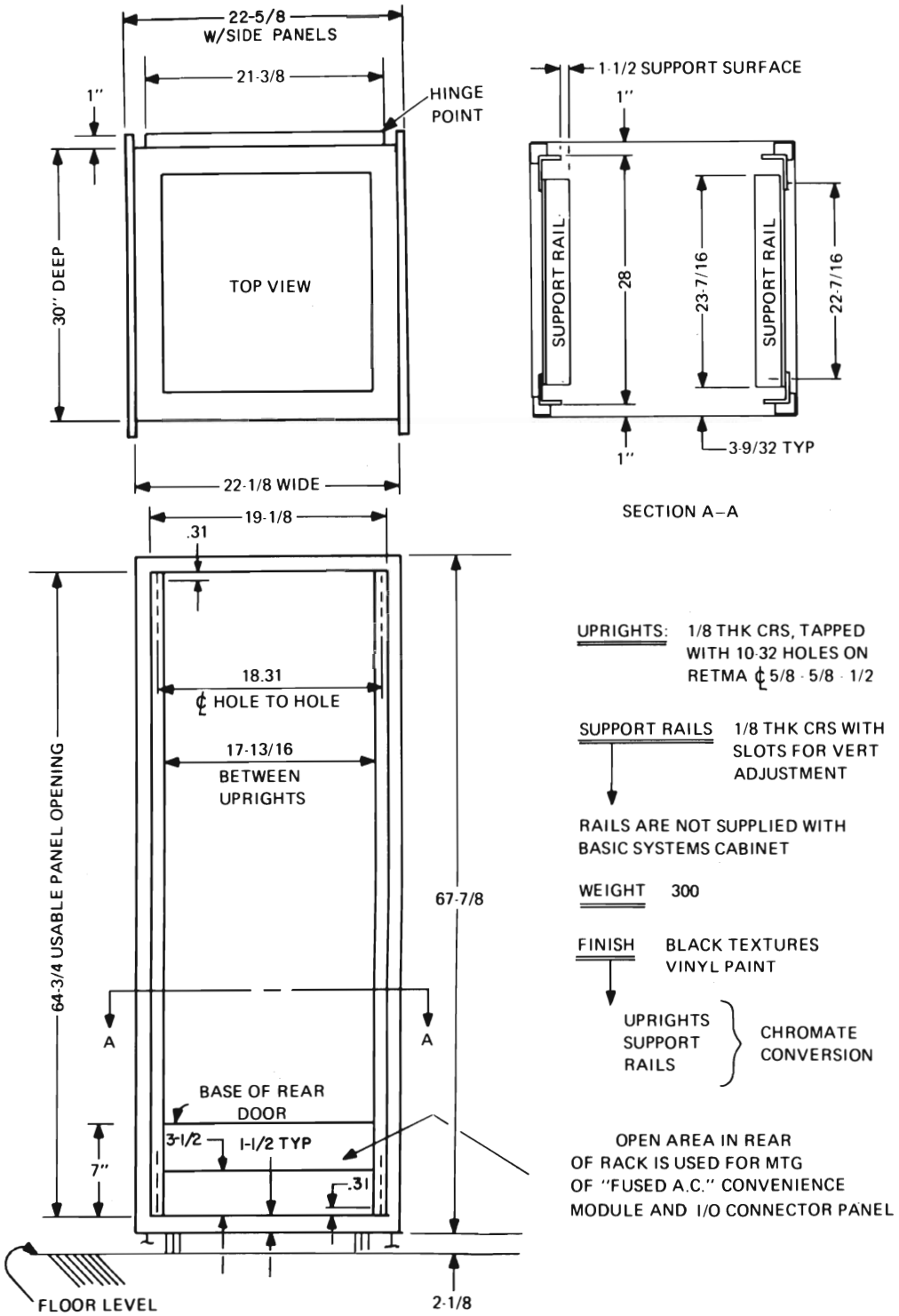


Figure 2. Basic Cabinet Physical Dimensions

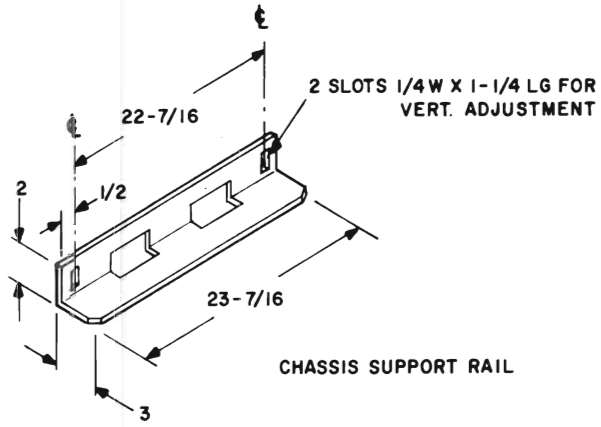


Figure 3. Chassis Support Rail

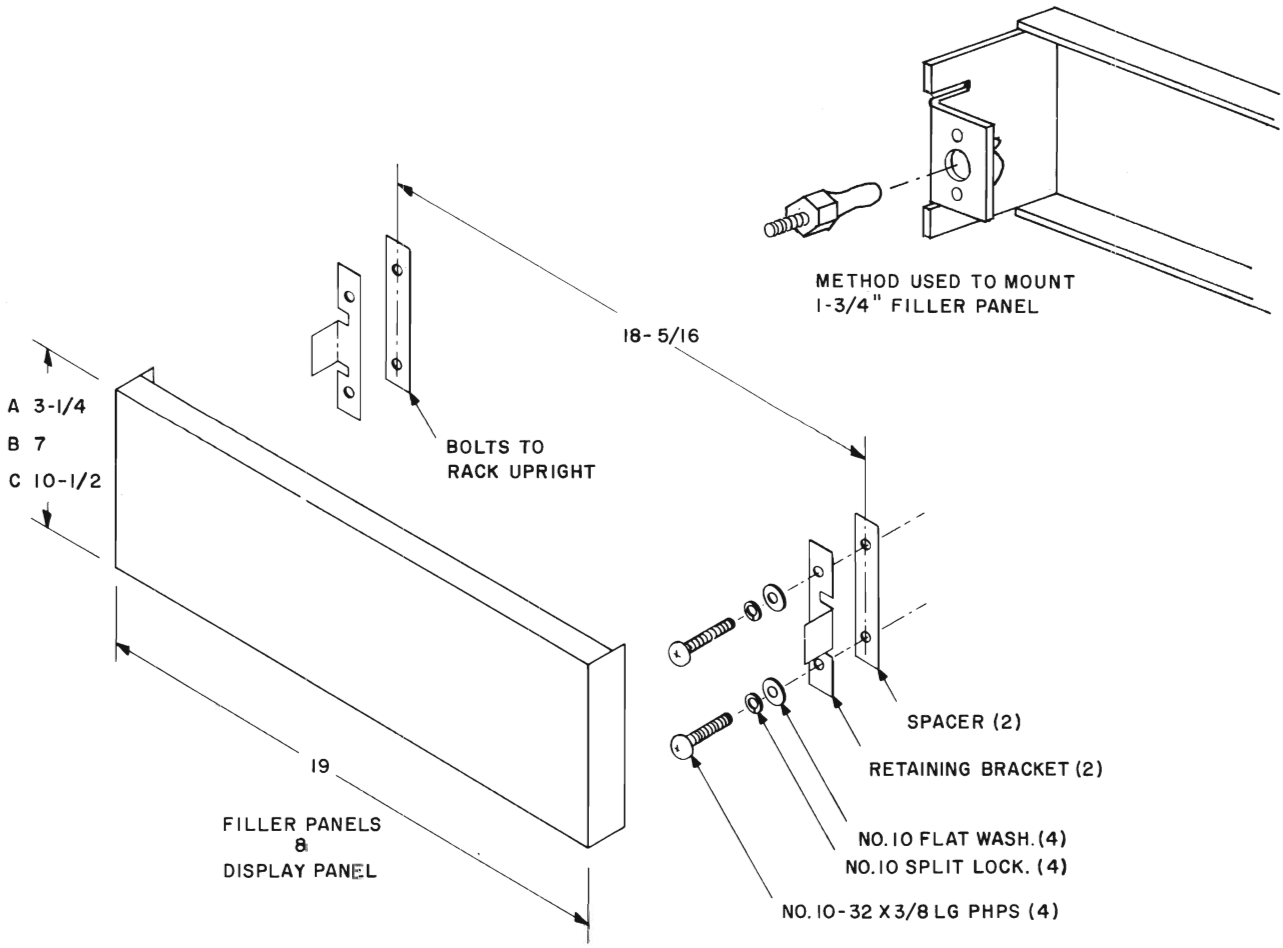


Figure 4. Typical Mounting Configuration for Display and Filler Panels

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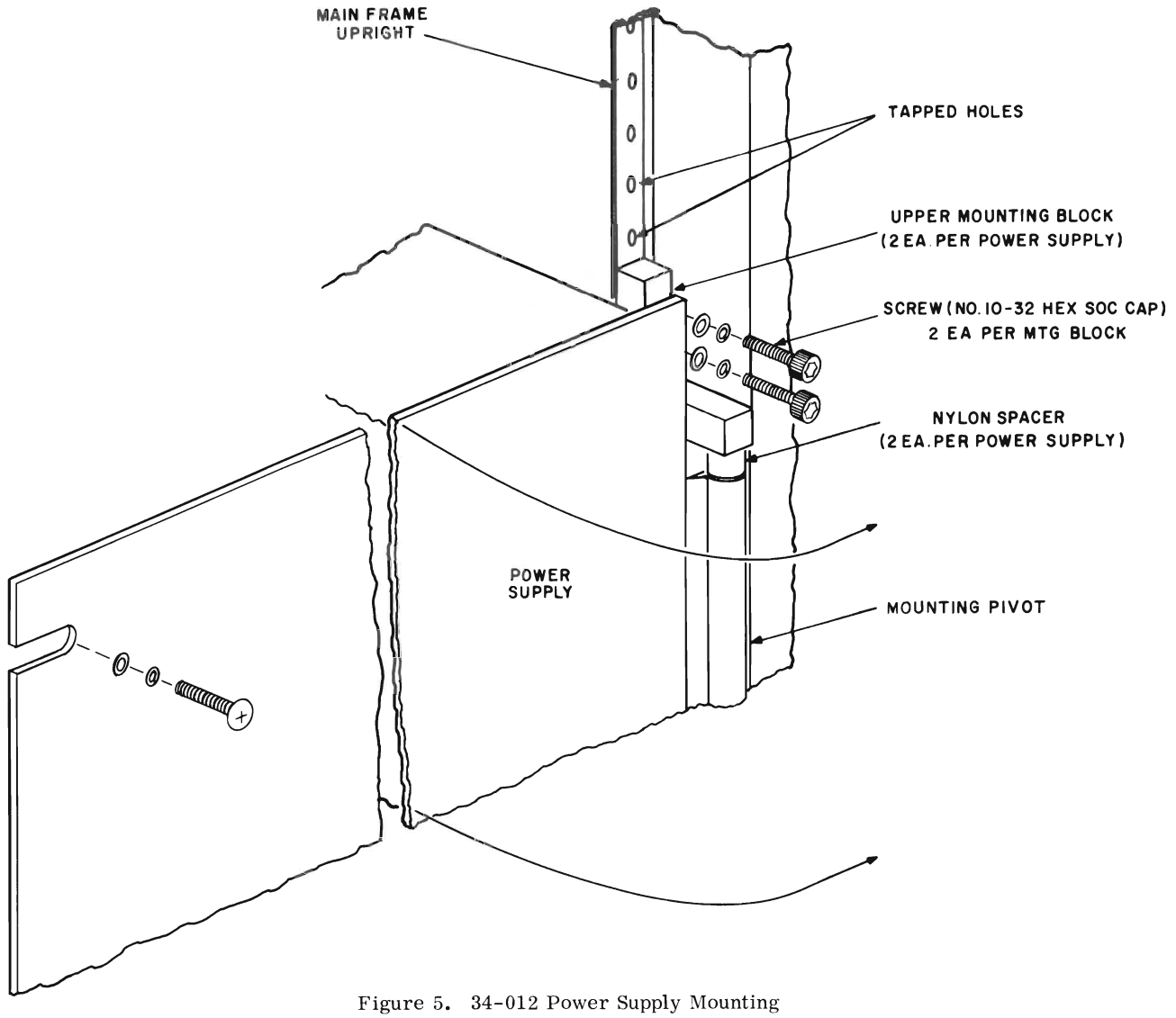


Figure 5. 34-012 Power Supply Mounting

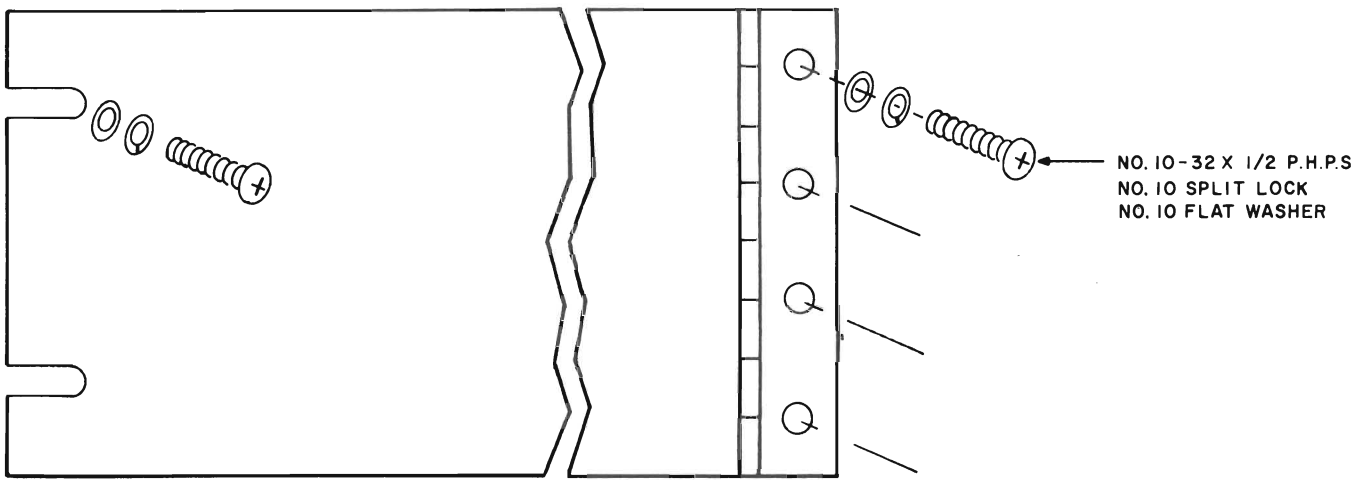


Figure 6. 34-017 Power Supply Mounting

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4. EXPANSION CHASSIS MOUNTING

Two Expansion Chassis (10 inch and 15 inch) are available for expanding the Model 70 Digital System. The Expansion Chassis have the same over-all dimensions as the Processor Chassis. See Section 5 on Configuration.

The Expansion Chassis slides into the rack on the two Chassis support rails (See Figures 2 and 3) from the front of the rack.

CAUTION

No chassis should be mounted in cantilever fashion. Chassis support rails MUST be used. If a rack cabinet other than an INTERDATA cabinet is used, consult rack manufacturer for proper support rails.

The chassis support rails are fastened to the mounting uprights at the front and rear of the rack. Slots are provided in the rails to allow vertical adjustment. The Expansion Chassis lock in place at the mounting uprights in front of the rack. The Expansion Chassis does not fasten in any way to the Chassis support rails. All Expansion Chassis mount below the Processor Chassis. Expansion Chassis cabling is discussed later in this document. Figure 7 shows Expansion Chassis location with respect to the filler panel and power supply.

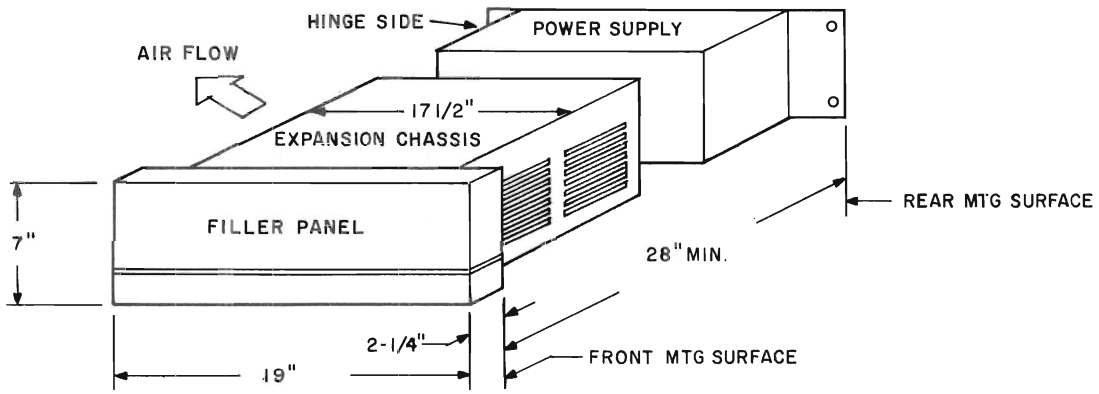


Figure 7. Expansion Chassis Location

4.1 15 Inch Expansion Chassis

The 15 inch Expansion Chassis contains eight universal expansion slots which can accept combinations of memory modules, single board peripheral controllers, system modules, selector channels, or user designed interfaces. Included with this chassis are the cooling fans and interconnecting cables. The chassis may be ordered with or without a power supply.

4.1.1 7 and 10 Inch Boards in a 15 Inch Chassis. A 10 inch I/O Controller (provided it does not use Connector 1) may be inserted in a 25 inch chassis via the 02-234 I/O Adapter Kit. (See Figure 8). One or two 7 inch boards (half boards) may be inserted into a 15" chassis via the 16-398 Half Board Adapter Kit (see Figure 9). The Half Board Adapter Kit may hold two active 7" boards or one active and one blank 7" board, depending on requirements. No wiring takes place between the boards and the adapters. The adapters are designed such that the connectors on the boards plug directly into the Expansion Chassis.

4.2 10 Inch Expansion Chassis

The 10 inch Expansion Chassis contains six 10 inch I/O expansion slots which can accept any combination of up to six wire-wrap or copper peripheral controllers, systems modules, or user designed interfaces. Included with the chassis are the cooling fan and system interconnecting cables. The Power Supply is separate. Power for this chassis is supplied by the system power supply.

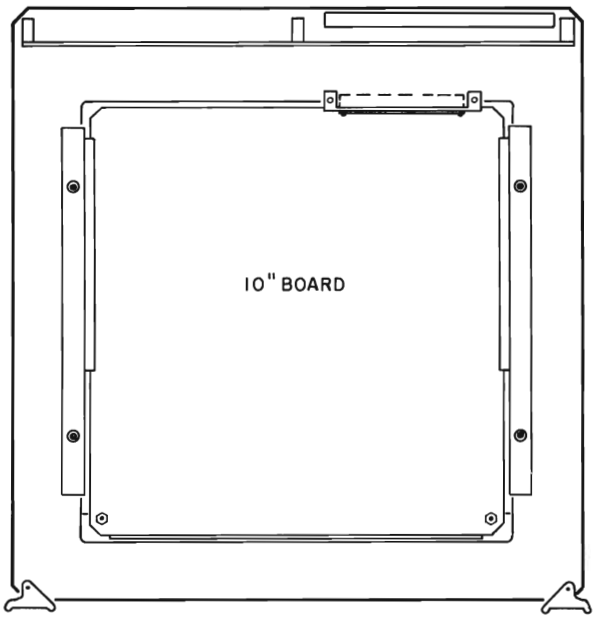
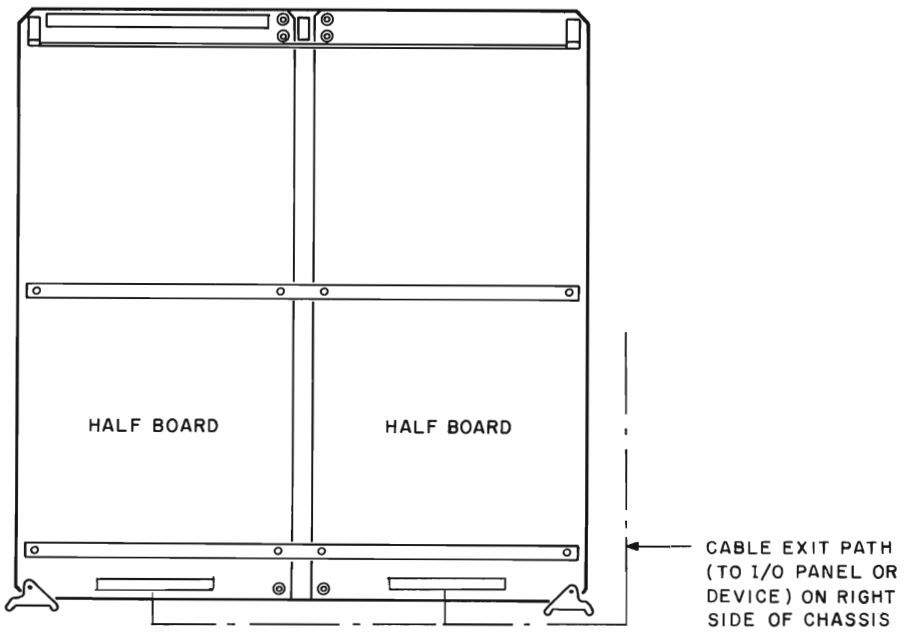


Figure 8. 02-234 I/O Adapter



NOTE: 35-398 HALF BOARD CAN BE LOCATED ON EITHER SIDE.

Figure 9. 16-398 Half Board Adapter

5. CONFIGURATION

5.1 System Expansion Chassis

When configuring a multi-chassis system there are four rules that must be followed:

1. The system expansion chassis must be mounted below the basic Processor chassis.
2. All chassis must be contiguous.
3. All 15 inch system expansion chassis must be mounted above the 10 inch system expansion chassis.
4. Multiboard peripheral device controllers (on 10 inch circuit boards) can only be used in the 10 inch system expansion chassis.

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5.2 Circuit Board Distribution

Model 70 Digital System may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and the system expansion chassis. See Figure 1

1. The Selector Channel can only be placed in Slot 0 of the Processor Chassis (and Slot 2 if the system contains a maximum of 8KB core memory), or Slots 6, 4, 2, or 0 of the system expansion chassis.

2. All slots below the position where the SELCH is inserted become SELCH Bus slots. (This only applies within the chassis containing the SELCH.) The SELCH Bus extends down the left side connectors (front view). Note that all 7", and 10" with adapter, device controllers connect to the Multiplexor Bus from the right side connectors (front view). Therefore, these device controllers may be inserted in vacant SELCH Bus slots.

3. The SELCH Bus can be extended by cable to any even numbered slot in an I/O chassis adjacent to the chassis containing the SELCH controller.

4. The Universal Clock module (7" x 15") is always mounted on the right side (front view).

5. The Memory Protect module (7" x 15") is always mounted on the left side, and is normally mounted with the Universal Clock module.

6. All device addresses are hard-wired on the device controller cards, so that the distribution of I/O device controllers in the chassis normally need only be considered as a matter of convenience.

7. Slots 3, 2, 1, and 0 of the Processor chassis and all slots of the universal expansion chassis are prewired with memory module addresses for up to 64KB. It is mandatory that these slots be used for memory when, and if, required.

8. The 15 inch system expansion chassis, and the basic Processor chassis may only be used for single board I/O device controllers. For multi-board 10 inch device controllers, use the 10 inch system expansion chassis.

9. The Memory Protect module must be placed in the first available I/O slot.

NOTE

The Memory Protect Module must be placed ahead of all other I/O device controllers with respect to the device interrupt priority, including the SELCH.

10. Priority is established by the physical placement within a chassis. After the Memory Protect and the Universal Clock modules, priority for interrupt driven devices should normally be established in order of descending speed, i.e. , drum higher than magnetic tape, and card reader higher than a paper tape reader, etc.

INTERDATA Configuration Data Sheet B, Figure 10, shows an example of circuit board distribution in the basic Processor and System expansion chassis.

5.3 Back Panel Wiring

Control Line CL050 from the Processor carries the Interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with Interrupt Control circuits.

Back panel wiring for interrupt control at a given position is: the Received ACK (RACK0) at Pin 122-1 and the Transmitted ACK (TACK0) at Pin 222-1. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 of a given position to Terminal 122-1 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 and 222-1 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller, the jumper from 122-1 to 222-1 must be removed from the back panel at that position.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices (i.e. SELCH, Memory Protect Module, etc.), see the appropriate installation specification.

5.4 System Configuration

System configuration data is provided in the Model 70 User's Manual, Publication Number 29-261.

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CONFIGURATION DATA SHEET "B" — CHASSIS, FRONT VIEW

SALES ORDER NO.: _____ P.O. OR QUOTE NO.: _____

CUSTOMER: _____ DATE: _____

SALESMAN — COMPLETED BY: _____

IN-HOUSE PERSONNEL: _____

PROCESSOR BOARDS	CONN I → SELECTOR BUS OR BUFFERED BUS	CONN O → INTERLEAVED DATA CHANNEL		CABLING CONN I	CABLING CONN O	+5	+16	-16	
1st 8KB			7						17-
2nd 8KB, SELCH, MBFR			6						17-
3rd 8KB			5						17-
4th 8KB, SELCH, MBFR			4						17-
5th 8KB			3						☐ M49-000 6 EA. 10" CARDS
6th 8KB, SELCH, MBFR			2						☐ M49-001 8 EA. 15" CARDS
7th 8KB			1						☐ M49-002 POWER SUPPLY
8th 8KB			0						
7th 8KB, SELCH, MBFR			7*						17-
6th 8KB			6*						17-
5th 8KB, SELCH, MBFR			5						17-
I/O ONLY			4						17-
I/O ONLY OR MBFR			3						☐ M49-000 6 EA. 10" CARDS
I/O ONLY			2						☐ M49-001 8 EA. 15" CARDS
I/O ONLY OR MBFR			1						☐ M49-002 POWER SUPPLY
I/O ONLY			0						
I/O ONLY OR MBFR			7*						17-
I/O ONLY			6*						17-
I/O ONLY OR MBFR			5						17-
I/O ONLY			4						17-
I/O ONLY OR MBFR			3						☐ M49-000 6 EA. 10" CARDS
I/O ONLY			2						☐ M49-001 8 EA. 15" CARDS
I/O ONLY OR MBFR			1						☐ M49-002 POWER SUPPLY
I/O ONLY			0						
I/O ONLY OR MBFR			7*						17-
I/O ONLY			6*						17-
I/O ONLY OR MBFR			5						17-
I/O ONLY			4						17-
I/O ONLY OR MBFR			3						☐ M49-000 6 EA. 10" CARDS
I/O ONLY			2						☐ M49-001 8 EA. 15" CARDS
I/O ONLY OR MBFR			1						☐ M49-002 POWER SUPPLY
			0						

MBFR = M48-005 MULTIPLEXOR BUS BUFFER

17-162 = CONN 0 I/O AND MEM BUS CABLE 4"

17-163 = CONN 1 I/O AND MEM BUS CABLE 4"

17-164 = CONN 0 I/O AND MEM BUS CABLE 9"

17-165 = CONN 1 I/O AND MEM BUS CABLE 9"

17-166 = CONN 0 15" TO 10" CHASSIS 36"

17-167 = CONN 1 15" TO 10" CHASSIS 36"

17-168 = (CONN 1) 10" TO 10" CHASSIS 36"

* SLOT IS NOT AVAILABLE ON M49-000 EXPANSION CHASSIS

—o— = THE MULTIPLEXOR BUS MAY BE CUT HERE

—✕— = THE MULTIPLEXOR BUS IS CUT

--► = DEVICE PRIORITY (ACKNOWLEDGE) LINE

A744-4

Figure 10. Configuration Data Sheet "B" (Chassis-Front View)

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6. CABLES

6.1 Power Cable

The standard six foot rack is wired for 30 AMP service. A three wire, twist lock, grounding, 30 AMP, 125 VAC receptacle (Hubbell # 2610 or equivalent) is required to accept this plug.

6.2 Jumpers

Drawing 01-051 C12, provided in the Model 70 Maintenance Manual, Publication Number 29-266, provides the various jumper part numbers and configurations used between Power Supplies and Expansion Chassis in the Model 70. A detailed view of the terminal boards at the front and rear of the Expansion Chassis is shown in Figure 11.

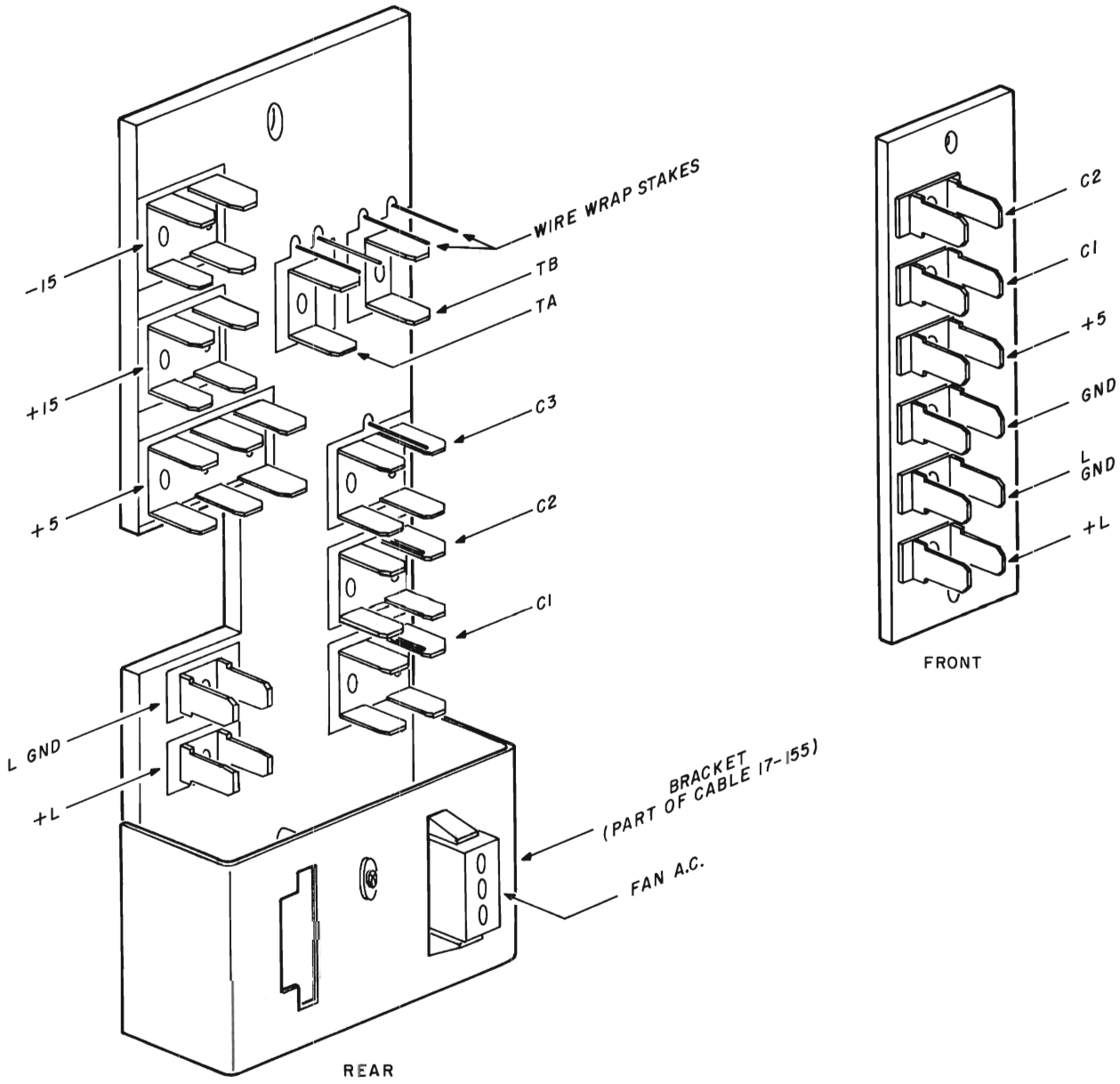


Figure 11. Terminal Boards

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7. NEW POWER SUPPLY

INTERDATA now has several new Power Supplies available for use with its line of digital systems. These supplies are manufactured by INTERDATA, and may replace those previously used. This section provides information on these new supplies, and on several associated changes to INTERDATA systems.

There are three power supplies now available:

Model Number 34-012 Power Supply. The 34-012 is the original power supply. This unit has a transformer that always supplies 115V for fan power at both 115V and 230V strappings. It supplies chassis fan power with a male connector.

Model Number 34-017 Power Supply. The 34-017 is the 25 ampere version of the INTERDATA supply. This unit supplies 115V or 230V depending on AC source for fan power. Chassis fan power is supplied with a U. L. approved female connector.

Model Number 34-020 Power Supply. The 34-020 is the 50 ampere version of the INTERDATA supply. The fan power consideration and the output connector are the same as for the 34-017 unit.

Two types of fan jumper cables are provided. Cable 17-181 is wired with two male connectors, while cable 17-287 is wired with one male and one female connector.

Because the newer power supplies supply line power for the fans, it is necessary to re-wire the fans in the chassis to operate with 230VAC. The New Chassis provides an AC power switch for switching fan power to either voltage. When using the newer supplies (34-017 or 34-020) with the former chassis, only 115V operation is possible, unless the chassis is modified as shown in Section 8 which follows.

8. CONFIGURATION DATA

The 34-012 may be replaced in the following ways.

25 AMP	34-012 (1 each)	Replaced by 34-017 (1 each)
50 AMP	34-012 (2 each)	Replaced by 34-020 (1 each)

The following paragraphs outline the factors involved in using different combinations of chassis, power supplies, and cables.

1. The 34-012 with the "Former Chassis".

   This unit is used for 115/230V operation. The "Former Chassis" (1 or 2 fan) is wired for 115V operation and equipped with two female connectors for fan power. Refer to Figure 12.

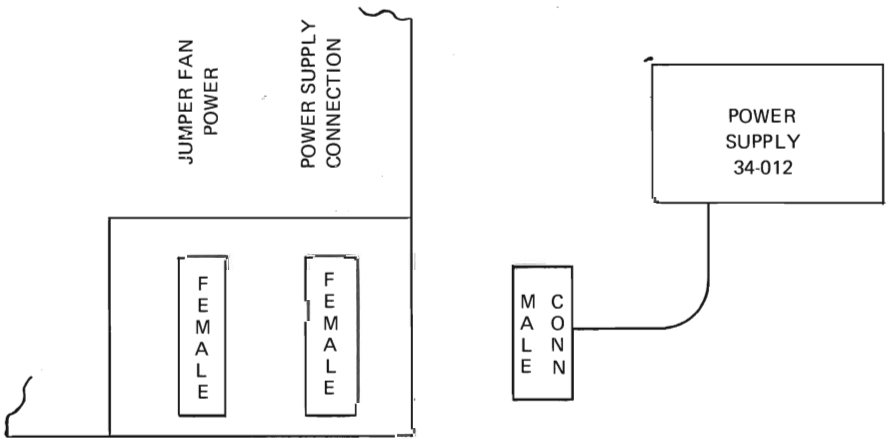


Figure 12. Former Chassis

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2. The 34-012 Power Supply with a "New Chassis".

This unit is used for 115/230V operation, however, the 115/230V fan switch on the "new chassis" must remain in the 115V position for 115V or 230V operation. If two or more "new chassis" are powered, standard fan jumper cable, 17-181, must be replaced by cable 17-287.

NOTE

The "new chassis" (1 or 2 fan) is wired for 115/230V fan operation and equipped with one male and one female connector for fan power. See Figure 13.

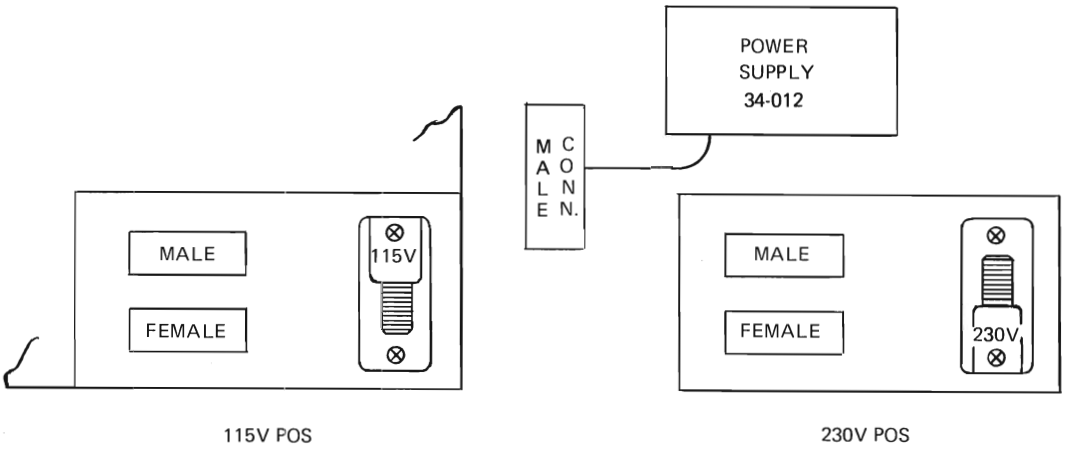


Figure 13. New Chassis

3. The 34-017 Power Supply with a "New Chassis".

This unit is used for 115/230V operation, however, the 115/230V fan switch on the chassis must be matched with the 115V or 230V strapping in the Power Supply.

4. The 34-017 Power Supply with a "Former Chassis".

This unit is used for 115V operation (ONLY) using cable 17-181.

NOTE

The "former chassis" must be rewired for 230V operation. Kits 39-020F01 (1 fan) and 39-020F02 (2 fans) must be used to convert a chassis wired for 115V to 115/230V fan operation.

EXHAUST FANS

New exhaust fan plates are equipped with a switch to provide either 115 or 230VAC operation. See Figure 14.

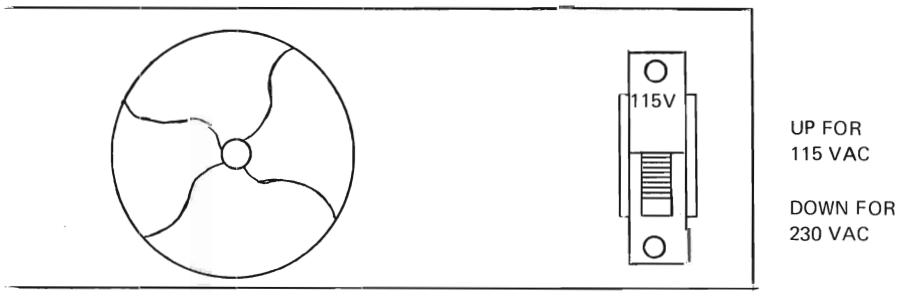


Figure 14. Fan Switch Setting

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WARNING

All AC fan connectors on Power Supplies which are not connected to mating receptacles MUST remain covered or shorting may occur. See Figure 15.

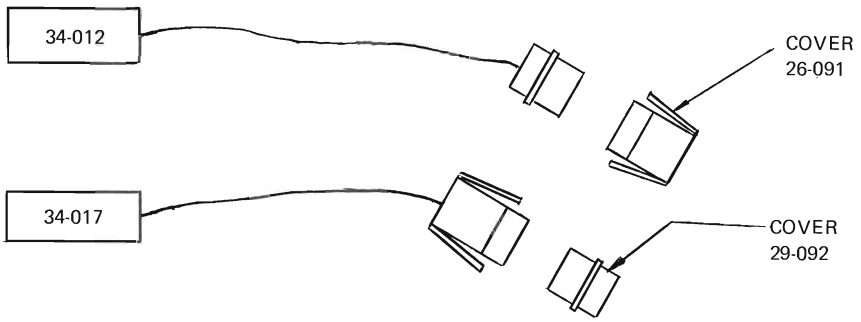


Figure 15. Fan Connector Caps

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PROCESSOR

01-051F01R01A21
March 1974

MODEL 70
MAINTENANCE SPECIFICATION

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MODEL 70
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The INTERDATA Model 70 Digital System is a low cost, general purpose system, versatile enough to perform a wide range of industrial control, data processing, and scientific computation. The Model 70 is well suited to the real-time scanning of hundreds of instrument readings, process alarms, and pulse trains. It is particularly useful where larger amounts of main processor time are needed for computation.

This specification provides maintenance information for the Model 70 Processor. A block diagram analysis is followed by functional descriptions of major processor areas with reference to functional schematics.

2. BLOCK DIAGRAM ANALYSIS

Figure 1 is a block diagram of a Model 70 Digital System. Processor operation is controlled by the Read-Only-Memory (ROM). The micro-program in the ROM makes the Model 70 appear to have the capabilities of a much larger machine. When executing the instructions of the emulated computer, the micro-program directs the hardware to read the instruction from core memory. The hardware decodes the user's instruction and steers the micro-program to a micro-subroutine that performs the emulated instruction. When the subroutine is finished, the micro-program directs the hardware to read the next instruction from core memory, thus closing the loop.

The micro-program in the ROM consists of combinations of micro-instructions. Each micro-instruction performs a basic machine operation. Table 1 lists the 16 different micro-instructions.

TABLE 1. MICRO-INSTRUCTIONS

INSTRUCTION	OP-CODE
DO	0000
COMMAND	0001
TEST	0010
BRANCH	0011
LOAD	0100
LOAD IMMEDIATE	0101
OR	0110
OR IMMEDIATE	0111
AND	1000
AND IMMEDIATE	1001
EXCLUSIVE OR	1010
EXCLUSIVE OR IMMEDIATE	1011
ADD	1100
ADD IMMEDIATE	1101
SUBTRACT	1110
SUBTRACT IMMEDIATE	1111

The Read-Only-Memory (ROM) is a high speed, solid state, non-destructive memory used to contain the micro-program. The Model 70 micro-program occupies 1536 words of ROM. Space is provided for an additional 512 words. Micro-instruction cycle time is approximately 250 nanoseconds.

The ROM location of a micro-instruction is defined by the 12-bit address contained in the ROM Address Slave Register (RAS) and the ROM Address Lower Register (RAL). RAL is an eight-bit micro-instruction location counter. It is loaded from the S Bus during a Branch Micro-instruction, or when specified as a Destination Register. RAL increments, by one, between the execution of all other micro-instructions so that it holds the address of the next micro-instruction to be executed. RAS is a four-bit register that holds the ROM page number. It is loaded from the ROM Address Higher Register (RAH) whenever RAL is loaded from the S Bus. Neither the RAS nor the RAH is involved when the RAL is incremented.

To transfer from one page (256 ROM words) to another, the destination page number is first loaded into RAH from the S Bus. When the location address is loaded into RAL, RAS is loaded from RAH. This insures that all 12-bits of the new ROM address are sensed simultaneously.

The ROM Address Registers may also be loaded from the Decoder Read-Only-Memory (DROM). All 12-bits are loaded in parallel from the DROM read-out. RAH and RAS are loaded with the same page number.

Every micro-instruction read from ROM is placed in the ROM Data Register (RD) where it remains until the micro-instruction is executed and the next micro-instruction is read out. The output from the RD is input to the Processor control logic.

The control logic decodes the micro-instruction and activates the gating leads to the Arithmetic Logic Unit (ALU). The Source and Destination addresses are decoded, and the signals to unload registers to the B Bus and load registers from the S Bus are generated. Core memory activity and Input/Output operations are initiated in the control logic as well as the signals directing the clock system and initialize circuits.

The OP field (RD 0:3) is decoded as the operation code of the micro-instruction being executed. RD Bit-3 defines Immediate instructions. An Immediate instruction is one that has the data to be manipulated appended to the micro-instruction word itself. During the execution of an Immediate instruction or a Branch instruction RD Bits 8:15 are gated onto B Bus Bits 8:15, and treated as data.

The D Field (RD 4:7) specifies the destination of the micro-instruction result formed in the ALU. The result is placed on the S Bus by the ALU and then gated to the Destination Register specified by the D field.

The S field (RD 8:11) specifies the register to be gated to the B Bus. The selected register is the source of one operand to participate in arithmetic or logical operations. The other operand is in the A Register (AR).

The E field (RD 12:15) is an extended micro-operation modifier. This field provides control of flag actions, shifts, or I/O operations.

The Instruction Register (IR) is a 16-bit register used to hold the user instruction currently being executed. The OP field of IR (IR 0:7) holds the user's operation code. The meaning of the remaining bits depends on the type of instruction. Generally the following applies. The YD field (IR 8:11) specifies the Destination Register of the user's result. The S Bus data is gated into the General Register specified by this field. The YD field can also specify a Condition Code (CC) to match in the case of a user Branch instruction. The YS field (IR 12:15) selects the General Register to be gated to the B Bus as an operand. The IR is automatically loaded directly from core memory during the instruction fetch phase. The IR may also be loaded from the S Bus when specified as the destination in a micro-instruction. A provision is made to unload the entire IR to the B Bus or just the YD field (IR 8:11). The YD field (IR 8:11) is ANDed with the Condition Code field of PSW to assist the emulation of user's Branch instructions (MSK).

The outputs of the Instruction Register are input to Control. The user's instruction is interpreted and, through the Decoder Read-Only-Memory (DROM), the micro-program is steered to the subroutine designed to execute the user's instruction. The resulting 12-bit read-out is jammed into RAH/RAS and RAL.

The Flag Register (FLR) is a four-bit register containing the following flags: Carry (C), Overflow (V), Greater than zero (G), and Less than zero (L). These flags are modified at the conclusion of arithmetic and logical micro-operations to reflect the result of the operation. The FLR is tested by the Branch Micro-instruction. The FLR can be loaded from S Bus Bits 12:15 and unloaded to the Condition Code field of PSW.

The Program Status Word (PSW) is a 16-bit register used to define the system status relative to the user program being executed. Bits 0:11, the Status field, may be loaded from S Bus Bits 0:11. Some of the status bits have hardware significance, while others are of significance only to the emulator. Bits 12:15, the Condition Code field (CC), may be loaded from the micro Flag Register (FLR). When PSW is loaded from the S Bus, Bits 12:15 of the S Bus are captured in the FLR. PSW (12:15) remains unchanged.

The Alarm Register (ALRM) is a three-bit register containing the following flags: Parity Fail on Data Read (PFD), Parity Fail on Instruction Read (PFI), and Early Power Fail detect (EPF). The alarm bits can also be loaded into the Condition Code field of PSW.

The micro-register stack contains three general purpose registers (MR0, MR1, and MR2) and one special purpose register, the Location Counter (LOC). The Location Counter (LOC) is a 16-bit appendum to PSW holding the memory address of the next user instruction to be emulated.

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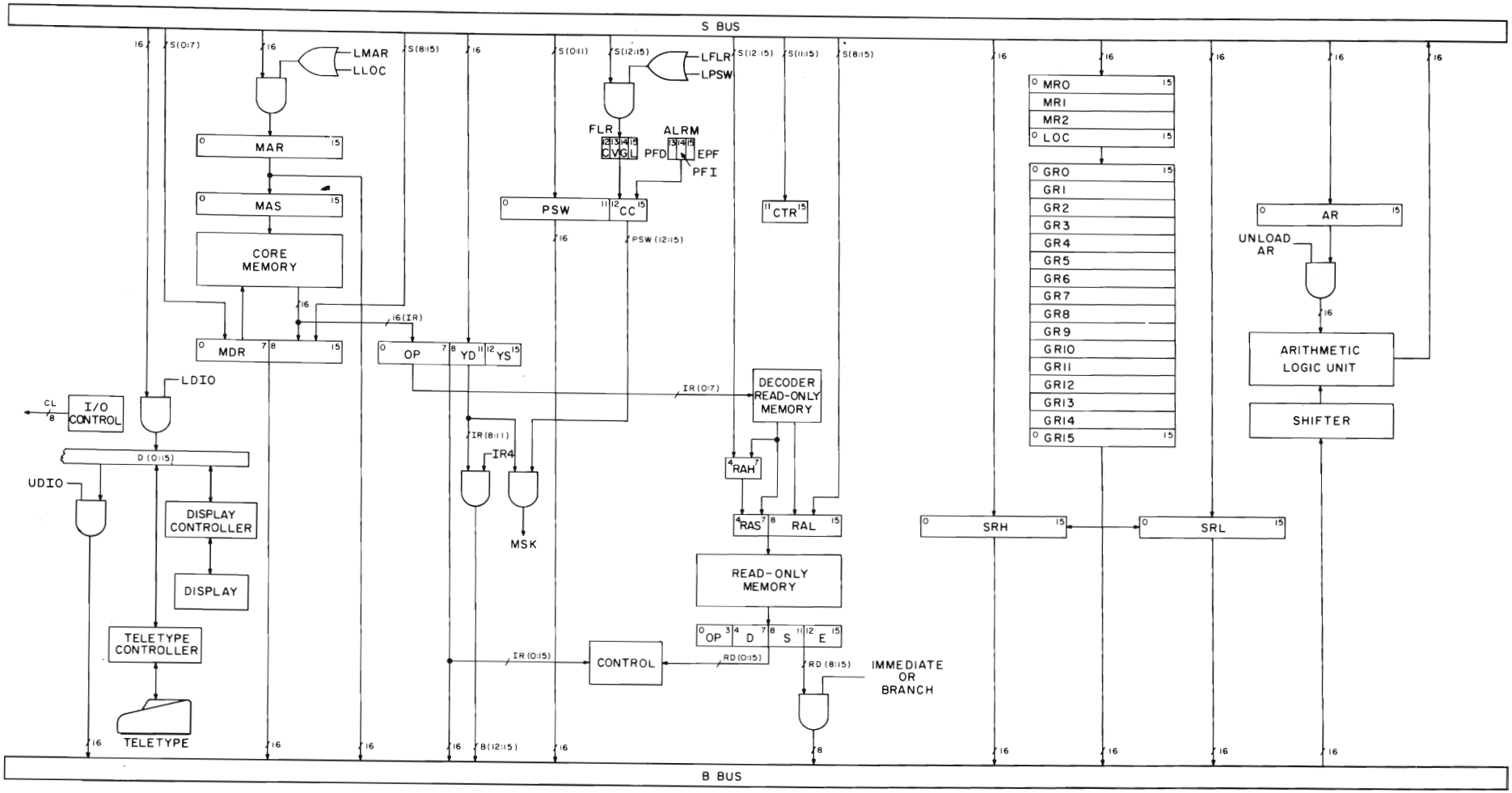


Figure 1. Model 70 Digital System

The user's register stack consists of 16 general purpose registers (GR0 through GR15). These registers are each 16-bits long and may be addressed only from the YD and YS fields of the IR. The micro-program accesses the General Register by specifying the field of IR - YD or YS - that contains the desired register address.

The Shift Registers High and Low (SRH and SRL) are two 16-bit general purpose micro-registers that can also be used in combination as a 32-bit shift register. The extended shift capability is used in multiply, divide, and other double precision operations.

The Arithmetic Logic Unit (ALU) performs the arithmetic or logical operation specified by RD. The operation executed is determined by the control lines activated when the control logic decodes the micro-instruction.

The B Bus, through the Shifter, provides one operand to the ALU. The Shifter performs Shift Left, Shift Right, Cross Shift, or direct gating of the B Bus data. The other operand is taken from the A Register (AR). The AR is a 16-bit register that can be loaded from the S Bus and input to the ALU as the second operand, if needed by the instruction being executed. The output from the ALU is the 16-bit S Bus.

The Counter (CTR) is a five-bit decrementing register used on multiply, divide, and repeat operations, and on the Branch on Counter Micro-instruction. The Counter is initialized to a count of 16; however, it may be pre-loaded with any value from 0 to 31 from the S Bus Bits 11:15.

The core memory is the source of user instructions and data constants. It contains 4K to 32K 16-bit locations. Memory operations are initiated by the control logic during a DO or Command Micro-instruction or by Direct Memory Access devices. For Processor initiated memory operations, the location selected in core memory is designated by the 16-bit Memory Address Slave Register (MAS). MAS is updated from the 16-bit outer-rank Memory Address Register (MAR) whenever a memory operation is not in progress. MAR may be loaded from the S Bus at any time and unloaded to the B Bus. Whenever the Location Counter (LOC) is loaded from the S Bus, MAR is also loaded with the same data. The 16-bits read-out or written into the addressed memory location are buffered in the Memory Data Register (MDR). MDR is separated into two eight-bit halves which may be loaded simultaneously or individually from the S Bus.

The memory timing signals are generated in the Processor. The Processor also resolves memory usage conflicts, handling external and internal requests for memory access. If the Processor attempts to unload MDR when memory data is not yet available, or load the MDR, or initiate another memory cycle when memory is still busy from the previous access, the Processor waits until memory data is available or the currect access is completed. Non-memory oriented operations may be interleaved with memory operations for maximum efficiency.

The Processor controls the multiplexed I/O Bus by directing device controllers to load data onto the D Bus or to accept data from the D Bus. The D Bus is a 16-bit bi-directional bus that can receive data from the S Bus or present data to the B Bus. The nature of the data on the D Bus is determined by the particular control line that has been activated.

The device controllers for the Control Console and the ASR 33 or 35 Teletype are built into the Model 70 Processor.

3. FUNCTIONAL DESCRIPTIONS

This section describes the major functional areas of the Processor. The descriptions reference both simplified drawings provided in this section, and the Processor Functional Schematic, 01-051D08.

3.1 Clock Control

The clock generator is shown on Sheet 19 and is located on the 35-390 I/O mother-board. The clock system employs a free-running 16MHz oscillator. The sinusiodal oscillator output (19C6) is ORed with the normally high External Clock (EXTCLK0)(19E6) producing OSC1 (19C7). The EXTCLK0 lead is provided so that an external clock may be used to run the system during troubleshooting. This is accomplished by grounding the CLKOFF0 lead to Pin 133-1 on the back panel to disable the internal oscillator, and then pulsing the EXTCLK0 lead. The external oscillator used should meet the following specifications:

1. Logic levels 0 to +0.45VDC for logic Zero.
   +2.6 to +5 VDC for logic One.

2. Square wave output, frequency up to 16 MHz.

3. Output drive = 7 milliamperes.

The Oscillator output (OSC1) is connected to the T input of the GO flip-flop (19C8). The K input to the GO flip-flop is tied to CLKSTP1 (19C5). When the system is initialized, CLKSTP1 goes high. The GO flip-flop toggles reset and SYSCL1 (19G5) is inhibited until the initialize sequence is terminated. At this time, CLKSTP1 goes low and shortly thereafter CLKSTP0 on the J input goes high. The GO flip-flop sets on the next negative going transition of OSC1. SYSCL1 is enabled by a high GO1 and a low CLKSTP1.

The oscillator is adjustable (via the variable Capacitor, C9) over the range of 50 to 110 nanoseconds. The oscillator is nominally adjusted for a period of 62.5 nanoseconds, and may be monitored at Test Point E during troubleshooting.

The negative going transitions of SYSCL1 step the two-stage clock counter, TFA and TFB (19G7,8). The system clocks are produced by decoding particular states of the clock counter. The system clocks occur every 250 nanoseconds and have a fixed pulse width of 62.5 nanoseconds, the period of SYSCL1. Figure 2 shows the clock sequencing.

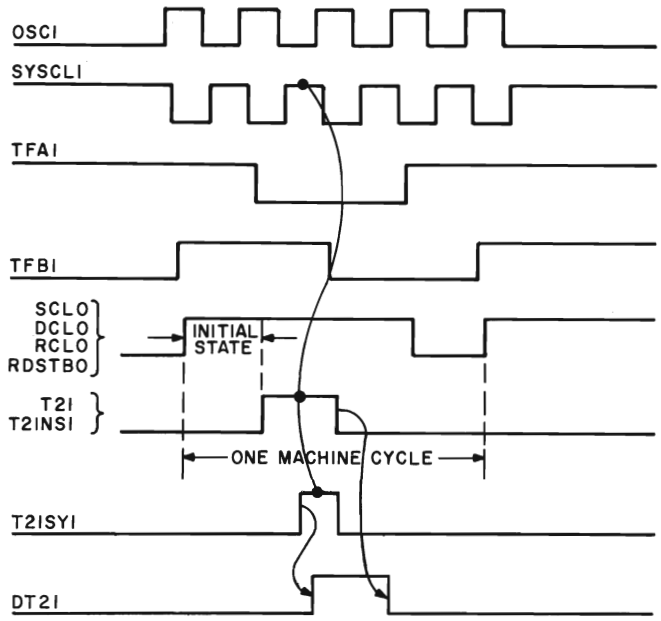


Figure 2. Clock Sequence

The initialize state of the clock counter is TFA and TFB set. This state is not decoded and no clocks are active. On the next negative transition of SYSCL1, TFA resets. This state (TFA reset, TFB set) is decoded to produce T21 and T21NS1 (19K9). T21 is inhibited (skipped) when the signal STPA0 (19J5) is low; T21NS1 is never skipped. T21 and SYSCL1 generate T21SY1 if STPA0 is high. T21SY1 serves as a strobe pulse for CLIR0 and RACLR0 which clear the IR and the ROM address registers respectively. It also is the toggle signal for the Device Stop flip-flop (DST). In addition, T21SY1, together with T21, generates a delayed T21 pulse, DT21, which appears on the ROM Board Back Panel Pin 115-1. DT21 goes high on the leading edge of T21SY1 and goes low on the falling edge of T21. These clock pulses, T21SY1 and DT21, are used when multiple operations have to be completed within one machine cycle. On the next negative transition of SYSCL1, TFB resets. This state (TFA reset, TFB reset) is not decoded and no clocks are active. On the next negative transition of SYSCL1, TFA sets. This state (TFA set, TFB reset) is decoded to produce RDSTB0, RCL0, DCL0, and SCL0.

ROM Data Strobe (RDSTB0)(19L9) is used to strobe data from the ROM into RD. RDSTB0 is skipped whenever any of the following signals are active: STPA0, DST0, STOP0, STPC0, or LRAL0.

ROM Clock (RCL0)(19L9) is used to load the ROM address registers and increment RAL. RCL0 is skipped whenever any of the following signals are active: STPA0, DST0, STOP0, or STPC0.

Destination Clock (DCL0)(19M9) is used primarily to gate data into the Processor registers. DCL0 is skipped whenever any of the following signals are active: STPA0, DST0, LRAL0, or KILDST0.

System Clock (SCL0)(19J9) is an uninhibited clock. The basic machine cycle is defined as the interval between the trailing edges of two consecutive System Clocks (SCL0).

After SCL0, the clock counter returns to the initial state, TFA and TFB set.

It is necessary to prevent the generation of certain timing functions at specific times. To achieve this, a hierarchy of clock inhibits is implemented. This network of clock stops can be divided into three categories:

1. Initialize - All clocks are stopped.

2. Asynchronous to synchronous timing conflicts - This category includes memory oriented operations and Input/Output operations.

3. Extended cycle operations - This category includes Branches and Loads to the RAL which require an extra clock period to allow the new ROM address to be accessed; the Commands Multiply, Divide, and Repeat, and the user instruction access activities carried on in a DO Micro-instruction.

When a memory oriented operation is attempted and memory is not ready, STPA0 goes low, disabling RDSTB0, RCL0, DCL0, and T21.

STPA0 is generated at 4K4 and is located on the 35-388 ROM mother-board. If an attempt is made to unload the MDR (UMDR1)(18C4) when memory data is not available (FMDUA1)(30J4), STPA0 goes low, stopping the Processor until memory data is available. If an attempt is made to load the MDR (LMDR1)(8F8) when the Memory Data Register is being used for the re-write cycle of memory (FMDBY0)(30R4), STPA0 goes low until the memory has finished with the MDR. If an attempt is made to start memory while memory is busy (FPMBY1)(30S8), MSST0 (4K2) goes low, generating STPA0 to stop the Processor until memory becomes un-busy. Note that MSST0 is not active if the Processor is in Phase Zero (P00)(4L1).

When an I/O Load Micro-instruction is performed, DST0 (4A4) goes low, disabling RDSTB0, RCL0, and DCL0. DST0 is generated at 4A4 and is located on the ROM mother-board.

The DST flip-flop (4A4) toggles set on the trailing edge of the first T21SY1 in the Load Micro-instruction (GIO1 true), producing DST0. The DST flip-flop remains set until a Sync is returned from the device (SYNCH1)(4E3) or a false Sync time-out, FSYN0, is generated. An I/O Load Micro-instruction takes a minimum of two system clocks.

The Skip flip-flop (18J8) provides the capability of skipping one clock period while performing a Branch or Load RAL Micro-instruction. The J input to the Skip flip-flop is normally low and goes high when clock cycles are to be skipped. The J input is fed by two NAND gates whose outputs are tied together. During a Branch instruction, if the branch is to be taken, GOBRA0 (18H8) is low, forcing both NAND gate outputs high. During a Load RAL instruction, LDI0 (18F9) is low, forcing one NAND gate output high (18J7). On a DO Micro-instruction, if the Processor is in Phase Zero of a non-RR instruction, SSKIP0 (18K6) is low, forcing the outputs from both NAND gates high. SSKIP0 is generated at 9B8. The high present on the J input to the Skip flip-flop is ANDed with its reset output (18K9) and SSKIP0 to produce LRAL0 (18K9). (LRAL0 is not active if Skip is being used by the Phase Zero DO.)

LRAL0 inhibits RDSTB0 and DCL0 (19L5) for one clock interval, until the Skip flip-flop toggles set. Note that RCL0 has not been inhibited. The S Bus data is toggled into the RAL on the trailing edge of RCL0. On the trailing edge of SCL1, the Skip flip-flop toggles set and LRAL0 goes false. RDSTB0 and DCL0 are re-enabled. On the next system clock, the Skip flip-flop will toggle reset because of a low LDI0 or GOBRA0. If Skip is being used by the Phase Zero DO, KSKIP0 (18J5) goes low when memory becomes un-busy. KSKIP0 is generated at 9F9. The DO Micro-instruction will be described later.

Referring again to Sheet 19, STOP0 (19L5) is active during Phase Zero of a DO Micro-instruction. STOP0 low inhibits RDSTB0 and RCL0.

STOP0 is generated at 9B4. STOP0 is low, if the micro-program is executing a DO Micro-instruction with phase change specified (DRD081) and is currently in Phase Two or Three (PC01) with no interrupts pending (DTEST0), or if in Phase Zero (P01A) and memory data is not yet available (FMDUA1), or if in Phase Zero (P01A) of a non-RR user instruction (RR0) and memory is still busy (FPMBY1). STOP0 prevents the strobing of a new ROM word (RDSTB0 false) or the incrementing of the RAL (RCL0 false) until the Processor is ready to leave Phase Zero.

The KILDST0 signal (19M5) is active if a Command Repeat is attempted when the Counter Register is equal to zero. KILDST0 stops DCL0 so that no Destination Register is loaded and the FLR is not changed. The attempted instruction is effectively skipped. KILDST0 is also low during a Phase Two Abort. See 3.9.2.

The STPC0 signal (19L5) is active during the Commands Multiply, Divide, and Repeat until the Counter Register decrements to one or zero. STPC0 inhibits RCL0 and RDSTB0 so that the same micro-instruction remains in RD for as many machine cycles as required to complete it.

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3.2 Initialize Control

The Initialize Control logic is shown on Sheet 19. This logic provides an orderly system shutdown when Initialize occurs. The following actions take place on initialization:

1. Stop clocks
2. Preset Clock Counter (TFA, TFB)
3. Clear RAH, RAS, RAL
4. Clear RD
5. Clear FLR
6. Clear ALRM
7. Preset CNTR to 16
8. Set Phase Counter to Phase Three
9. Clear BANK and UTILITY flip-flops
10. Clear RUN, CMODE, and RPT flip-flops
11. Reset I/O Control (DST, LINE)
12. Reset Memory Control
13. Provide reset signal to Multiplexor Bus.

NOTE

Do not use I/O Device Number X'05' in your system for anything other than a Loader Storage Unit Controller. Device Number X'05' is reserved for the LSU Controller, a device which is treated specially by the hardware on power-up or initialize sequences, which automatically loads a new PSW and up to 2,048 bytes of main memory. The hardware assumes that if Device Number X'05' exists in a system that it is an LSU and the automatic PSW and memory load sequence occur on power-up. Accordingly, extraordinary results can occur if Device Number '05' is assigned to any other device controller.

The system is initialized as a result of one of the following conditions:

1. Command Power Down (POW)
2. AC input (with optional power fail detector) falls below minimum operating level.

The master reset signal (SCLR0)(19N1) is active when the Initialize Relay K1 (19M2) is de-energized. This happens when the POWDN0 signal (19F1) is active. During normal operating conditions, POWDN0 is high, allowing the Darlington circuit to conduct (Q5 and Q6). As long as the Darlington circuit conducts, the Initialize Relay K1 remains energized.

POWDN0 goes low if the STPSYS flip-flop sets (19J4), or if one of the voltages; +5 volts, +15 volts, -15 volts, or the AC input is lost.

The STPSYS flip-flop (19J4) is direct set if a Command Power Down (POW) is executed, or it toggles set one millisecond after Primary Power Fail (PPF) is detected. PPF0 (19H5) is true one millisecond after the key-operated power switch is turned off (POFF0)(19A4), if the Control Console Initialize switch is depressed (INIT0)(19A4), or if the optional Primary Power Fail Detector determines that the AC voltage is too low (PFDT0)(19C3).

If one of the three above mentioned items occur, the one millisecond delay at 19G2 is set. The negative transition of the zero (0) side toggles the Early Power Fail flip-flop set (EPF)(17S7). If PSW02 is set, Alarm Register Bit-15 sets, generating a Machine Malfunction Interrupt (MALF1). As soon as ALRM15 flip-flop sets, the EPF flip-flop is cleared. The Processor tests for MALF between the execution of each user instruction. In response to the Machine Malfunction Interrupt, the user has an opportunity to do any necessary system resetting.

After the initial one millisecond delay, the negative transition of the one (1) side of the EPF delay toggles the Primary Power Fail flip-flop set (PPF)(19J3). This starts the other one millisecond delay at 19G4. If this delay times out before the micro-program executes a Command Power Down, the STPSYS flip-flop toggles set (19J4). The Processor tests for PPF between the execution of each user instruction. When PPF is detected, the micro-program stores the PSW, LOC, and General Registers in core and executes a Command Power Down (POW), setting the STPSYS flip-flop and clearing the second one-millisecond delay. When STPSYS1 goes high, the POWDN0 lead goes low, de-energizing the Initialize Relay K1. STPSYS0 active causes CLKSTP1 (19N5) to go high. The GO flip-flop toggles reset (19D9), stopping the system clocks.

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The second instance when POWDN0 goes low is when one of the voltages is lost. If the N15 (-15VDC) supply voltage is lost (19J1), the output from the NAND gate at 19J1 goes low. If the P15 (+15VDC) supply voltage is lost (19D1), the POWDN0 lead becomes effectively open as Transistor Q4 is normally off. If the P5 (+5VDC) is lost, the collector supply for the Darlington circuit is removed (19L2), causing the Initialize Relay K1 to de-energize. If the AC input is lost, the POWDN0 lead is also forced low. The AC input is sampled from the secondary of a 12VAC transformer and rectified. The pulsating DC voltage is applied to Potentiometer R60 (19B1). The potential selected by the potentiometer is applied to the optional Power Fail Detector.

Initially, Transistors Q2, Q3, and Q4 are off and Transistor Q1 is conducting. With Transistor Q1 conducting, a high enough potential on the base of Q4 keeps Q4 cut off, and applies about +6 volts to the emitter of Q2. The potential from Potentiometer R60 (approximately 8 volts) is felt on the base of Q2. If the AC input is lost, or fluctuates enough, the potential on the base of Q2 becomes more negative and Q2 conducts.

When Q2 conducts, it places a positive potential on the base of Q3, turning Q3 on. This causes the potential on the emitter of Q1 (by way of Q2) to become less positive, turning Q1 off. When Q3 conducts, its collector goes to ground, generating the low signal, PFDT0 (19D3).

When Transistor Q1 turns off, the positive potential is removed from the base of Q4. Transistor Q4 conducts, grounding the POWDN0 lead, turning the Darlington circuit off, and de-energizing the Initialize Relay K1. (The Initialize Relay K1, which is a dry reed relay with Single Pole Double Throw contacts, is shown de-energized.) When the relay de-energizes, the SCLR0 contact is grounded. This metallic ground is distributed to the memory and I/O boards for initialize control. SCLR0 also holds CLKSTP1 active, keeping the clocks off.

SCLR0 is inverted through the gate at 19N2. The output SCLR1A rises to +5 volts and generates SCLR0A (19H5) and SCLR0B (19R5) for use on the I/O board. SCLR1A (19R1) is also distributed on the back panel for use by the other Processor boards.

SCLR0A holds CLKSTP1 active and also clears the STPSYS flip-flop. Resetting the STPSYS flip-flop removes the ground from the POWDN0 line. The two 33mfd capacitors (C1 and C2) charge slowly (19K3). When the threshold of the input Transistor Q5 of the Darlington circuit is reached, the circuit conducts and the Initialize Relay K1 is energized.

The SCLR0 contact opens and SCLR1A goes to ground. SCLR0B goes high, removing the direct set signal on the Timer flip-flops (TFA and TFB) and the direct clear signal on the GO flip-flop. SCLR0A goes high allowing CLKSTP1 and the K input to the GO flip-flop to go low. The J input (CLKSTP0) is delayed by the 2.2mfd capacitor (19R5) to ensure that the clocks do not start until all initialize activity is completed.

In the case where Initialize is caused by a failure of P5, N15, P15, or the AC supply, the Initialize Relay K1 de-energizes and remains in that state until the fault is corrected.

3.3 Read-Only-Memory

The Read-Only-Memory (ROM) is a high-speed, solid-state, non-destructive memory used to hold the micro-program. The ROM is organized into pages of 256 16-bit words. Each page of ROM contains four integrated circuit (IC) packages arranged such that each integrated circuit holds four-bits of every word on the associated page.

The Model 70 micro-program is complete in six ROM pages, 24 ROM integrated circuits. Three additional ROM integrated circuits comprise the Decoder ROM (DROM). Space is provided on the ROM mother-board for an additional two pages of ROM.

Each ROM integrated circuit has two enable leads. Both enables have to be low before a read-out is obtained. If the enables are false, the four data output leads are high. Address decoding is done internal to the IC.

3.3.1 ROM Address Lower (RAL). The ROM Address Lower Register (RAL) is an eight-bit register that selects one of 256 addresses in a Read-Only-Memory page. RAL is shown of sheet 5.

During the performance of the major portion of the micro-program, micro-instructions are selected from successive locations in the ROM. RAL is an up-counter. The RAL is incremented as each new micro-instruction is read from ROM. During a Branch Micro-instruction with the specified condition true, or if the RAL is specified as the Destination Register, the RAL increment signal is disabled and the new address is loaded from the S Bus.

RAL is direct cleared by System Clear (SCLR0)(5A1) when the system is initialized, or conditionally on a DO Micro-instruction by RACLR0 (5A1). The ROM Clock (RCL0)(5K1) is used to increment RAL or to gate the S Bus data into the RAL. If a Branch or a Load RAL instruction is performed, LRAL0 (5R2) is low and LRAL1 (5N4) is high. LRAL1 is NANDed with each bit of the S Bus (8:15) to set up the J and K inputs to each RAL flip-flop. LRAL0 low causes the two 19-040 four-bit carry networks to pass RCL1 to the toggles of RAL 09 through 14. RCL1 is always present on RAL15 and is gated to RAL08 by LRAL1. On the trailing edge of RCL0, the S Bus data is copied into RAL.

When the Processor is not executing a Branch or a Load RAL, LRAL0 is high and LRAL1 is low. LRAL1 low causes both the J and K inputs to each RAL flip-flop to be high. If a flip-flop receives a toggle, it will complement. A flip-flop is given a toggle pulse if all previous flip-flops are set. RAL15 will complement on the trailing edge of every RCL0. The 19-040 four-bit carry network (5R7) toggles RAL14 if RAL15 is set. RAL13 toggles if RAL14 and RAL15 are both set, etc. The signal PF0, low if RAL 12 through 15 are set, enables the second 19-040 four-bit carry network (5M7) which supplies the toggles for RAL09, RAL10, and RAL11. The toggle for RAL08 is generated separately if the PF0 lead from the 19-040 four-bit carry network (5M7) is low, indicating that RAL09 through 15 are all set.

When the DO Micro-instruction generates a new ROM address, the ROM Address Registers are first cleared, then the new address is loaded. The DO instruction generates RACLR0 (9B9), a 30 nanosecond pulse, T21SY1. RACLR0 clears RAH, RAS, and RAL. DT21, which extends beyond the falling edge of T21SY1, is applied to the direct set input of the appropriate ROM Address Register bits.

3.3.2 ROM Address Higher (RAH). The ROM Address Higher Register (RAH) is shown on Sheet 5. RAH is a four-bit extension of the RAL which increases the ROM addressing capability to 4096 locations. RAH is independent of the RAL from both the programming and hardware viewpoint. When RAL is incremented from its highest value (hexadecimal 'FF'), it recycles to zero, but no carry is propagated into RAH. Consequently, the RAH must be loaded independently each time a Branch or Load RAL selects a different page.

A new page address is loaded into RAH at the trailing edge of RCL0 when the RAH is specified as the Destination Register (LRAH0 low)(5K1). RAH is cleared by SCLR0 (5A1) on Initialize or by RACLR0 on a DO Micro-instruction. Both the RAH and RAS receive the same page number when the DO instruction generates a new ROM address.

3.3.3 ROM Address Slave (RAS). The ROM Address Slave Register (RAS) is slaved to the four-bit RAH. The outputs from RAS select the page of ROM to be accessed.

The contents of RAH are loaded into RAS every time RAL is loaded from the S Bus. This allows the proper page number to be established in RAH in advance of a Branch or Load RAL.

The RAS is cleared by SCLR0 on Initialize or by the RACLR0 signal on a DO instruction. Note that RAH04 and RAS04 are cleared separately from the remaining bits of RAH, RAS, and RAL. Bit-4 of RAH and RAS is unconditionally held clear when PSW Bit-7 is reset. The only time that ROM Pages 8 and above can be specified is when PSW Bit-7 is set. Since Pages 8 and above physically do not exist, the illegal condition will be forced upon access. The connection between ROM address Bit-4 and PSW07 will be explained later in Section 3.4.

3.3.4 ROM Addressing Logic. Pages 0 through 3 of the ROM are shown on Sheet 6 and Pages 4 through 7 are shown on Sheet 7. One enable lead to the 16 ROM integrated circuits on Sheet 6 is RAH051. If RAH specifies Page 0, 1, 2, or 3, RAH051 is low, enabling the 16 devices on Sheet 6. If RAH specifies Page 4, 5, 6, or 7, RAH050 is low, enabling the 16 devices on Sheet 7. One ROM page (four devices) out of the four pages enabled by RAH05 is selected by decoding RAH06 and RAH07. The signal EN000 is low if Page 0 or 4 is selected. EN010 is low if Page 1 or 5 is selected. Page 2 or 6 selected causes EN100 to go low. Page 3 or 7 causes EN110 to go low. The combination of an ENXX0 lead and RAH05X causes 4 ROM integrated circuits, out of 32 possible, to be enabled. The enabled devices each gate four-bits of data onto the high active SRDXX1 leads.

The address decoding of a word within a page is done internal to the ROM integrated circuits. The address selected is specified in RAL. Page 0, 1, 2, and 3 devices are addressed by the one (1) side of the RAL flip-flops and Page 4, 5, 6, and 7 devices are addressed by the zero (0) side of the RAL flip-flops. This is done for fan-out reasons.

The SRDXX1 leads are tied to the J inputs of the ROM Data Register (RD) flip-flops and inverted onto the K inputs (Sheet 8). At clock time, the ROM data is toggled into RD.

3.3.5 ROM Data Register (RD). The ROM Data Register (RD) is a 16-bit register shown on Sheet 8. The RD can be thought of as the micro instruction register. Each bit of the RD has a dual-rail input from the ROM array. Each micro-instruction read from ROM is clocked into RD, where it remains while the instruction is executed.

Bits 0:3 of RD hold the Op-Code of the micro-instruction being executed. If the instruction is not a command, RD Bit-3 set means the instruction is Immediate. The data to be used as the first operand is contained in Bits 8 through 15 of the instruction. During an Immediate instruction, RD 8:15 are gated onto the B Bus Bits 8:15.

Bits 4:7 of RD are decoded as the Destination Register address for all micro-instructions except DO, Command, Test, and Branch. This identifies the register that will contain the result upon completion of the micro-instruction. If the micro-instruction is a DO, Command, or Test, Bits 4:15 of RD are the function code. If the instruction is a Branch, RD 4:7 defines the condition that the Processor will branch on.

Bits 8:11 of RD are decoded as the Source Register address for micro-instructions in the Register-to-Register format. The Source Register contains the first operand for the micro-operation.

Bits 12:15 of RD make up the Extended operation field for Register-to-Register Micro-instructions. The Extended field controls shifting, flags, I/O operations, or whether to enable the A Register input to the ALU.

The RD is cleared by SCLR0 on Initialize or when a Privileged instruction is addressed and the Processor has PSW Bit-7 enabled.

3.4 Decoder Read-Only-Memory

The Decoder Read-Only-Memory (DROM) consists of the three ROM integrated circuits shown on Sheet 4. Each IC contains 256 four-bit words. The Read-Only-Memories are addressed in parallel by Bits 0:7 from the Instruction Register (IR). The high active DROM read-out is gated onto the SRAXX0 leads by the GDROMA and GDROMB signal (4C8) that occurs at DT21 before the Processor enters Phase Two. The ROM Address Registers are direct cleared at T21SY1. The DROM data is the starting address in ROM of a Phase Two micro-subroutine.

DROM read-out Bit-4 is active only on the privileged user instructions. A Privileged instruction may only be executed if PSW Bit-7 is reset. PSW071 (5A1) on the DC clear input to RAH04 (5C3) keeps RAH04 from setting if PSW07 is reset. If PSW07 is set, RAH04 is allowed to set from the DROM output. If a Privileged instruction is in the IR, RAH04 sets and the illegal address condition exists. The gates at 8A2 will cause the RD to clear on the next RDSTB0 and the illegal condition will occur. Privileged instructions that are attempted when PSW07 is set, are treated as illegal.

3.5 Processor Registers

The Processor executes micro-instructions received from the ROM. The majority of micro-instructions move data from one register to another and modify it in the ALU. Most of the Processor registers are 16-bit registers. Some of these registers perform special functions, but the majority are general purpose. Data is transferred between registers and other system elements by way of the 16-bit B and S Buses in the Processor. Each register is described in the following paragraphs.

3.5.1 Flag Register (FLR). The Flag Register (FLR)(Sheet 17) is a four-bit register located on the 35-390 I/O mother-board. The FLR is direct cleared by the SCLR0A signal (17D5). The FLR is loaded from the S bus when the FLR (address '4') or the PSW (address '2') is specified as the destination. Destination address '4' causes LFLR0 (17S1) to be active. Destination address '2' causes LPSW1 to be active (17S1). LFLR0 is generated on the 35-388 ROM mother-board at 8D9. LPSW1 is inverted and NANDed with LFLR0, producing LDFLR1 (17K2). LDFLR1 is NANDed with S Bus Bits 12 through 15. If any bit of the S Bus is true, SFLRXX0 on the K input to the corresponding bit in the FLR goes low and the J input goes high, allowing the corresponding flip-flop to toggle set on the trailing edge of the next Destination Clock (DCL0)(17A1). If the S Bus bit is false, the K input is high and the J input is low, and the flip-flop toggles reset.

Since the FLR is used to hold flags indicative of the result of micro-instructions, there are instances when individual bits will be changed independently. To facilitate this, different toggle leads are developed for the different bits.

LDFLR0 is inverted and ANDed with the CLR0 signal (17R1) producing LDCLR0 (17M4). CLR0 is active, when specified, during a DO Micro-instruction. CLR0 is generated on the ROM board at 9N4. If the Processor is executing a DO Micro-instruction, D1 is high (8D5). If the Processor is not in Phase Zero (P00) and no memory clock stop is in effect (MSST0), CLR0 is allowed to go low. MSST0 assures that CLR0 only occurs during the last clock interval of a DO Micro-instruction. CLR0 is forced low when the new phase is to be Phase Three (GTP30). LDCLR0 allows all the FLR bits to change.

The toggle lead for FLR Bits 14 and 15 is developed by the two NAND gates collector AND tied at 17R4. The input to one gate is the Destination Clock (DCL0) and one input to the other gate is LDCLR0. The toggle for Bits 12 and 13 is the ungated DCL1. The gating for these bits is done individually on the J and K inputs.

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FLR Bit-12 is used as the Carry Save flip-flop (C)(17E5). FLR12 is set or reset to reflect whether or not a carry or borrow resulted from an Add or Subtract Micro-instruction, or to reflect the state of the bit shifted out during a Load Micro-instruction. FLR12 is allowed to change state when LDCLR0, SVSC0, or SVAC0 is active. If none of the gating leads are active, the J and K inputs are held at ground.

SVSC0 is generated in two places with an OR tie across the back panel. The first source is on the ROM board at 8S9. SVSC0 goes low if the Processor is executing a Load Micro-instruction (LOAD1) other than I/O (LDIO0·UDIO0) and RD Bit-15 is set (RD151), specifying Carry Out. The second source of SVSC0 is on the ALU board at 13A4. SVSC0 is active during a Command Shift Left (CSL0) or a Command Shift Right (CSR0) other than during a Multiply (MPY0) if RD Bit-15 is set (RD151), specifying Carry Out.

SVAC0 is also generated in two places with an OR tie across the back panel. The first source is on the ROM board at 8S9. SVAC0 is active during a non-immediate (RD030) AND, OR, Exclusive OR, Add, or Subtract Micro-instruction (RD001+RD011·RD021) if RD Bit-15 is set (RD151), specifying Carry Out. The second source of SVAC0 is on the ALU board at 13B4. SVAC0 is low during a Command Multiply Micro-instruction (MPY1) if RD15 is set (RD151), specifying Carry Out.

FLR12 is set when SFLR120 is low. SFLR120 is generated by four NAND gates collector OR tied. The input to the first NAND gate is SHOT1 (17C1), generated on the ALU board (13C9). SHOT1 goes high when the Processor is executing a Shift Right (SHR1) and B Bus Bit-15 is active (B150), or a Shift Left (SHL1) and B Bus Bit-0 is active (B000), or a Command Shift Right (CSR1) other than on Multiply (MPY0) and Shift Register Lower Bit-15 is set (SRL151), or Command Shift Left (CSL1) and Shift Register Higher Bit-0 is set (SRH001).

The second NAND gate is enabled by SVAC1 (17D3). The Carry Output from the ALU (CSV1) is Exclusive ORed with Subtract (SUB1) and applied as the second input. The third input to the NAND gate at 17D3 is the Exclusive-NOR of RD000 and RD010 and is high when RD000 and RD010 are alike. The only time that RD000 and RD010 are alike when SVAC1 is high, is during an Add, Subtract, or Command Micro-instruction. The meaning of CSV1 from the ALU differs depending on whether an Add or Subtract Micro-instruction is performed. The Exclusive OR of CSV1 and SUB1 inverts the ALU Carry on a Subtract Micro-instruction.

The third NAND gate (17C2), enabled by LDFLR1, has a low output when S Bus Bit-12 (S121) is active. The fourth NAND gate is the master enable for the K input to FLR12. SFLR120 is inverted and the J input is allowed to go high. FLR12 toggles set on the trailing edge of the next Destination Clock (DCL1).

FLR Bit-13 serves as the Overflow flag (V) for Add and Subtract operations. FLR13 is allowed to change state when LDCLR0 or STFL0 is active. If neither of the gating leads are active, the J and K inputs are held at ground.

STFL0 (17F1) is generated on the ROM board at 8R9. STFL0 goes low if the Processor is doing a non-immediate (RD030) Add or Subtract Micro-instruction (RD001·RD011) and RD Bit-13 is set (RD131), specifying set flags.

FLR13 is set when SFLR130 is low. SFLR130 is generated by three NAND gates collector OR tied. The first NAND gate (17H3) is enabled by LDCLR0. The second input is the Exclusive OR of S000 and GB000. The third input is DIFF1, the Exclusive OR of GB000 and, the Exclusive OR of GA001 and SUB1. The NAND gate at 17H3 is low when the overflow condition exists. The overflow indication is created after the ALU has produced the Sum or Difference. Overflow occurs on an Add with like signs or a Subtract with different signs when the resulting sign is different from the sign of the first operand on the B Bus.

The second NAND gate at 17H2, enabled by LDFLR1, has a low output when S Bus Bit-13 (S131) is active. The third NAND gate (17F3) is the master enable for the K input to FLR13. SFLR130 is inverted and the J input is allowed to go high. FLR13 toggles set on the trailing edge of the next DCL1.

FLR13 can also be direct set by SV0. SV0 goes low when the False Sync flip-flop is set (4E3). The False Sync flip-flop is set if the Processor does not receive a return Sync from a device controller within 13 to 15 microseconds from the time the I/O control line is activated to start an I/O operation.

FLR14 and FLR15 serve as the Greater than and Less than flags respectively. FLR14 is set by SFLR140 if the data manipulated on the S Bus is greater than zero or the result of a Test Micro-instruction is true. FLR15 is set by SFLR150 if the data manipulated on the S Bus is less than zero or if the result of a Test Micro-instruction is false.

SFLR140 is generated by three NAND gates collector OR tied. The first NAND gate (17J2) is used to load FLR14 from S Bus Bit-14. The second NAND gate (17J2) is enabled by STF1. The second input is CTF1 and the third input, S000, is high when the S Bus is not negative.

The gating leads STF0 and STF1 are active during a non-immediate AND, OR, Exclusive OR, Add, or Subtract Micro-instruction if RD Bit-13 is set, specifying set flags (8R9).

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The Change Test Flags signal (CTF1)(17J1) is active if any bit of the S Bus is active, or if the G or L flag is set. If either the G or L flag is set, FRNS1 is low (17N5). This signal is NANDed, on the ALU board, with the zero indicating outputs from the four 4-bit ALUs at 14S8. If S Bus Bits 0:3 are zero, S0031 is high. If S Bus Bits 4:7 are zero, S0471 is high. If S Bus Bits 8:11 are zero, S8111 is high. If S Bus Bits 12:15 are zero, S1251 is high. The output from the NAND gate at 14S9 (CTF1) returns to the I/O board to enable changing the G and L flags.

The third NAND gate (17K2) is active during a Test Micro-instruction (CTEST1) if the result of the test is true (TTEST1).

The TTEST0 signal (17K1) is generated on Sheet 18 as the collector OR tie of the inverted outputs of the three 19-026 four-to-one multiplexors. TTEST0 (18H5) is low if a testable function is true and the corresponding mask bit in the RD is set. The testable functions and the associated RD bits are listed below.

TESTABLE FUNCTION		
RD BIT	MNEMONIC	MEANING
4	FST1	Fast I/O Interrupt
5	ATN1 · PSW011	I/O Attention and PSW Bit-1 set
6	ARST1	Automatic Restart
7	CATN1	Console Attention
8	SNGL1	Console Single Mode
9	UT1	Utility flip-flop set
10	MALF1	Machine Malfunction
11	PPF1	Primary Power Fail
12	DC1	Data Channel Request
13	DRD1	Data Channel Read
14	MSK1	Mask
15	OP1	Operation Length

The logic to generate SFLR150 is similar to that that generates SFLR140. Except when the FLR is being loaded from the S Bus or cleared on a DO Micro-instruction (CLR0), SFLR140 and SFLR150 are complementary.

The toggle for FLR14 and 15 is generated at 17N4 as the collector AND tie of DCL0 and LDCLR0, STF0, or CTEST0.

3.5.2 Program Status Word (PSW). The Program Status Word (PSW) is a 16-bit register used to define the system status relative to the user program being executed. The Status field (PSW 0:11) is located on the 35-387 Memory Control mother-board and is shown on Sheet 29. The Condition Code field (PSW 12:15) is located on the 35-390 I/O mother-board and is shown on Sheet 17.

PSW 0:11 is loaded from S Bus Bits 0:11 when the PSW is specified as the destination (LPSW1)(29C1). LPSW1 is ANDed with the Destination Clock (DCL1)(29C1) at the gate (29C2) and applied to the clock input of the three 19-030 four-bit shift registers (A48-A50). Pin 06 of each 19-030 shift register is tied to P5 to establish the Load Mode rather than Shift Right Mode.

PSW Bits 12:15 are contained in the 19-017 quad latch (17B-G9). The Condition Code Register may be loaded from the Flag Register or from the Alarm Register. The clock input to the Condition Code latch is high at System Clock time (SCL0)(17B5) when either LCC0 or JACC0 is active (17C5). LCC0 is generated at 9M4 and is low on a DO Micro-instruction (D1) if the Processor is in Phase Three (P31) and RD Bit-12 is set, specifying copy alarm flags to the Condition Code. The data inputs to the quad latch are LCC1 and FLR 12:15, or JACC1 and ALRM 13:15.

All 16 PSW bits are applied to the eight 19-038 dual four-to-one line multiplexors on Sheet 29 for gating onto the B Bus. When the PSW is specified as the Source Register (address '4'), the signal USTRB0 (29A4) goes low enabling all the 19-038 multiplexors. USTRB0 is generated at 18C5 and is active when the Source Register address is hexadecimal 4, 5, 9, or A. RD Bits 9 and 11 are decoded internal to the multiplexors to select which of the four input registers are gated out to the B Bus.

PSW Bit-1 is the I/O interrupt enable. PSW011 is ANDed with ATN1 at 18J3 for the Test Micro-instruction and at 18N3 for generating an interrupt. PSW Bit-2 set allows the Alarm Register Bits 13:15 to be set (17K6). PSW Bit-4 is available at Pin 226-0 on the I/O board back panel to enable detection of the Fast I/O interrupt. (For the regular Model 70, this pin is tied to ground instead of PSW041.) PSW Bit-7 controls the supervisor/user mode of the Model 70 Processor. If PSW07 is set, detection of Privileged instructions is allowed and the optional Memory Protect feature is enabled. PSW07 set allows RAH04 to be set from the DROM (5C2). Privileged instructions are flagged in the DROM by having Bit-4 set. If RAH04 sets, the non-existent ROM address forces the Illegal instruction trap. No hardware significance is attached to the remaining PSW bits.

3.5.3 Alarm Register (ALRM). The three-bit Alarm Register is located on the 35-390 I/O mother-board and is shown on Sheet 17. PSW Bit-2 (17K6) enables setting any bit in the Alarm Register.

ALRM15 is set on the occurrence of Early Power Fail (EPF)(17S6). Refer to 3.2. ALRM14 is set if a Memory Parity Failure occurs (PFF1)(17M6) during Phase Zero or Phase One (PC00). ALRM13 is set if a parity failure occurs during Phase Two or Phase Three (PC01)(17K6). If any bit in the Alarm Register sets, Machine Malfunction goes high (MALF1)(17S9).

The Alarm Register bits can be copied into the Condition Code of the PSW on a DO Micro-instruction, JACC1 high. This is done during the PSW swap routine for Machine Malfunction Interrupt so that the user is informed of the nature of the interrupt.

The Alarm Register is cleared by SCLR0 on Initialize or it toggles clear at SCL1 time when JACC1 is high.

3.5.4 Counter Register (CTR). The Counter Register (CTR) is shown on Sheet 27. It is used to count the number of repetitions of a single micro-instruction when the Processor is executing a Command Repeat, Multiply, or Divide. The Counter is also a testable item for the Branch Micro-instruction.

The five-bit decrementing CTR is loaded from S Bus Bits 11:15 by LDCTR0 (27B1). LDCTR0 is generated at 8C9 and is low when the Destination address is hexadecimal 'C'. LDCTR0 is inverted and NANDed with DCL1 (27E3), producing the low active load pulse for the 19-035 four-bit counter at 27F5. The S Bus Bits 12:15 are toggled into CTR 12:15 at the trailing edge of the load pulse. CTR Bit-11 is maintained in a separate JK flip-flop (27B5) and is toggled by the AND of LDCTR1 and DCL1 (17A3). The J and K inputs to CTR11 track S Bus Bit-11 when DECTR0 is false (27C1).

The DECTR0 lead goes low to allow the CTR to decrement on the trailing edge of DCL1. DECTR0 is generated in two places with an OR tie across the back panel. The first place is on the 35-390 I/O board at 18E9. DECTR0 goes low if the Processor is executing a Branch on Counter Micro-instruction. Op-Code '3' causes BRA1 (18H8) to go high. If the CTR is the specified condition, RD 04:07 are reset and LD01 (18D7) is high. The second place DECTR0 is generated, is on the ALU board at 13F9. DECTR0 is low if the CTR is not zero (CEMT0 false)(13F7) and the Processor is executing a Command Multiply (MPY0), or a Divide (DIV0) Micro-instruction, or if the Counter Mode flip-flop (CMODE) is set after a Command Repeat (13G8). For these instructions, DECTR0 remains active until the counter decrements to zero.

DECTR0 is inverted and ANDed with DCL1 (27A1) to produce the low active decrement pulse to the 19-035 four-bit counter. If the low four-bits are zero when the decrement pulse occurs, a carry pulse is produced on Pin 13 of the I.C. and the CTR 12:15 wraps to a count of 'F'. The carry pulse complements CTR Bit-11.

Two states of the CTR are decoded. Counter equal to zero causes CEMT0 at 27C9 to go low. Counter equal to one causes CTONE0 at 27C9 to go low. These signals are used by the Branch on Counter and the Counter mode logic.

The Counter is preset to a count of 16 by SCLR0 (27C1) on initialize, or CLR1 and SCL1 (27D2) on a DO Micro-instruction.

3.5.5 Register Stack. The register stack shown on Sheet 11 is located on the 35-389 ALU mother-board. The register stack consists of 20, general purpose, 16-bit registers which can be specified as Source and Destination Registers for micro-instructions. These registers can be loaded from the S Bus and unloaded to the B Bus.

The register stack consists of 20, 19-041 four-bit by four-word register files. Each IC has a read enable and two read select lines, and a write enable and two write select lines. This allows a stack register to be both the source and destination in the same micro-instruction. The read enable level selects one of five sets of four ICs. The micro-register stack (MR0, MR1, MR2 and LOC) is selected by RMS0 (11A2). The RMS0 signal is generated at 10D4 and is active when the Source Register address is hexadecimal 0, 1, 2, or 3, or when the DO Micro-instruction forces the LOC to be both the source and destination (FRCLOC0)(9J4).

General Registers 0 through 3 are selected by the signal GR00 (11C1). General Registers 4 through 7 are selected by GR10 (11G1). General Registers 8 through 11 by GR20 (11J1) and General Registers 12 through 15 by GR30 (11M1). The General Registers are addressed by the YD or YS field of the Instruction Register (IR). The micro-program accesses a General Register by specifying the field of the IR that contains the register's address. If the Source Register is YS (hexadecimal D), or if a DO Micro-instruction in Phase Zero has generated Load AR from YS (LARYS0)(9C4), RYS1 is high (10B6). RYS1 is NANDed with the four decoded states of IR Bits 12 and 13 (10M1) to activate the appropriate GRX0 lead on Sheet 10. If the Source Register is YD or YDP1 (hexadecimal E or F), RYD1 is high (10A6). RYD1 is NANDed with the four decoded states of IR08 and 09 (10L1) to activate the GRX0 leads.

Given that RMS0 or one of the GRX0 leads is active, selection of the particular register is done internal to the 19-041 by decoding the state of the two read select lines.

The micro-registers are selected by the leads RMA1 and RMB1 (10F3). These lines track RD Bits 10 and 11 respectively. Both lines are forced high by FRCLOC0 (10F1).

The General Registers are selected by the leads RA1 (10H9) and RB1 (10F9). RB1 tracks IR Bits 10 or 14 depending on whether YD or YS is the source. If YDP1 is the source, RA1 is forced high so that an odd address register is selected (11C1).

The logic for writing into the register stack is similar to that for reading. The significant difference is that the write enable line is a pulse rather than a level. This pulse occurs at SYSCL1 time during DCL1 (10H3). The write pulse is about 30 nanoseconds wide. The minimum pulse width necessary to satisy the 19-041 is 25 nanoseconds. The maximum pulse width depends on the delay through the ALU and is approximately 50 nanoseconds. A wider write pulse mutilates data in a register if the same register is specified as the source and destination.

3.5.6 Shift Registers (SRH and SRL). The two 16-bit Shift Registers, SRH and SRL, are located on the 35-389 ALU mother-board and are shown on Sheet 15. Either shift register may be loaded from the S Bus and unloaded to the B Bus. The SRH and SRL consist of four 19-048, eight-bit, shift register packs, that function as a single 32-bit register when used by the Command Shift Left, Shift Right, Multiply, or Divide Micro-instructions.

The shift register devices can load, shift left, or shift right, depending on the state of the two mode control leads on Pins 01 and 23 of the devices. The logic that generates the mode control leads is shown on Sheet 15.

SRH is loaded from the S Bus when the Destination address is hexadecimal 6. SRH is forced to be a destination during a Command Multiply or during a Command Divide Micro-instruction when the ALU Carry is active (CSV1)(15R1). When SRH is the destination, HDEST0 is low (15L1). HDEST0 causes both SRH mode control leads, SRHM01 and SRHM11 (15J4), to go high, establishing the load function. On the trailing edge of DCL0 (15S1), the S Bus data is copied into SRH. When the Processor is executing a Command Multiply Micro-instruction, MPY0 is low (15L1), forcing SRHM01 and SRHM11 high. During a Command Divide Micro-instruction (15L1), DIV0 is low, forcing SRHM11 high. If CSV1 is high (15R1), SRHM01 is also forced high, establishing the Load Mode. If CSV1 is false, SRHM01 is low and SRH is in the Shift Left Mode.

The data in SRH is shifted left one bit position when SRHM01 is high and SRHM11 is low. This condition is established as mentioned previously for the Divide Micro-instruction, or by CSL0 (15L1) during a Command Shift Left. Anytime SRH is shifted left, SRL Bit-0 shifts into SRH Bit-15. Bits shifted out of SRH00 may be saved in the Carry flag (FLR12) if RD Bit-15 is set, specifying Carry Out (15A3).

The data in SRH is shifted right one bit position when SRHM01 is low and SRHM11 is high. This condition occurs only during a Command Shift Right Micro-instruction (CSR0)(15M1). If RD Bit-14 is set, specifying Carry In, the state of the Carry flag (FLR12) is shifted into SRH00 (15A3).

SRL is loaded from the S Bus when the Destination address is hexadecimal 7. LSRL0 (15N1) goes low forcing SRLM01 and SRLM11 high, establishing the Load Mode.

The data in SRL is shifted left one bit position when SRLM01 is high and SRLM11 is low. This condition occurs during a Command Shift Left (CSL0) or a Command Divide Micro-instruction (DIV0). If RD Bit-14 is set, the state of the Carry flag (FLR12) or, if Divide, the static ALU Carry (CSV1), is shifted into SRL15 (15S9).

The data is SRL is shifted right when SRLM01 is low and SRLM11 is high. This condition occurs during a Command Shift Right (CSR0) or a Command Multiply Micro-instruction (MPY0). The state of SRH15 is shifted into SRL00. If RD Bit-15 is set, specifying Carry Out, the bit shifted from SRL15 is saved in FLR12 (15A3) except during Multiply (MPY0).

The gates that unload SRH and SRL to the B Bus are shown on Sheet 16. The SRH is unloaded when the Source address is hexadecimal 6 (USRH0)(16A1) or when the Processor is executing a Command Multiply or Divide (MD0)(16A1). The SRL is unloaded when the Source address is hexadecimal 7 (USRL1)(16A3).

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3.5.7 Instruction Register (IR). The Instruction Register (IR) is located on the 35-387 Memory Control mother-board and is shown on Sheet 28. The IR holds the user's instruction word during emulated execution. The IR may be loaded from the S Bus when it is specified as the Destination. It is also loaded directly from memory upon instruction access Phase Zero. The IR may be unloaded to the B Bus.

During Phase Zero (P01), the Memory Strobe Bus (MS 0:15) is gated to the direct set inputs of the IR flip-flops by GMSIR1 (28B3). IR was previously direct cleared when Phase Zero was entered, CLRIR0 from 28A1.

When the IR is specified as the Destination (hexadecimal 9), LIR0 goes low (28S1). LIR0 is used to develop the toggle inputs (TIR0)(28S3) to the IR flip-flops.

Bits 0:7 of the IR are applied, as the address, to the Decoder Read-Only-Memory and to the instruction class decoders on Sheet 4. IR Bits 8:15 are used to select the General Registers (Sheet 10). In addition, IR Bits 8:11 are ANDed with PSW Bits 12:15 at 29S7 to generate the testable MSK function.

All 16 IR bits are applied to the eight 19-038 dual four-to-one line multiplexors (Sheet 29) for gating onto the B Bus. When the IR is specified as the Source Register (address '9'), USTRB0 goes low (29A4). RD Bits 9 and 11 are decoded internal to the multiplexors to select the IR. When the Source Register address is 'C', UIR40 goes low (18E5). UIR0 is inverted and ANDed with IR Bits 8:11 (Sheet 28) to develop the B Bus Bits 12:15. The remaining B Bus bits stay false.

3.5.8 Arithmetic Register (AR). The Arithmetic Register (AR), located on the 35-389 ALU mother-board, is shown on Sheet 12. The AR is used to hold the second operand of the Add, Subtract, OR, AND, or Exclusive OR Micro-instruction. The AR may be loaded from the S Bus and unloaded to the Arithmetic Logic Unit (ALU).

When the AR is specified as the Destination (hexadecimal 8), LAR1 goes high (12A1). LAR1 is used to develop the toggle inputs to the AR flip-flops.

The set outputs from the AR are NANDed with the ULAR1 signal to develop the GA leads (GA000:150) as gated inputs to the ALU. ULAR1 is generated at 13N5. For fan-out reasons, it is developed twice. One input to each AND gate at 13N5 is NA0 (13R4). The other input comes from the 19-026 four-wide AND/OR pack at 13N3.

NA0 is only low during a non-immediate (RD030) Micro-instruction that has Bit-12 set, specifying the No AR option. The 19-026 pack produces a high output whenever one of the following conditions is met:

1. The Processor is executing an AND, Exclusive OR, Add or Subtract Micro-instruction (RD001).
2. The Processor is executing an OR Micro-instruction (RD011·RD021).
3. The Processor is executing a Command Divide Micro-instruction (RD010·RD020·RD031·RD061·RD081)
4. The Processor is executing a Command Multiply Micro-instruction (RD010·RD020·RD031·RD061·RD071) and SRL Bit 15 is set (SRL151).

3.6 B Bus Shifter

The GA leads provide the second operand input to the ALU (Sheet 14). The other input is the GB output from the B Bus Shifter (Sheet 14). The B Bus Shifter can load, shift left, shift right, or cross shift the B Bus data prior to presenting it to the ALU. The function performed is determined by the state of the SHCA1 and SHCB1 control leads applied to the eight 19-038 dual four-to-one multiplexors.

3.6.1 Load. The quiescent state of the B Bus Shifter is the Load Mode. This mode exists when both B Bus Shifter control leads are low. SHCA1 is low (12B9) when the Processor is not doing a Command Divide (DIV0)(12B6) or a Load specifying Shift Left or Cross Shift. SHCB1 is low (12C9) when the Processor is not doing a Command Multiply (MPY0)(12C6) or a Load specifying Shift Right or Cross Shift. SHCA1 and SHCB1 are decoded internal to the 19-038 packs to gate each bit from the B Bus to the corresponding GB lead.

3.6.2 Shift Left. The B Bus Shifter is conditioned to shift the B Bus data left one position when SHCA1 is high and SHCB1 is low. This occurs on a Command Divide or on a Load specifying Shift Left (LOAD1·RD121)(12B6). Each bit from the B Bus is gated onto the next more significant GB line. If Carry In is specified on the Load (RD141·DIV0) (15A3), the state of the Carry flag (FLR12) is applied to GB150.

3.6.3 Shift Right. When SHCA1 is low and SHCB1 is high, the B Bus Shifter shifts the B Bus data right one position. This occurs on a Command Multiply (MPY0) or on a Load specifying Shift Right (LOAD1·RD131). Each bit from the B Bus is gated to the next lower position of the GB Bus. If Carry In is specified (DIV0·RD141)(15A3), the state of the Carry flag (FLR12) is gated onto GB000.

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3.6.4 Cross Shift. The B Bus data is byte swapped by the B Bus Shifter when SHCA1 and SHCB1 are both high. This condition exists only during a Load Micro-instruction (LOAD1)(12B6), if Cross Shift is specified (RD121·RD131) and not suppressed by the X0 lead (12A6). A Cross Shift becomes conditional if the Memory Data Register (MDR) is specified as either the Source or Destination, or if on an I/O data read or data write, the Halfword test line is active. If the Processor is executing a Data Available or Data Request I/O operation, NOCS0 goes low (9K4) if the Halfword line is low (HW0)(9K1). NOCS0 suppresses Cross Shift (CS1) and jam sets RAL14. If the Cross Shift is not suppressed by NOCS0, and MDR is involved, the Cross Shift is allowed if the Memory Address Register is even (MAR150 high). If MAR is odd (MAR150 low), the Cross Shift is not performed. When the Cross Shift occurs, Bits 00:07 from the B Bus are gated to GB 08:15 and B 08:15 are gated to GB 00:07.

3.7 Arithmetic Logic Unit (ALU). The Arithmetic Logic Unit (ALU) consists of four 19-039 four-bit ALU packs and one 19-040 carry look-ahead pack. The ALU is shown on Sheet 14. The ALU receives five control lines defining the function it is to perform. These control lines are summarized on Table 2.

TABLE 2. ALU CONTROL LINES.

OP	M	S0	S1	S2	SUB
D	0	1	0	0	0
C	0	1	0	0	0
T	1	1	1	1	0
B	1	1	1	1	0
L	1	1	1	1	0
O	1	1	1	0	0
N	1	0	1	1	0
X	1	1	0	0	0
A	0	1	0	0	0
S	0	0	1	1	1

Each 19-039 ALU pack develops four-bits of the low active S Bus. The four S Bus bits are internally NANDed to produce the SXXX1 zero indicating signal. When the signals S1251, S8111, S0471, and S0031 are all high, the S Bus data is zero. Each ALU produces an output carry on Pin 16. Only the carry output of the most significant ALU is used (CSV1)(14D9). The internal Carry Propagated (CP) to the most significant stage of each ALU pack is available on Pin 15, and the Carry Generated (CG) for the most significant stage is available on Pin 17. These signals, CPXX1 and CGXX1 are applied to the 19-040 carry look-ahead pack to develop the Carry In to the next more significant ALU pack (CNXX1).

Each function of the ALU is described in the following paragraphs. Unless otherwise noted, all gate references are to the arbitrary labels on Figure 3.

3.7.1 Load. The ALU is conditioned to the Load Mode on a Test, Branch, or Load Micro-instruction. In this mode, Gates 1, 2, 3, and 4 are enabled by S01, S11, S21 and SUB0 respectively, and Gate 8 is disabled by M1. The AR is not unloaded, so the false GAXX0 Bus disables Gates 2 and 3. Gate 1 produces a high output causing the output from Gate 5 to go low. The state of the GBXX0 Bus is passed to the SXX0 Bus from Gates 4, 6, 7 and 9.

3.7.2 AND. In this mode, conditioned by the AND Micro-instruction, each bit from the B Bus is logically ANDed with the corresponding bit from the GA Bus. The output equation for Gate 5 becomes $\overline{A}\cdot B$. The output equation for Gate 6 is simply B. Consequently, Gate 7 yields the function $A\cdot B$ which is inverted by Gate 9, forming the S Bus.

3.7.3 OR. The OR Micro-instruction causes each bit from the B Bus to be logically ORed with the corresponding bit from the GA Bus. Gate 5 produces a low output because of the complimentary GA inputs. The OR function is realized entirely by Gate 4. Gate 4 produces a low output whenever either the GA or GB input is active (low). The logical sum is double inverted by Gates 6 and 9, forming the S Bus.

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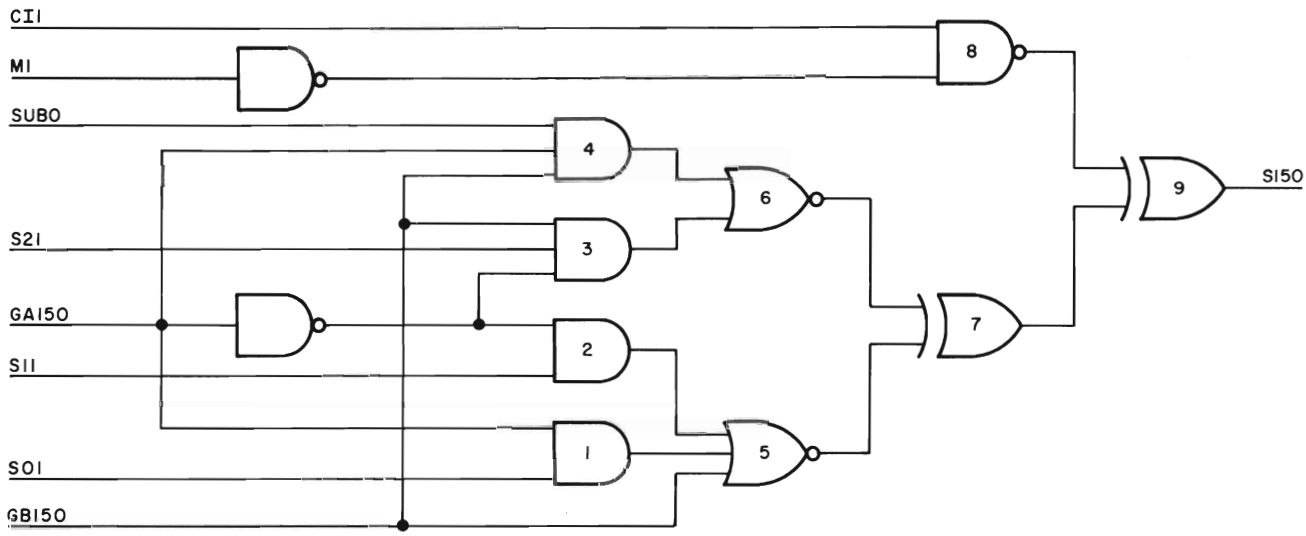


Figure 3. Least Significant ALU Stage

3.7.4 Exclusive OR. The Exclusive OR Micro-instruction produces the logical difference of the data on the GA and GB Busses. Gate 5 produces a high output when the A·B condition is met. Gate 6 produces a high output when the A+B condition is met. When combined by Gate 7, the Exclusive OR function ($A\cdot\overline{B} + \overline{A}\cdot B$) is realized.

3.7.5 Add. The ALU is conditioned to the Add Mode on a DO, Command, or Add Micro-instruction. Note that with the exception of the M control line, Add is the same as Exclusive OR. The M control line enables the carry networks internal to the ALU device so that the output from Gate 8 is $(\overline{A}B+A\overline{B})\cdot\overline{C} + (AB+\overline{A}\overline{B})C$. Figure 3 shows only the least significant stage of the 19-039 four-bit ALU. The next three stages are identical with the exception of the internally propagated carry.

3.7.6 Subtract. The Subtract function produced by the 19-039 four-bit device is A-B-1. For this reason, the Carry In to the least significant state is inverted on the Subtract Micro-instruction. The output equation for Gate 5 is $\overline{A}B$ and the equation for Gate 6 is $\overline{A}+B$. Gate 7 produces a high output when the equation $\overline{A}\overline{B}+AB$ is satisfied. If no Carry In is specified, the CI1 (14A5) lead is high and the output from Gate 9 is high. If Carry In is specified, the output from Gate 7 is inverted by Gate 9, producing the S Bus.

3.8 Counter Dependent Operations

A Command Micro-instruction with RD Bit-6 set implies a counter dependent mode of operation that is maintained until the Counter Register (CTR) is zero. Command Repeat causes the next micro-instruction to be repeated the number of times specified in the CTR. Command Multiply and Command Divide cause the Command itself to be repeated with SRH forced to be the Source and Destination Register. These modes are implemented by the circuit shown on Sheet 13.

3.8.1 Repeat. When a Command Repeat Micro-instruction is executed, CMD1 goes high (13K7). The Repeat flip-flop (RPT)(13K8) toggles set on the trailing edge of SCL1 · SYSCL1. On the same edge,, the Counter Mode flip-flop (CMODE) will toggle set if the CTR is not zero (CEMT0)(13N6). If the CTR is zero, the next micro-instruction should not be executed. Since, at the same time RPT flip-flop toggles set, the next micro-instruction toggles into RD, the Processor has to execute the instruction. However, KILDST0 goes active (13N9) stopping the Destination Clock, DCL0 (19M9). No register will be modified, nor will the FLR change. RPT will toggle reset on the next SCL1 · SYSCL1.

If the CTR is not zero, CMODE and RPT both toggle set. Now the target micro-instruction is in RD. Because CMODE is set, DECTR0 (13F9) goes low until the CTR is zero. The CTR will decrement on each Destination Clock. As long as CMODE is set and the CTR does not equal zero or one (CTLT21)(13M8), STPC0 is low (13R9), disabling RCL0 and RDSTB0 (19L9). The RAL will not increment nor will another micro-instruction be strobed into RD until the Counter decrements from one to zero. As soon as the CTR decrements from one to zero, CMODE and RPT both toggle reset. STPC0 is high and the next sequential micro-instruction is executed.

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3.8.2 Multiply. Prior to executing the Command Multiply Micro-instruction, the following preliminary conditions are assumed: The multiplier is in SRL, SRH contains zero, the AR holds the multiplicand, the Carry flag is cleared, and the Counter contains 16. The Command Multiply is executed in 16 machine cycles. On each Destination Clock; the CTR is decremented, SRL is shifted right one place, FLR12 is updated from the ALU Carry (CSV1)(14D9), and SRH is loaded from the S Bus. Refer to Figure 4.

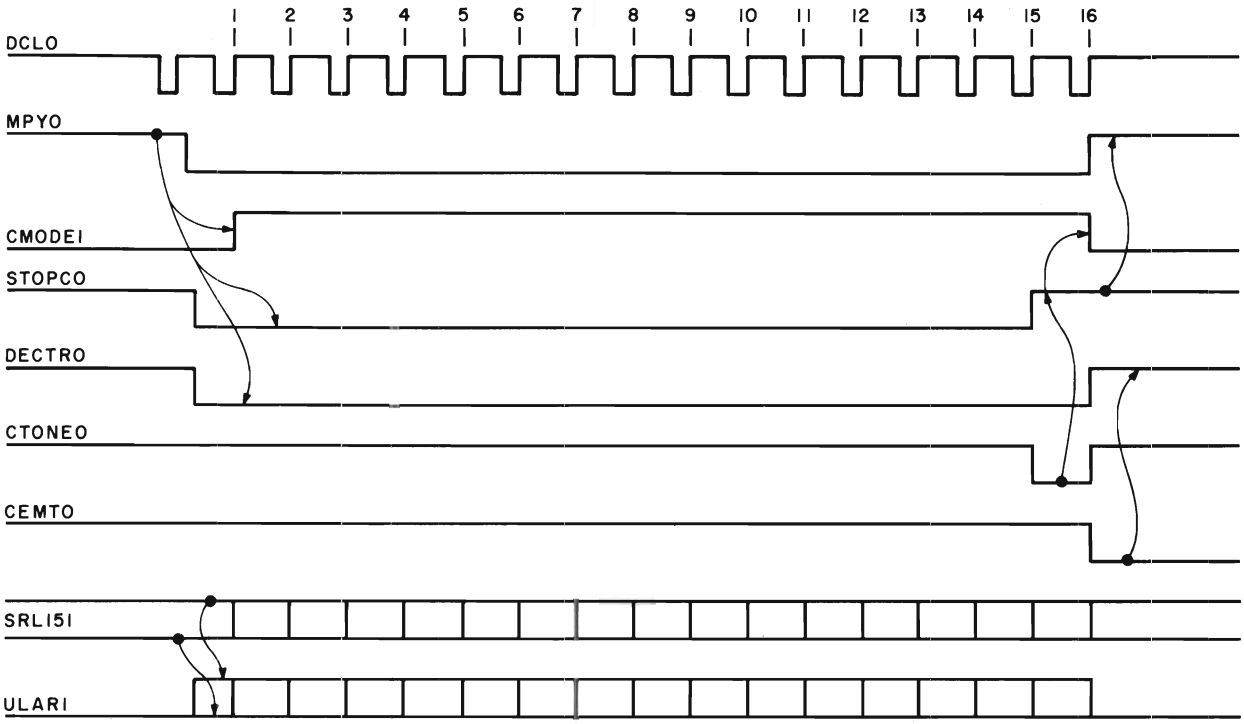


Figure 4. Command Multiply Timing Diagram

As soon as the Command Multiply Micro-instruction is decoded, the signal MPY0 goes low (13H7). As long as the CTR is not zero (CEMT0 false), DECTR0 is low (13F9) and the Counter decrements on the trailing edge of each Destination Clock. Shift Register Lower (SRL) is also conditioned to the Shift Right Mode, SRLM01 low and SRLM11 high, by the MPY0 signal. Similarly, Shift Register High (SRH) is conditioned to the Load Mode, SRHM01 and SRHM11 high. At the trailing edge of each DCL0, SRL shifts right one position and SRH is loaded from the S Bus.

The data loaded into SRH constitutes the sum of the accumulated partial products. The signal MPY0 is ORed with DIV0 to produce MD0 (13H9). MD0 forces the contents from SRH to be gated onto the B Bus (16A1). The B Bus Shifter is forced to the Shift Right Mode by MPY0. Now, depending on the state of the least significant bit from the multiplier (SRL15), the multiplicand in AR is either gated to the ALU or not. If SRL151 is high, ULAR1 (13N5) is high. The AR is gated to the ALU and the sum from AR and the shifted SRH is gated back into SRH. If SRL151 is low, the AR is not gated to the ALU and zeros are added to the shifted SRH. The result of the latter case is a 32-bit shift right.

Carries resulting from the additions that occur are saved in the Carry flag (FLR12) which is shifted back into the high end of the B Bus Shifter for the next cycle so no data is lost.

After the Command Multiply, the product in SRH and SRL must be shifted right one more position.

3.8.3 Divide. Prior to executing the Command Divide Micro-instruction, the following preliminary conditions are assumed: The 32-bit positive dividend is in SRH and SRL, the divisor is in two's complement negative form in the AR, the Carry flag is reset, and the CTR contains 16. The Command Divide executes in 16 machine cycles. On each DCL0; the CTR is decremented, SRL is shifted left one position, FLR12 is updated from the ALU Carry, and SRH is either shifted left one position or loaded from the S Bus. Refer to Figure 5.

The signal DIV0 is low during the Command Divide. DIV0 causes DECTR0 to go low until the Counter decrements to zero. SRL is conditioned to the Shift Left Mode, and SRH assumes the Load Mode or the Shift Left Mode depending upon the state of the ALU Carry (CSV1).

The most significant 16-bits of the dividend in the SRH are present on the B Bus. The data is shifted left one position by the B Bus Shifter and presented to the ALU. Note that SRL00 is carried into GB15 (14R1). The AR is unloaded to the ALU and an 'Add' is performed.

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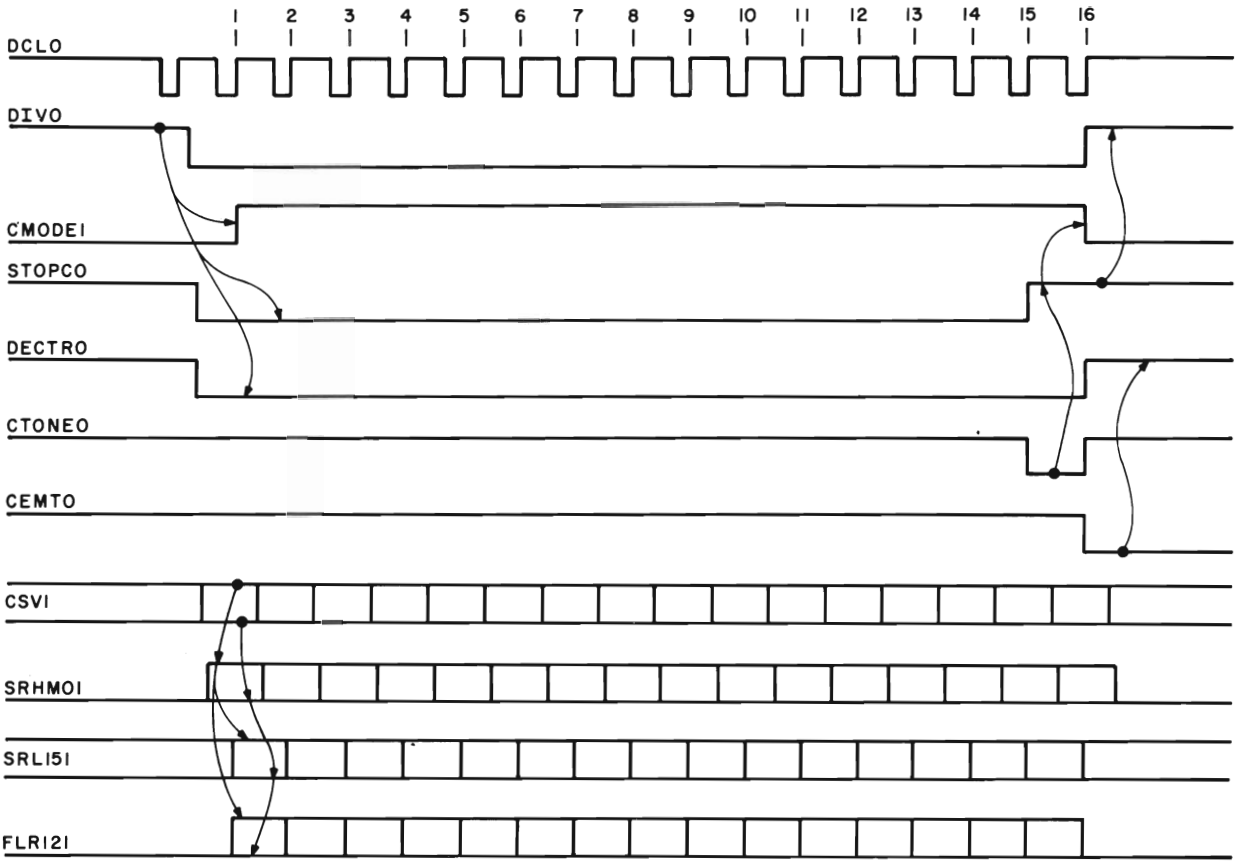


Figure 5. Command Divide Timing Diagram

By adding the two's complement from the divisor in the AR to the most significant half of the dividend in the SRH, the result on the S Bus is actually the difference between the two. If this 'trial subtraction' is successful, the ALU produces a Carry (CSV1 high), and the partial remainder on the S Bus is gated into the SRH. If the 'subtraction' is unsuccessful, CSV1 is low, and the SRH is shifted left one position; the S Bus data is ignored. The CSV1 signal is shifted into SRL15 to form the quotient bits. CSV1 is also saved in FLR12. After the Command Divide, the remainder is in the SRH and the quotient is in the SRL.

3.9 Phase Control

3.9.1 General Description. The Phase Control logic, contained on the 35-388 ROM board, is shown on Sheet 9 and in block diagram form on Figure 6. Phase is a hardware condition that is affected by the DO Micro-instruction and user program activity. Phase, in turn, affects actions resulting from the DO Micro-instruction.

The two stage Phase Counter defines the four hardware phases. Referring to Figure 6, from a count of 00 (Phase Zero), the Phase Counter can go to a count of 01 (Phase One) or 10 (Phase Two). From Phase One, the Phase Counter can only go to Phase Two. From Phase Two, the Phase Counter can go to a count of 00 (Phase Zero) or 11 (Phase Three). From Phase Three, the Phase Counter can only go to Phase Zero. A phase change usually occurs on a DO Micro-instruction. Initialize unconditionally forces the Phase Counter to Phase Three, as does a Phase Two abort.

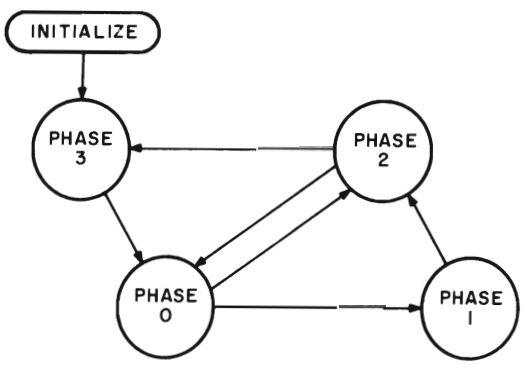


Figure 6. Phase Control Flow Diagram

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Each phase, other than Phase Zero, has corresponding sets of micro-code routines. The phase control hardware generates the starting addresses of these routines.

Phase Zero is dedicated to user's instruction decoding. Phase Zero is a purely hardware state, lasting for two or four system clocks. During Phase Zero, the user's instruction is automatically loaded into the Instruction Register (IR), and the A Register (AR) is automatically loaded from the User's second operand register (YS). If the user's instruction is of the RR format (Op-Codes 0n, 1n, 2n, 3n, 8n, or 9n), Phase Zero is exited and Phase Two is entered. If the user's instruction is not RR, a second memory read is generated to fetch the second half of the fullword instruction, the Location Counter (LOC) is incremented by two and Phase Zero is exited.

If the user's instruction is RS (Op Codes Cn or En), Phase One is entered if the instruction is indexed - IR Bits 8:11 not zero - and the ROM Address Registers are forced to '002'. If the instruction is not indexed, Phase Two is entered.

If the user's instruction is RX (Op Codes 4n, 5n, 6n, 7n, An, Bn, Dn, or Fn), Phase One is entered. The ROM Address Registers are forced to '006' if the instruction is indexed or to '004' if the instruction is not indexed.

The Phase One micro-code routines perform the second operand address arithmetic.

The Phase Two entry point for a particular user instruction is derived from the Decoder Read-Only-Memory (DROM). Words in the DROM are addressed by the Operation Code field of the user's instruction, IR 0:7. The DROM contains 256, 12-bit words. The Model 70 user's instruction repertoire uses 113 words. The words not used contain zeros and correspond to illegal user's instructions.

As Phase Two is entered, the DROM read-out is jammed into the ROM Address Registers. The next micro-instruction executed will be that at the specified location.

The Model 70 instruction repertoire includes 22 Privileged instructions. Privileged instructions (all I/O instructions plus LPSW and EPSR) may only be executed if PSW Bit-7 is reset. If PSW07 is set and an attempt is made to execute a Privileged instruction, the Illegal instruction interrupt is forced.

The Privileged instructions are identified in the DROM by having Bit-4 of the read-out set. When Phase Two is entered, the ROM Address Registers are allowed to be jammed from the DROM. Then, when the non-existant location is read-out, the ROM Data Register (RD) is direct cleared.

When Phase Two is entered, the abort Enable flip-flop (EBL) is set. As long as EBL is set, the Processor can be interrupted by the occurrence of an I/O Attention (ATN), a Data Channel request, or a Machine Malfunction which includes parity failure and Early Power Fail (EPF) detection. This abort condition forces the Processor to Phase Three and jams the ROM Address Registers to '00A', the starting address of the abort micro-routine. The EBL flip-flop automatically resets whenever the micro-program does a Memory Write (MW or PW), an I/O operation, or changes a user General Register or the PSW or the LOC. When Phase Two is exited, the DO Micro-instruction automatically tests for interrupts, regardless of the state of EBL. The interrupts tested for are I/O Interrupt (ATN), Console Interrupt (CATN), Console Single Mode (SNGL), Machine Malfunction (MALF), Primary Power Fail (PPF), Data Channel request (DC), and Fast I/O Interrupt (FAST). If any interrupt is true, Phase Three is entered and the ROM Address Registers are jammed to '010'. If no interrupts are pending, Phase Zero is entered.

The Phase Three firmware sets (entry points '000', '00A', '010', and '100') are dedicated to display and interrupt support. When Phase Three is exited, Phase Zero is entered.

3.9.2 Functional Description. When RD 00:03 are zero, D1 goes high (8K4). This may occur on the DO Micro-instruction or an Illegal instruction. The illegal condition exists if the Run flip-flop is set (8J6) and the RD14 flip-flop is reset (8R3). (A DO Micro-instruction always has RD Bit-14 set.)

When the Processor is initialized, the signal SCLR1A (8A6) is active. Initialize clears the ROM Address Registers and the ROM Data Register, and the Run flip-flop at 8J6 is reset. D1 is ANDed with RD140 and RUN1. If the Run flip-flop is not reset at this time, ILEG0 goes low, forcing the Processor to Phase Three and the ROM address to '100'. As soon as a word whose Op-Code is not zero is read from the ROM, D0 on the J input to Run goes high and the flip-flop toggles set.

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The DO Micro-instruction may specify one or more functions to be performed. Bits 4 and 5 specify a Memory Read, Memory Write, or Privileged Write. DDC1 (8B9) is high if the Processor is executing a DO or Command Micro-instruction. DDC1 at 30R9 generates a memory start (PSTART0). See Section 4.

Bit-6 set causes the Location Counter (LOC) to be incremented by two. If the Processor is not going to Phase Three (GTP30) or is not in Phase Zero with Memory Busy (P01·FPMBY1), FRCLOC0 goes low (9J5). FRCLOC0 forces the LOC to be both the Source and Destination (25B1) and forces GA140 to be active (12S3). The AR is not unloaded, so the GAXX0 Bus equals 2. The ALU is conditioned to do an Add operation and, at DCL0, LOC is loaded with the value (LOC)+2.

Bit-7 set causes the contents of the Flag Register to be copied into the Condition Code Register. LCC0 at 9N4 goes low during the last machine cycle of a DO Micro-instruction. A DO Micro-instruction is normally executed in one machine cycle (250 nanoseconds). It takes more than one cycle if a memory operation is specified and memory is busy, or if a phase change is specified and the new phase is Phase Zero.

The phase change is specified by RD Bit-8. The signal DRD081 goes high (8J9) to indirectly enable the Phase Counter. The Phase Counter is initialized to Phase Three. From Phase Three, the Phase Counter can only step to Phase Zero. The K input to the PC1 flip-flop (9G2) goes high with DRD081. The K input to the PC0 flip-flop (9F2) goes high because DTEST0 and GTP30 are false. DTEST0 can only be active during Phase Two and, GTP30 can only be active during Phase Two or on Illegal. The NAND gate at 9F7 produces a low output on DRD081 if memory is not busy (FPMBY0). The Phase Enable lead (PHEN1) at 9F9, goes high. This lead is ANDed with MSST0 and SCL1 to develop the toggle input to the Phase Counter flip-flops (9F2). MSST0 (9E1) is low if an attempt is made to start memory when the memory is busy. On the trailing edge of SCL1, Phase Zero is entered.

The DO Micro-instruction that causes Phase Zero to be entered must specify a Memory Read. The word read from memory will be taken as the next user instruction to perform. Phase Zero lasts for two or four machine cycles (assuming one microsecond core memory). For the duration of Phase Zero, the DO Micro-instruction remains in RD. The signal STOP0 goes low for the cycle before Phase Zero was entered by DRD081·DTEST0·PC01 (9B1). As soon as Phase Zero is entered, P01A·FMDUA1 (9D1) holds STOP0 down until memory data is available. STOP0 disables RDSTB0 and RCL0 (19L6) so that another micro-instruction is not strobed into RD, and RAL does not increment.

On the machine cycle before Phase Zero is entered, the ROM Address Registers are cleared (PHEN1·P00·T21SY1 = RACLR0) (9B9). At the same time, the Instruction Register is direct cleared by CRLIR0 (9A9).

When the memory data is strobed into MDR, the IR receives the same information. GMSIR1 goes high (28C2) to gate the Memory Strobe Bus (MS) to the direct set inputs of the IR flip-flops. Shortly after the Memory Strobe (MS), and one machine cycle into Phase Zero, the data unavailable signal FMDUA1 goes low. See Figure 7.

If the instruction in IR is of the RR type, RR1 (9D5) goes high. Phase Zero and RR generate GTP21 (9D9) and PHEN1 (9F9). GTP21 allows the J input to the PC1 flip-flop to go high (9G2). The Phase Counter steps to Phase Two on the SCL1. GTP21 also generates GDROM0A and GDROM0B at DT21 time (9H9). These signals strobe the DROM read-out into the ROM Address Registers on Sheet 5. On the clock that steps the Phase Counter to Phase Two, the AR is loaded from the user's second operand register, specified by YS. LARYS0 at 9C4 goes low when memory data becomes available. LARYS0 forces YS to be the source and the AR to be the destination. The contents of YS are added to zero and placed into the AR.

If the user's instruction is not RR, the signal STOP0 is held low until memory becomes un-busy (9D3). Phase Zero will last for four machine cycles. After memory data becomes available, the AR is loaded from YS and, at the same time, the Skip flip-flop (Sheet 18) is toggled set by SSKIP0 (9B9).

The Skip flip-flop resets, on the clock, after memory goes un-busy (KSKIP0)(9F9). The Skip flip-flop keeps YS off the B Bus for the remainder of Phase Zero by disabling the LARYS0 signal at 9C4.

The B Bus must be kept clear so that when memory does go un-busy, the LOC can be incremented again (FRCLOC)(9J5). As soon as memory goes un-busy, another Memory Read is started. This occurs because the DO Micro-instruction is still in RD. This Memory Read will fetch the second half of the user's instruction. If the instruction in IR is RS with no indexing (AMOD0), the new phase is Phase Two (GTP21 = 1)(9D9). When memory goes un-busy, PHEN1 goes active to step the Phase Counter to Phase Two. See Figure 8.

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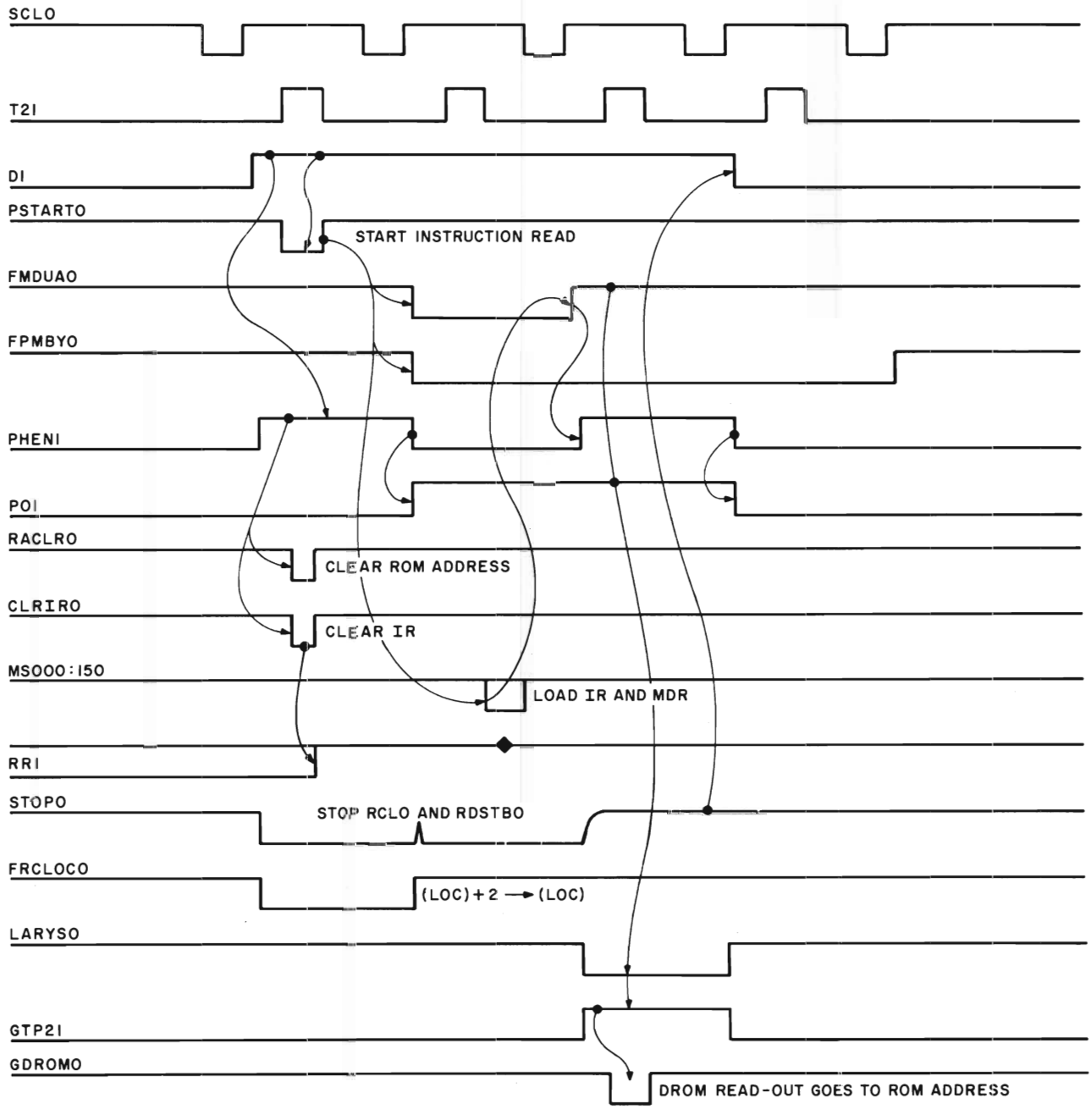


Figure 7. Phase Zero Timing (RR)

If the instruction in IR is RS with indexing or is RX, the new phase will be Phase One. The J input to PC1 goes high (P01·GTP20). On T21, the Phase One entry point is generated by the gates in area 9C3 and at SCL1, Phase One is entered.

The DO Micro-instruction exiting Phase One always causes Phase Two to be entered. GTP21 is active during all of Phase One. The DO Micro-instruction that exits the two RX Phase One routines ('004', '006') specifies a Memory Read. Normally, execution of the DO Micro-instruction is delayed because memory is still busy from the Memory Read generated in Phase Zero.

If IR holds a STH, BAL, BTC, or BFC user instruction (Op-Codes '40', '41', '42', or '43'), the signal STBR1 at 9E6 goes high. STBR1 generates DISB0 at 9C9 which in turn causes PHEN1 to go high and NOMEM0 to go low. This Phase One DO Micro-instruction will execute in only one machine cycle. NOMEM0 keeps the memory from starting (8A9) and DISB0 keeps the clocks from stopping (4L1). See Figure 9.

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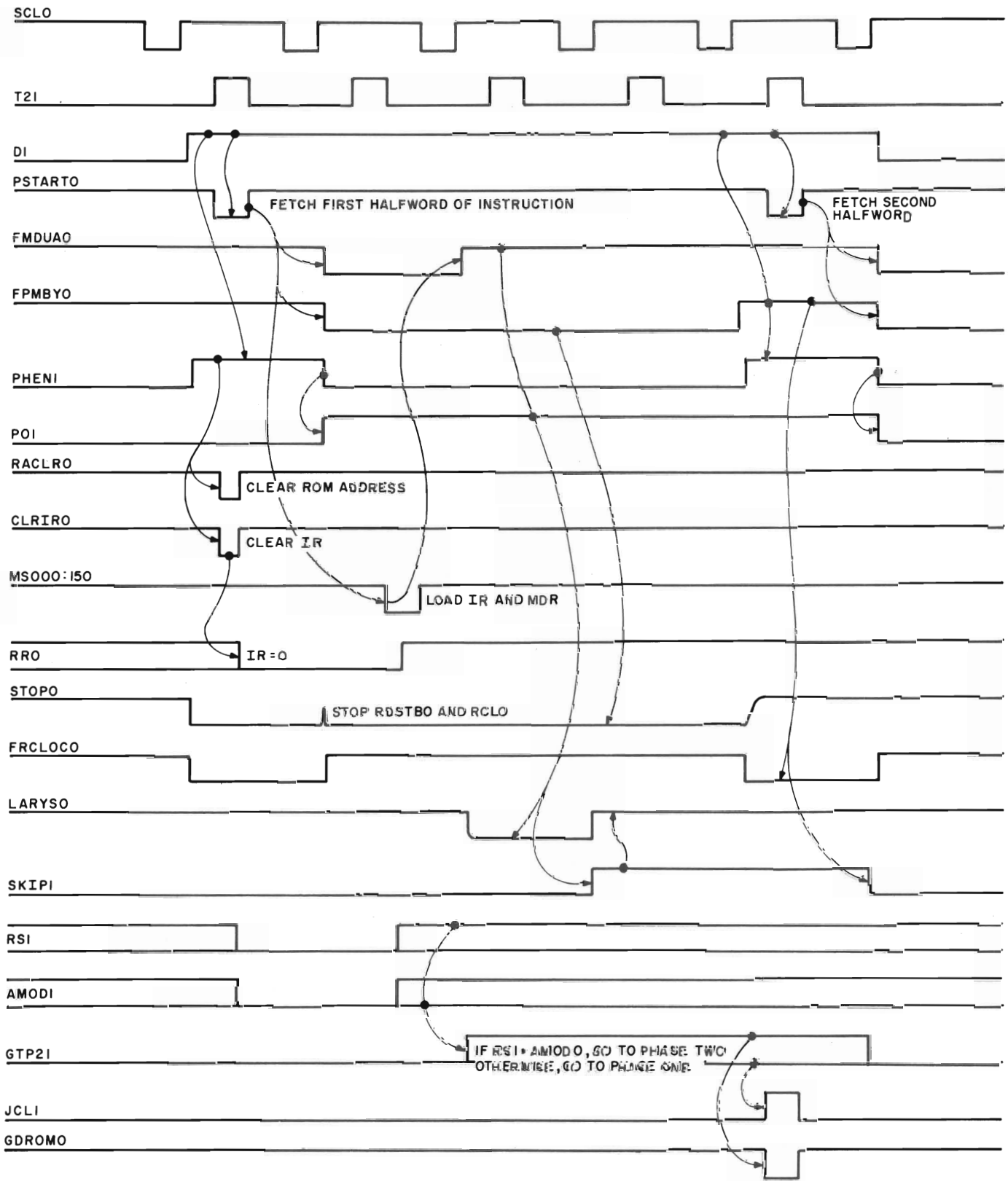


Figure 8, Phase Zero Timing Non-RR.

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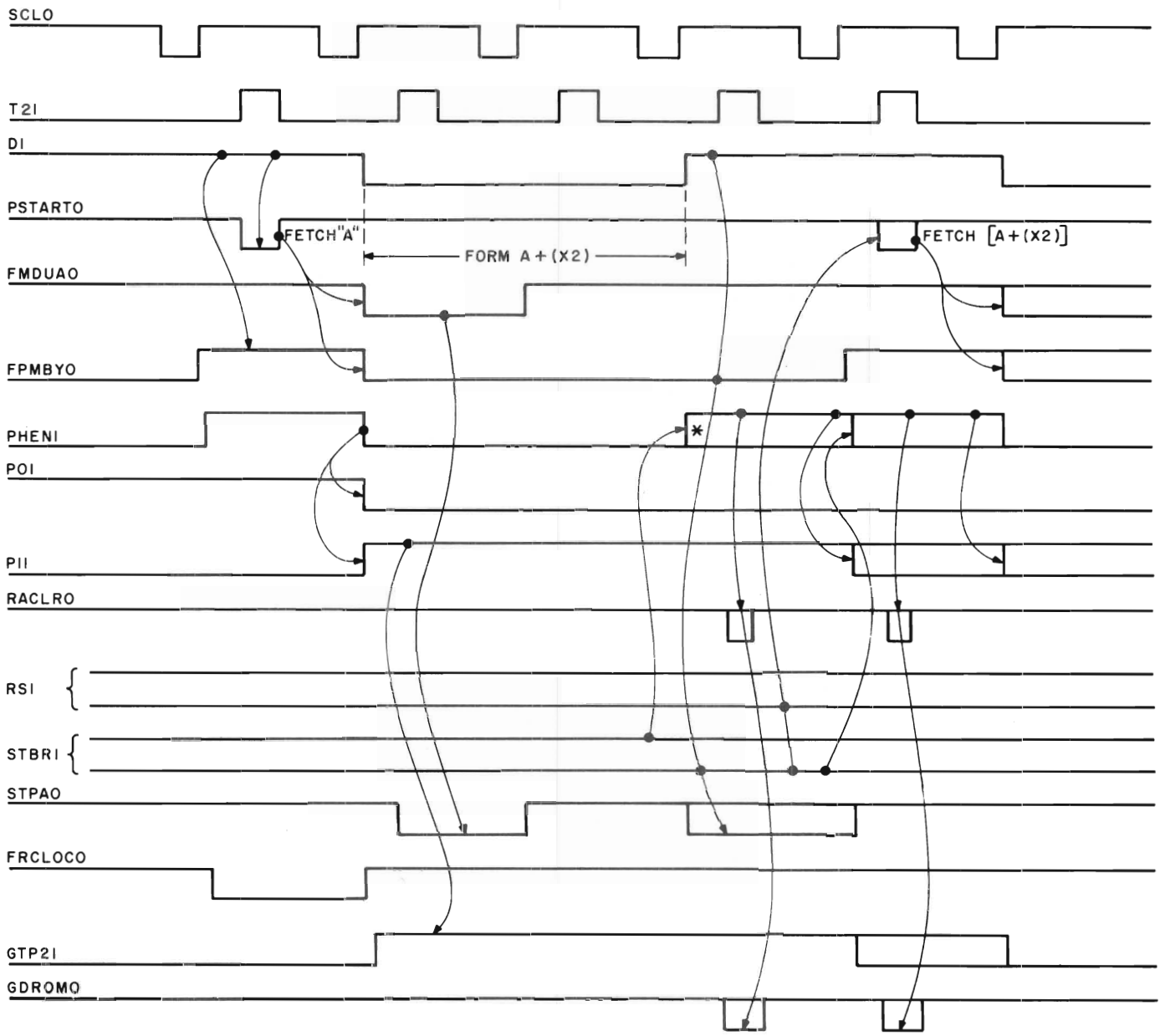


Figure 9. Phase One Timing

If the instruction in IR is illegal, the associated DROM read-out is zero. The Processor enters Phase Two and reads the contents of ROM location '000' into RD. ROM location '000' contains zeros so the illegal condition occurs. ILEG0 goes low (9G5). PHEN1 goes high due to the GTP30 signal. On the next SCL1, the Phase Counter steps to Phase Three. The ROM Address Registers clear at T21SY1 (RACLR0), and RAH07 is forced set (SRAH070)(9H9). If the instruction in IR is privileged (DROM Bit-4 set) and if PSW07 is set, RAH04 is allowed to set. The illegal ROM address causes RD to be direct cleared on RDSTB0 and the illegal condition occurs. See Figure 10.

As soon as Phase Two is entered, the abort Enable flip-flop (EBL)(4S3) is allowed to set. EBL resets when a Memory Write or Privileged Write is performed (MWPW0), an I/O operation is performed (UD100, LD100), a General Register is loaded (LYD0), PSW is loaded (LPSW0), or the LOC is loaded (LLOC0, FRCLOC0). If one of these conditions occurs on the first micro-instruction in Phase Two, EBL resets immediately. As long as EBL remains set, if an I/O Interrupt (ATN1·PSW01), Data Channel Interrupt (DC0), or Machine Malfunction (MALF1) occurs, the TESTA flip-flop is allowed to set. If TESTA sets during Phase Two, ABRT0 goes low if NLRAL0 is high. NLRAL0 goes low on a branch micro-instruction or a micro-instruction other than Do, Command, or Test in which RAL is the destination. ABRT0 causes GTP30 to go low (9G6). On the next SCL1, the Processor enters Phase Three at ROM address '00A'. See Figure 11.

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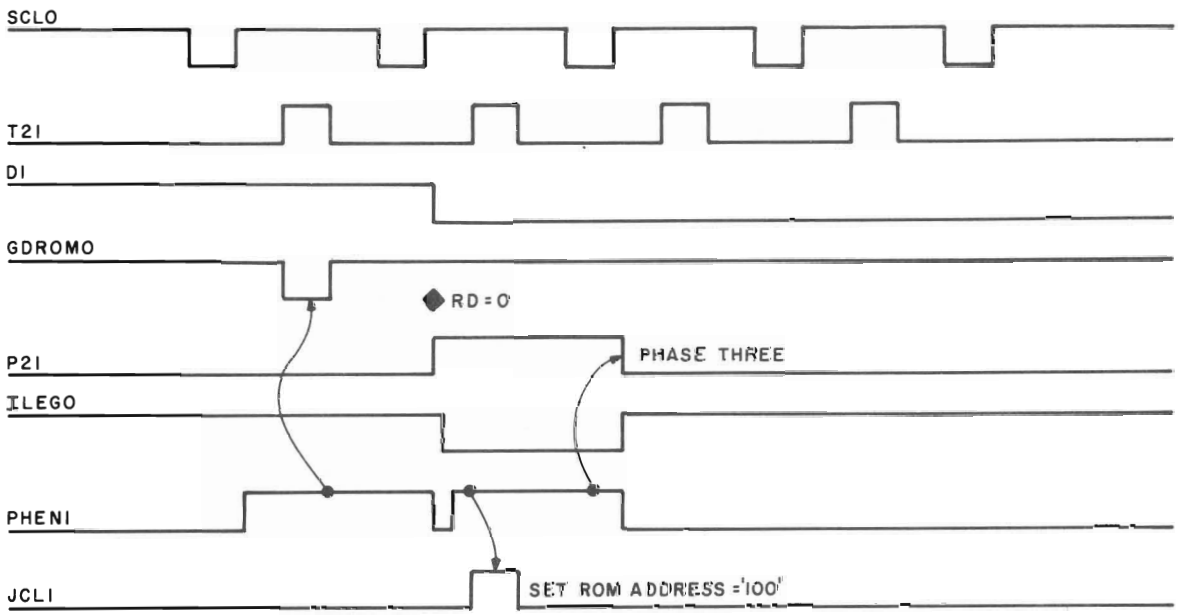


Figure 10. Phase Two Timing (Illegal)

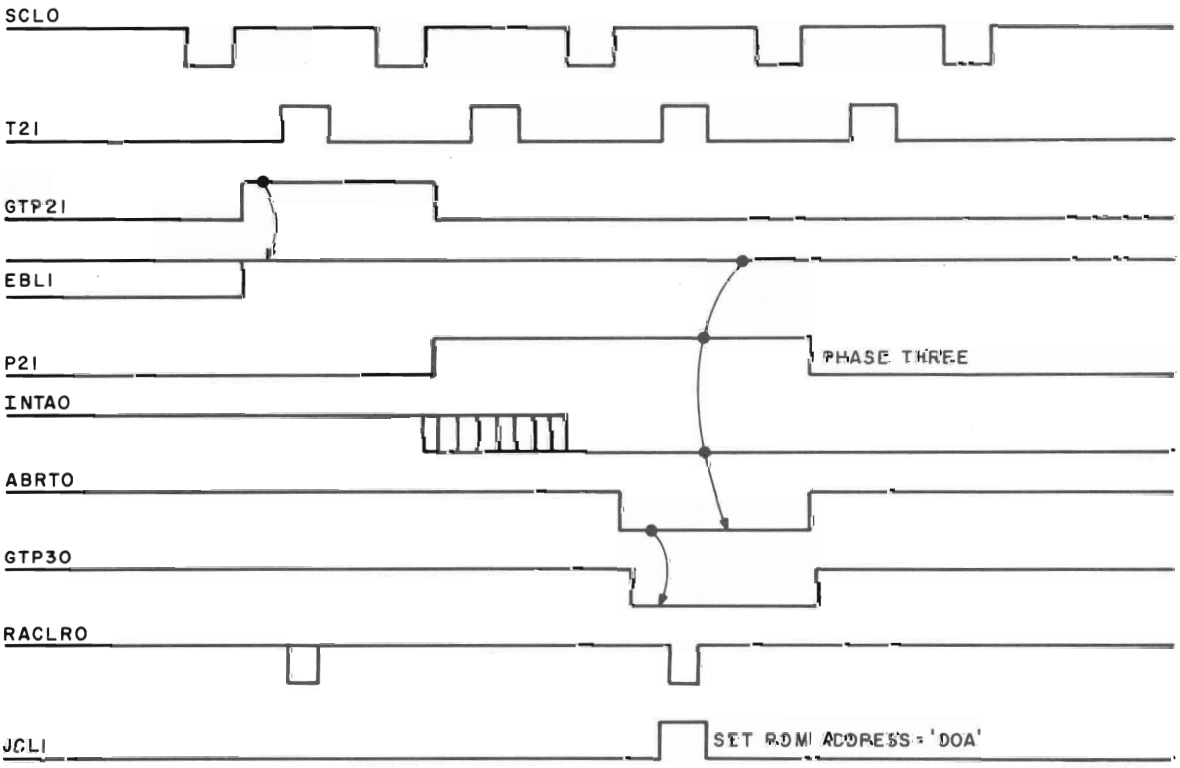


Figure 11. Phase Two Timing (Abort)

If an abort has not occurred, the DO Micro-instruction that exits Phase Two automatically tests for interrupts. See Sheet 18. The interrupts tested for are ATN1·PSW11, DC0, and MALF1 which form INTA0; and CAT80, SNGL0, or PPF0 which form INTB0. The occurrence of any interrupt is synchronized by the Test flip-flop. If Test is set when the DO Micro-instruction that exits Phase Two is executed, E1·BD081A·TEST1 generates DTEST0. DTEST0 (18N9) causes GTP30 to go low. The Processor enters Phase Three at ROM address '016'. See Figure 12.

If no interrupts are pending, DTEST0 remains high and the Processor goes to Phase Zero instead of Phase Three, as shown in Figures 7 and 8.

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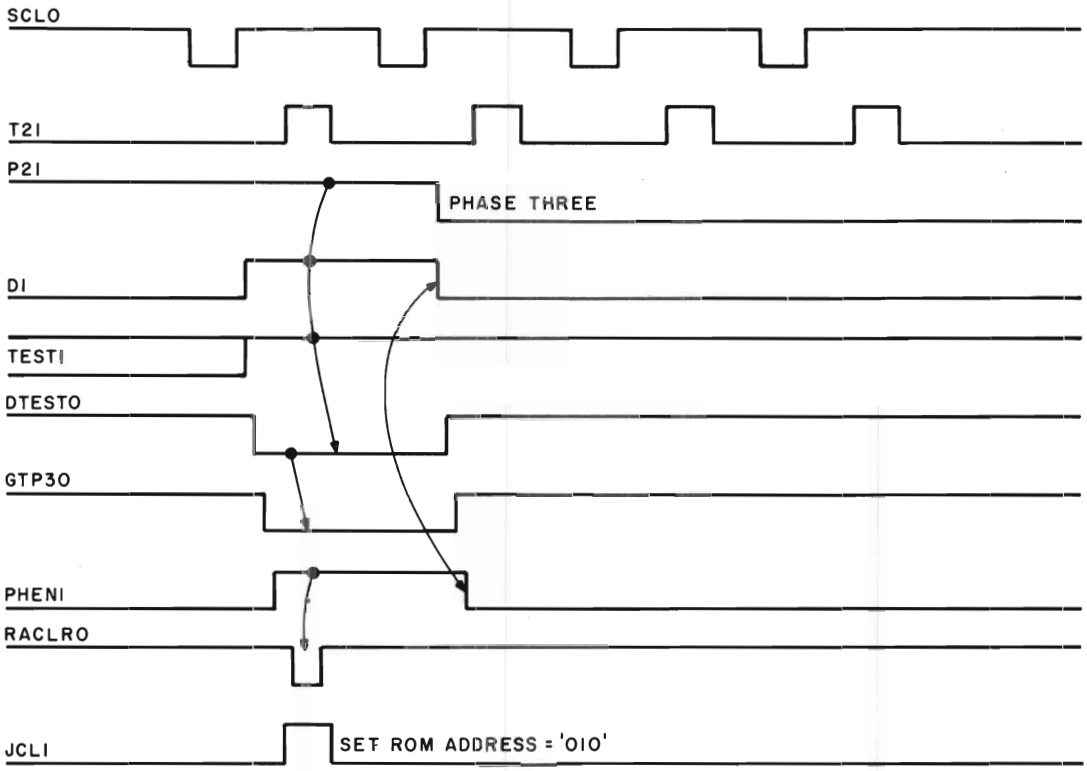


Figure 12. Phase Two Timing (Interrupt)

Bit-9 set causes CLR0 to go low during the last machine cycle of a DO Micro-instruction. CLR0, also low on GTP30, resets the Bank flip-flop (12M8), the Utility flip-flop (12M8), the CMODE flip-flop (13M8), the RPT flip-flop (13K8), the Flag Register (Sheet 17), and the Counter (27F5). For the case where CLR0 and LCC0 are both active, the Condition Code of PSW is updated from the FLR before the FLR is reset.

If RD Bit-10 is set, the Wait indicator on the Control Panel is set. The Wait lamp is driven by the RS flip-flop shown on Sheet 8. RD Bit-11 set causes the Wait flip-flop to reset.

If RD Bit-12 is set, Bits 13, 14 and 15 of the ALRM Register are loaded into Bits 13:15 of the Condition Code. The signal JACC0 (9L4) goes low if D1, MSST0, P00, and RD121 are active. On Sheet 17, if LCC0 is also active, the ALRM bits are ORed with the FLR bits and loaded into the Condition Code.

If RD Bit-15 is set, a Power Down is generated (POW0)(19L2) to set the STPSYS flip-flop.

3.10 I/O Control

An I/O operation is initiated if IO is the Source or Destination of a Load Micro-instruction. The I/O Control logic is shown on Sheet 4. The control line gating is shown on Sheet 20 and the data line gating is shown on Sheets 16 and 20. If RD contains a Load Micro-instruction, LOAD1 at 4B1 is high. If IO is the Source, UDIO0 is low. If IO is the Destination, LDIO0 is low. LOAD1·ABORT0·(LDIO1+UDIO1) produces G101 (4B2) which starts the I/O sequence. I/O timing is discussed separately for input and output.

3.10.1 Input. The initialized state of the I/O sequencer is Line, DST, and DIO flip-flops reset. On input, UDIO0 is low and LDIO0 is high. The gate at 4C3 produces a low output at DT21 time, direct setting the Line flip-flop. On the trailing edge of T21SY1, the DST flip-flop toggles set. This disables the clocks DCL0, RDSTB0 and RCL0 until a Sync returns to reset the DST flip-flop. Because the Line flip-flop sets, a control line, selected by RD 14 and 15 is gated out (Sheet 20). The addressed device controller should respond to the control line with data on Data Lines D00:15 and a Sync.

When the Line flip-flop sets, the 13-15 microsecond delay at 4H2 starts. This delay generates a False Sync if a device fails to respond within the delay period, assuring that the Processor does not hang up. The RS flip-flop (DIO)(4E3) latches the occurrence of a False Sync and locks out the other. SYNCH1 goes high allowing DST to toggle reset on the next T21SY1, and the Line flip-flop to toggle reset on the following DCL0 which resets the RS flip-flop had Sync time out occurred. The False Sync delay is also direct cleared.

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When the Line flip-flop resets, the control line drops and the device controller drops SYN0. SYNCH0 is used to keep an I/O operation from starting until SYN0 from the previous operation has been dropped.

In the case of a False Sync, the Overflow flag (FLR13) is direct set at SCL1 time by the SV0 lead (4F4). If the I/O operation was a Status Request, B Bus Bit-13 is forced active (B130)(4G4) to simulate the Examine Status condition.

At the end of an Input type I/O operation, the DCL0 that toggles the Line flip-flop reset also loads the specified Destination Register from the S Bus. See Figure 13.

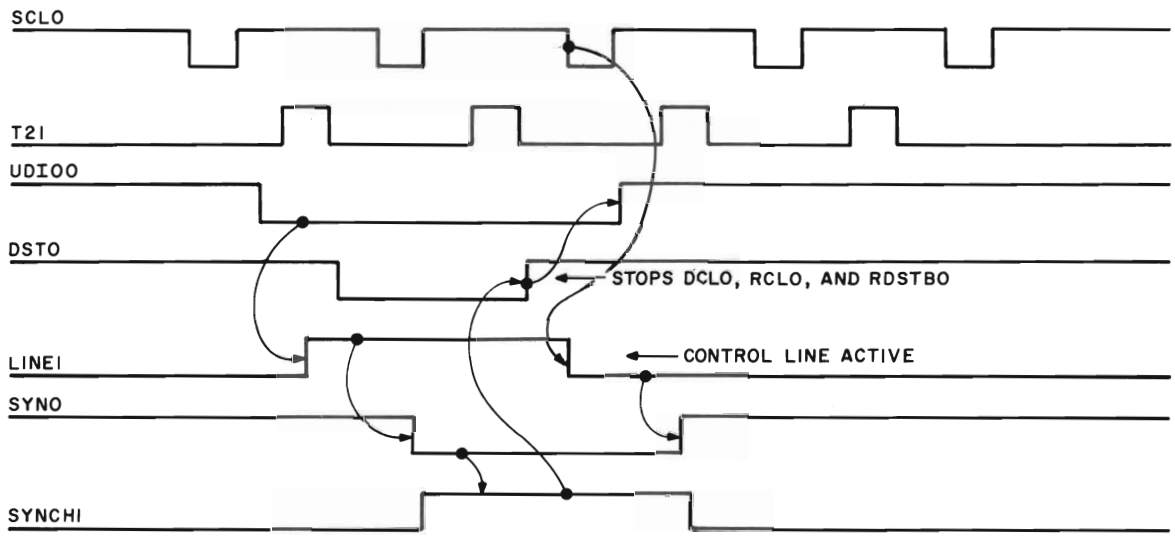


Figure 13. I/O Timing (Input)

3.10.2 Output. With LDIO0 active, DST toggles set at T21SY1 time and 100 nanoseconds later, the Line flip-flop is direct set by the gate at 4C4. The delay is to guarantee that the data to be output is present on Data Lines D00:15 at least 100 nanoseconds before the control line is switched on. The control line, selected by RD Bits 14 and 15, is active from the time the Line flip-flop sets until DST resets. The control line is dropped early so that the data lines remain active for at least 100 nanoseconds after the control line. When the Line flip-flop sets, the False Sync delay starts. When a Sync returns (SYN0) or a False Sync is generated, the DST flip-flop toggles reset followed at DCL1 by the Line flip-flop. The DIO flip-flop latches the occurrence of a False Sync until the Line flip-flop resets. See Figure 14.

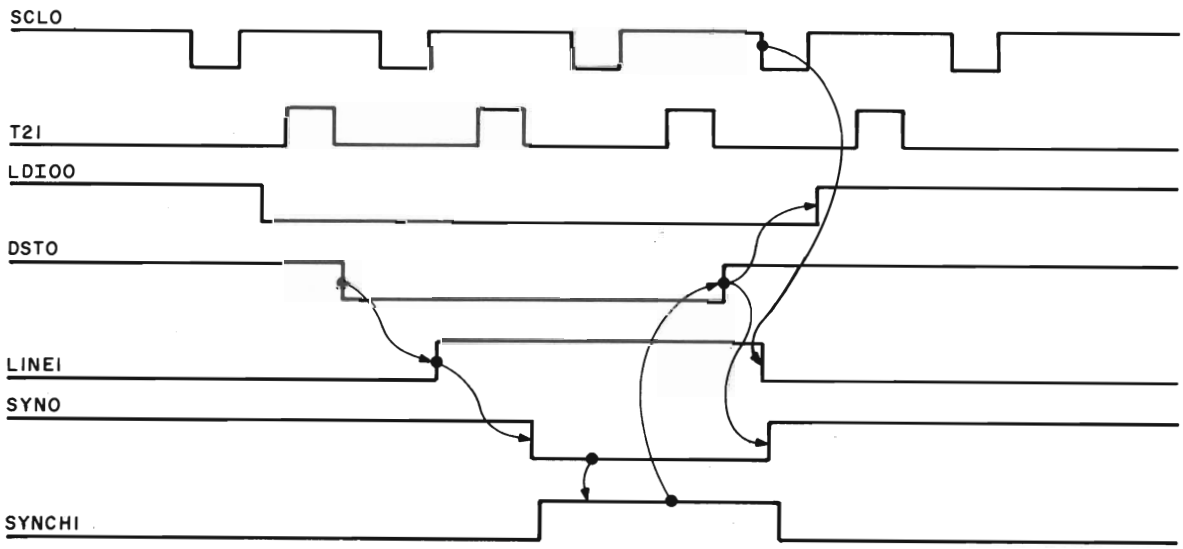


Figure 14. I/O Timing (Output)

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3.10.3 Halfword I/O. Special device controllers that make use of the 16-bit I/O data bus activate the Halfword (HW0) test line while they are addressed.

NOTE

Data Channel devices must not activate the Halfword test line (HW0).

The HW0 line has no affect on the Input/Output sequencing described above. NOCS0 forces Cross Shift (CS1)(8M9) to be false so that X0 is high and no Cross Shift can occur. Also, RAL Bit-14 is forced set by SRAL140 at 5H5. This results in a skip of two micro-instructions, unless RAL14 is already set.

Data should only be exchanged with halfword devices with the RH, RHR, WH and WHR user instructions. Only on these instructions has the firmware been purposely aligned to take advantage of the skip on Halfword I/O.

4. MEMORY INTERFACE

4.1 General Description

The memory interface consists of data, address, timing, and control lines which provide the communication path between the memory modules, the Processor, and the Direct Memory Access (DMA) ports. Up to four Direct Memory Access devices plus the Processor may be connected to the memory via the memory interface.

The timing and control circuits for the memory are contained on the Memory Control mother-board. The logic for controlling the memory parity and the Memory Protect controller is also included on this board; although these features are optional, the basic circuits are always provided. The memory may be expanded up to 32K 16-bit words with no modification to the existing control circuits.

The Data and Address Registers are OR tied to the Memory Bus. They are contained on the Memory Control mother-board and are dedicated for Processor memory operations. The timing and control logic is shared by all the devices using the memory. All busses are of the false type (low active). That is; an active bit is 0 to .4 VDC and an inactive bit is 2.4 to 5.0 VDC.

4.2 Functional Analysis

4.2.1 Memory Address Registers. The Memory Address Register (MAR) shown on Sheet 25, is a double rank register consisting of four 19-030 four-bit shift registers (MAR), and four 19-027 quad latch circuits, the Memory Address Slave Register (MAS). The shift registers are permanently tied in the parallel load mode. These registers are loaded on the trailing edge of DCL0 when LMAR0 is present. MAR may be unloaded to the B Bus via the eight 19-038 multiplexors shown on Sheet 29. The MAS Register follows the MAR whenever the memory is not in use. This is accomplished by holding the clock on the MAS latch circuits high except when MB1 or PMBY1 are active (25A1). MB1 and/or PMBY1 are active throughout the memory cycle. See Figure 15. It is therefore possible that the MAR holds information different from that in the MAS Register. The outputs from the MAS Register (MA000:140) are gated to the Memory Address Bus any time PSEL1 and PSEL1A are active (25H7). When a Direct Memory Access device captures a memory cycle, PSEL1 and PSEL1A are inactive, inhibiting the MAS Register outputs to the Memory Address Bus.

Memory Address Bits MA000, MA010, and MA020 are inverted and assigned to back panel pins. The true and false sides of these memory address bits are used to define the active memory module. The memory positions on the back panel have pre-wired slots to accept eight memory modules.

In addition to the Memory Address Bus, the seven most significant bits of the MAS Register (25A-G6) are brought out via connector three, where they are available for the Memory Protect controller option.

4.2.2 Memory Data Register. The Memory Data Register shown on Sheet 26 is a 16-bit register which can be loaded from the S Bus or the Memory Bus. Its outputs can be unloaded to the B Bus or the Memory Data Bus. When the MDR is loaded from the S Bus, data is toggled in on the falling edge of DCL1. The gating provided allows three different modes to load the MDR. If the micro-code specifies no Cross Shift operation, the entire 16-bits on the S Bus are loaded into the MDR. This is accomplished by the inactive Cross Shift (CS1)(26A1) which allows the clock DCL1 to appear at all toggle inputs. If a Cross Shift operation is specified, either the least or the most significant byte is loaded without changing the remaining byte. The state of X1 (26A1) determines which byte is loaded. X1 is generated on Sheet 9 and is active if Memory Address Register Bit-15 is inactive. An active X1 loads the cross shifted S Bus Bits 8:15 (on S Bus 0:7) into the MDR 0:7, thus only the left-most byte at the specified 16 bit memory location is changed. If X1 is inactive (MAR15 active), the cross shifted S Bus Bits 0:7 (on S Bus 8:15) are loaded into the MDR 8:15, thus only the odd or right-most byte is changed.

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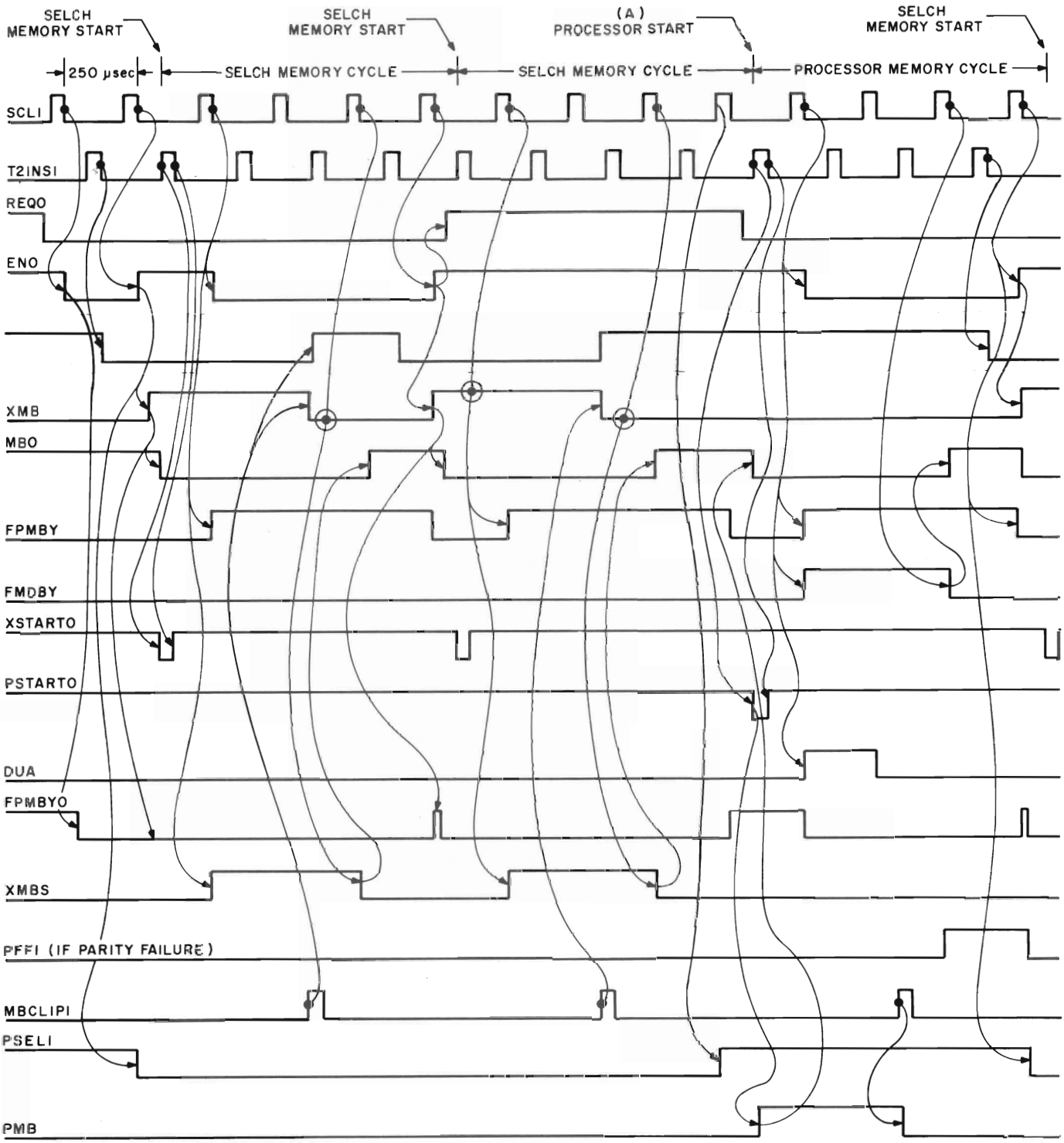


Figure 15. Memory Interface Timing Diagram

When a Memory Read operation is specified by the micro-code, the MDR is loaded directly from the Memory Bus (MS). In this case, READ1 (26A1) and PSEL1A (26B1) are true and the single rail MS Bus is gated to the direct set inputs of the MDR. MDR is cleared prior to memory data being strobed to the MS Bus by the gate at 26A2. Data Unavailable (DUA1) and READ1 (26A1) are both true during the Clock pulse (SCL1) that follows a Processor initiated Memory Read operation. MDRCLR0 goes active clearing the MDR. The memory access time is approximately 300 nanoseconds thus memory data appears on the MS Bus between the two Clocks pulses (SCL1) following a Processor memory start.

4.2.3 Memory Control Circuit. The memory control circuit shown on Sheet 30 consists of two sets of control flip-flops, one set is used when a DMA device captures memory, the other is used when the Processor captures memory. Figure 15 indicates the control sequence.

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Assume that a Selector Channel requests a memory cycle. REQ0 (30L1) is activated and on the falling edge of the Clock pulse (SCL1), the EN flip-flop toggles set and EN0 to the channel drops. The EN flip-flop also prevents the Processor from starting memory, by holding PSTART0 high and FPMBY0 low. An active EN1 is applied to the J input of the AXMBY flip-flop. On the falling edge of the next T21NS1, AXMBY0 goes active and maintains FPMBY0 low after EN0 resets. FPMBY0 is used primarily to stop the clocks.

When the EN flip-flop is set, the SELCH is guaranteed the next memory cycle. If memory is not busy, the EN flip-flop is cleared on the next SCL1. This causes the XMB and PSEL flip-flops to toggle set, allowing the memory to be started on the next occurrence of T21NS1 and deselecting the Processor registers. The Selector Channel may continue requesting memory and capture succeeding cycles under control of the EN flip-flop. On the Clock pulse following the start of the memory cycle, the FPMBY and XMBS flip-flops toggle set assuring FPMBY0 to the Processor and setting up conditions for a graceful completion of the memory cycle. MBCL0 is activated from the memory timing pulse generator. The rising edge of MBCL0 triggers a one shot, the output of which produces the CLMF0 pulse. This pulse falls between the second and third SCL1. CLMF0 is of sufficient width to reset the AXMBY, XMB, and PMB flip-flops. With XMB reset, the J-K inputs to XMBS are low and high respectively. On the third SCL1 after memory start, XMBS toggles reset and MB0 becomes inactive, allowing EN and the FPMBY flip-flop to be cleared on the fourth SCL1. If the Selector Channel is not requesting a second cycle, MNB1 is high before the fourth SCL1 occurs. On the leading edge of SCL1, PSEL is cleared and the Processor is free to start a memory cycle via PSTART0.

For a CPU memory cycle (PSTART0), the sequence of events is similar to the Selector Channel memory cycle except that the DUA flip-flop is set for one system clock period following CPU memory start. The DUA flip-flop prevents the unloading of the Memory Data Register prior to memory readout which is in the order of 300 nanoseconds from memory start.

4.3 Memory Timing Pulses

The memory timing pulses, ER0, LR0, INH0, and W0 are generated on the Memory Control mother-board and are used to drive the memory modules. Figure 16 provides the waveforms for a memory cycle. A memory cycle is initiated by XSTART0 or PSTART0. These signals enable an oscillator and direct set a flip-flop. The set state of the flip-flop enables toggle pulses to the A, B, C, D, and E flip-flops.

A, B, C, and D are connected as a 2n state shift register in which only one flip-flop changes state on any toggle pulse. Initially, these cells and the E flip-flop are in the cleared state. When a memory cycle is initiated, the first toggle pulse sets A, the second B, the third C, and the fourth D. With all flip-flops set, the J input to A is low and the K is high. On the fifth pulse, A is reset, the sixth, B etc. until all flip-flops are in their initial cleared state after the eighth toggle pulse.

The E flip-flop is in the reset state during the read portion of the memory cycle and set during the write interval. E toggles if C is reset, and D is set.

The flip-flop which enables the toggle pulses has its J input grounded. The K input goes high when E and D are set and C is reset. In this interval, the toggle resets the flip-flop and the toggle signals are disabled until another memory cycle is initiated.

Note that the period of the oscillator must be 60 nanoseconds, and therefore the memory pulses are multiples of the oscillator period.

4.4 Parity Check Circuit

The parity control circuit is shown on Sheet 27. Parity is generated on each Write operation and is checked on each Processor initiated read cycle. The Exclusive OR circuits at locations 27R1-5, are tied directly to the Memory Data Bus and statically generate GMD160 which is low if the bus contains an even number of active bits. If a memory read cycle is initiated by the Processor, the Read flip-flop at 27R9 is set. This allows the MS Bus, including the parity bit, to be gated to the Memory Data Register. Bit-16, the parity bit, is loaded into the flip-flop at 27J1. The register is cleared on the start of each cycle by ER0. If the generated parity bit (GMD160) is the same as the received parity bit (MS160), the Parity Fail signal (PFF1) at 27J9 remains inactive. The signal PFF1 will be active on a failure for one clock period during the memory cycle where READ1, PAR0, PMBY1, and FPMBY1 are active and FMDBY0 is high. See Figure 15. Note that non-parity memory modules, when accessed, hold PAR0 high which disables the parity fail gate.

The parity bit written to memory during the restore portion of the memory cycle is generated by the check circuit on a write cycle. On a read cycle, the received parity bit is returned to memory. The circuits at 27B3 control this operation. The signal WRT0A presented by a Selector Channel, is active when the Selector Channel is writing.

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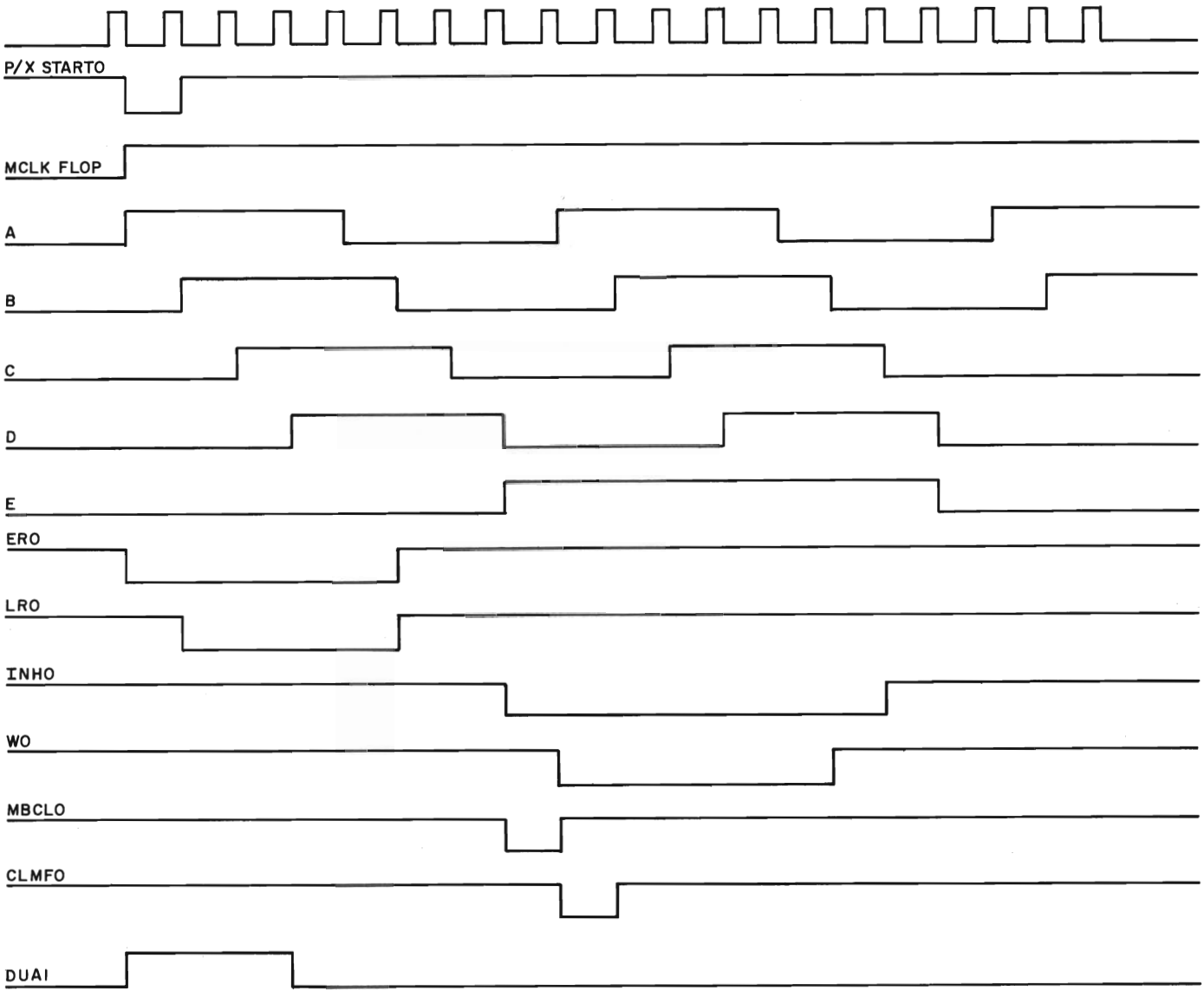


Figure 16. Typical Memory Cycle.

4.5 Memory Protect

Memory Address Bits 00:06 from the Processor Address Register, are presented to the optional Memory Protect Controller. Note that this provides for protection only on Processor initiated Write operations. If PSW Bit-7 is set, indicating the protect mode, the signal, PRTECT0, is sent to the controller at T21NS1 when FPMBY0 is inactive. The controller, if it recognizes a protected address, returns with the Change Write to Read signal (CWR0) which sets the Read flip-flop and allows the MS Bus to be gated to the Memory Data Register, thus creating a read cycle.

5. DISPLAY SYSTEM

The Display System provides a means for reading the contents of all the system registers and any core memory location, together with the capability of manually entering data and programs. Figure 17 shows the Control Console layout. Two register displays are provided. Sixteen switches provide a means for entering memory data and addresses into the machine. The momentary EXEcute control switch requests that any operation, selected by the 12 position rotary Function switch and the SGL and RUN function switches, be executed. The Initialize (INT) control switch resets the system and peripherals. The LOCK-ON-OFF key operated security lock switch, controls power to the system and permits locking the controls. The Control Console is an input/output device interfaced with the Multiplexor Bus. The Display System is supported by a special micro-program sequence in the Read-Only-Memory. The Control Console operating procedures may be found in the Model 70 User's Manual, Publication Number 29-261.

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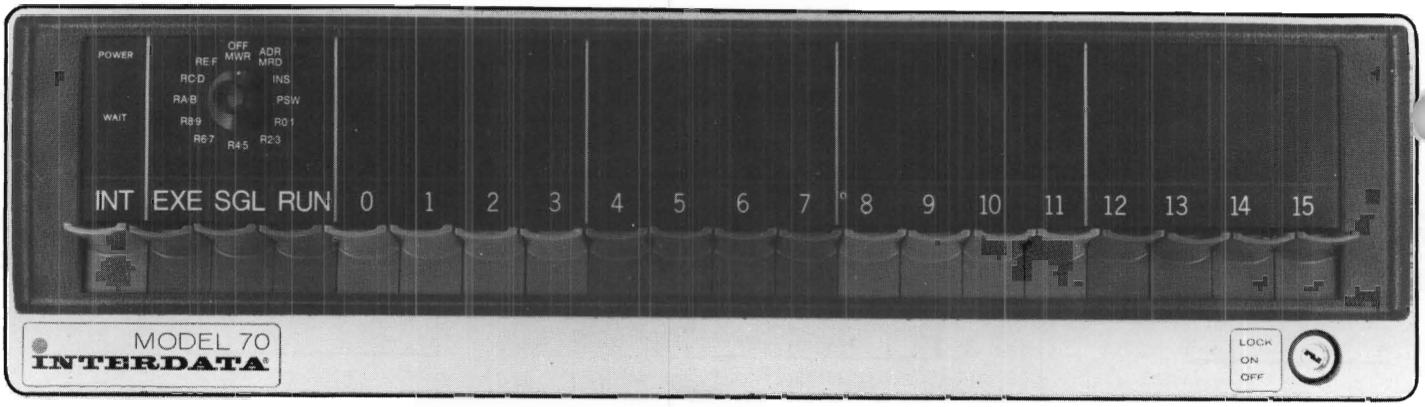


Figure 17. Control Console

5.1 Block Diagram Analysis

Refer to the block diagram on Figure 18. The Processor Multiplexor Bus is shown on the left, the Display System device controller is shown in the center, and the Control Console is shown on the right side.

The address logic is shown in the upper left area of the block diagram. On receiving a request for service via the EXEcute switch and the CATN signal, the Processor outputs the eight-bit display address (X'01') on Data Lines D08:15. This is followed by the ADRS control line which causes the decoded address to be strobed into the Address Storage flip-flop. The set output from this flip-flop enables all other I/O commands into the display controller logic.

Data to the Control Console is transmitted one byte at a time. The first byte is output on Data Lines D08:15, and the Data Available (DA) control line is raised. This command causes the first byte of data to be strobed into Bits 8 through 15 of Display Register Two. The DA line is then dropped, and the two-stage byte counter is incremented. The second byte of data is then placed on Data Lines D08:15, and the DA activated again. This process is repeated four times. Each time the display is addressed, the byte counter is automatically reset to zero for the first byte of data.

Data from the Input Register data switches is read into the system one byte at a time via Data Lines D08:15. On raising the Data Request (DR) control line, Bits 8 through 15 of the data switches are read into the system. The DR command is then dropped and the one-stage byte counter is toggled, enabling the second byte of data. The DR control line is again activated and Bits 0 through 7 of the data switches are read. The one-stage byte counter is automatically reset when the display is addressed.

The status of the control and register switches is read into the system as a single byte of encoded data by raising the Status Request (SR) control line. The twelve positions of the register display rotary Function switch are encoded into Bits 4:7 of the status byte and the Control switches are encoded into Bits 0:7. The status byte is read into the system on Data Lines D08:15. The 32 register display lamps and the 16 data switches may be I/O programmed by the user. An Output Command (OC) instruction causes the CMD control line to set a flip-flop that disables the byte counters from being reset when the device is addressed.

The control logic is shown on the bottom of the block diagram. Depressing the EXEcute switch sets a flip-flop in the console attention control logic (21N7). This generates a CATN signal to the Processor. On receiving CATN, the Processor addresses the display, which in turn resets the flip-flop.

The Single switch (SGL) causes the Single control line (SNGL) to go active after the EXEcute switch is depressed to signify the Single Step Mode of operation to the Processor. A user instruction is executed each time the EXEcute switch is depressed. The Initialize (INT) switch causes the resetting of the Processor, Display Panel and all I/O devices.

5.2 Addressing Logic

Refer to Sheet 21. The Control Console's device number is decoded from Data Lines D08:15 by the eight-input NAND gate at 21L3. The Address flip-flop (ADR)(21L5) toggles set on the falling edge of ADRS1. When the display is addressed, ASYN0 goes low (21B4). ASYN0 generates a return Sync, SYN0 on 23G8.

If the Command flip-flop at 21A2 is reset, SCLR0F goes low to reset the two-stage byte counter at 21D3 and the one-stage byte counter at 21A6.

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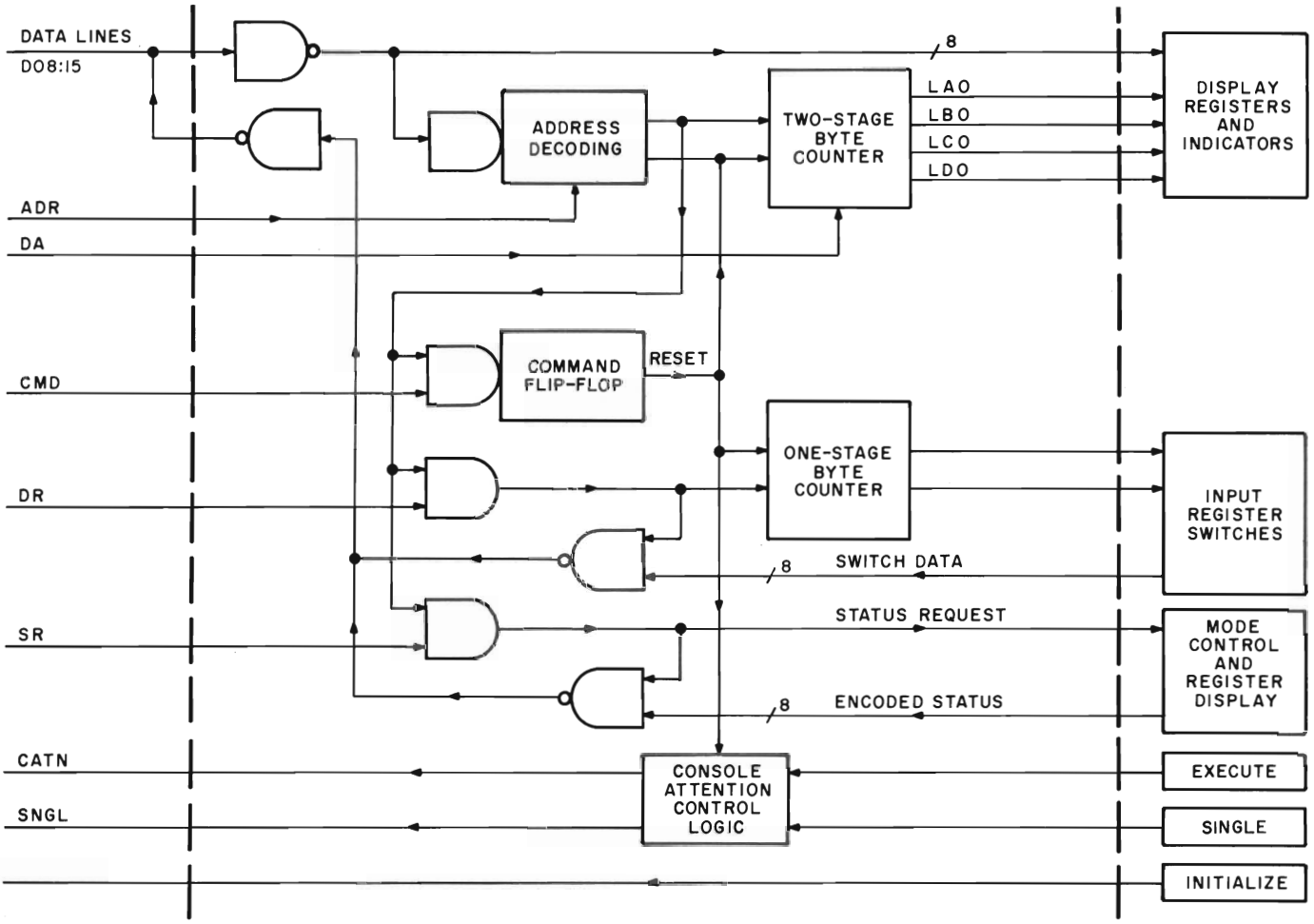


Figure 18. Display Controller Block Diagram

5.3 Data Output

The two-stage byte counter at 21D3 is set to zero on Initialize (SCLR0), on an Output Command to the display (21D8), or when the display is addressed in the Normal Mode. The state of the two-stage byte counter, the Data Available lead (DA1), and the set output from ADRS are input to the 19-032 one-of-ten decoder. The outputs LA0, LB0, LC0, and LD0 correspond to the four states of the byte counter and enable the four bytes of the two display registers. The display registers are shown on 09-051D08, Sheet 2.

The DA0 control line causes Data Lines D08:15 to be gated onto the bi-directional SD00:07 Bus (GSD1A)(21K6). On 09-051D08, Sheet 2, LA0 gates SD00:07 into Display Register 2, Bits 08:15. LB0 gates the SD Bus into Display Register 2, Bits 00:07. LC0 gates into Display Register 1, Bits 08:15. LD0 gates into Display Register 1, Bits 00:07.

The GSD1A lead is delayed from the DA0 line so that the LX0 line will drop before the SD Bus drops. The trailing edge of the gated Data Available (DAG1 at 21C9) increments the two-stage byte counter.

5.4 Data Input

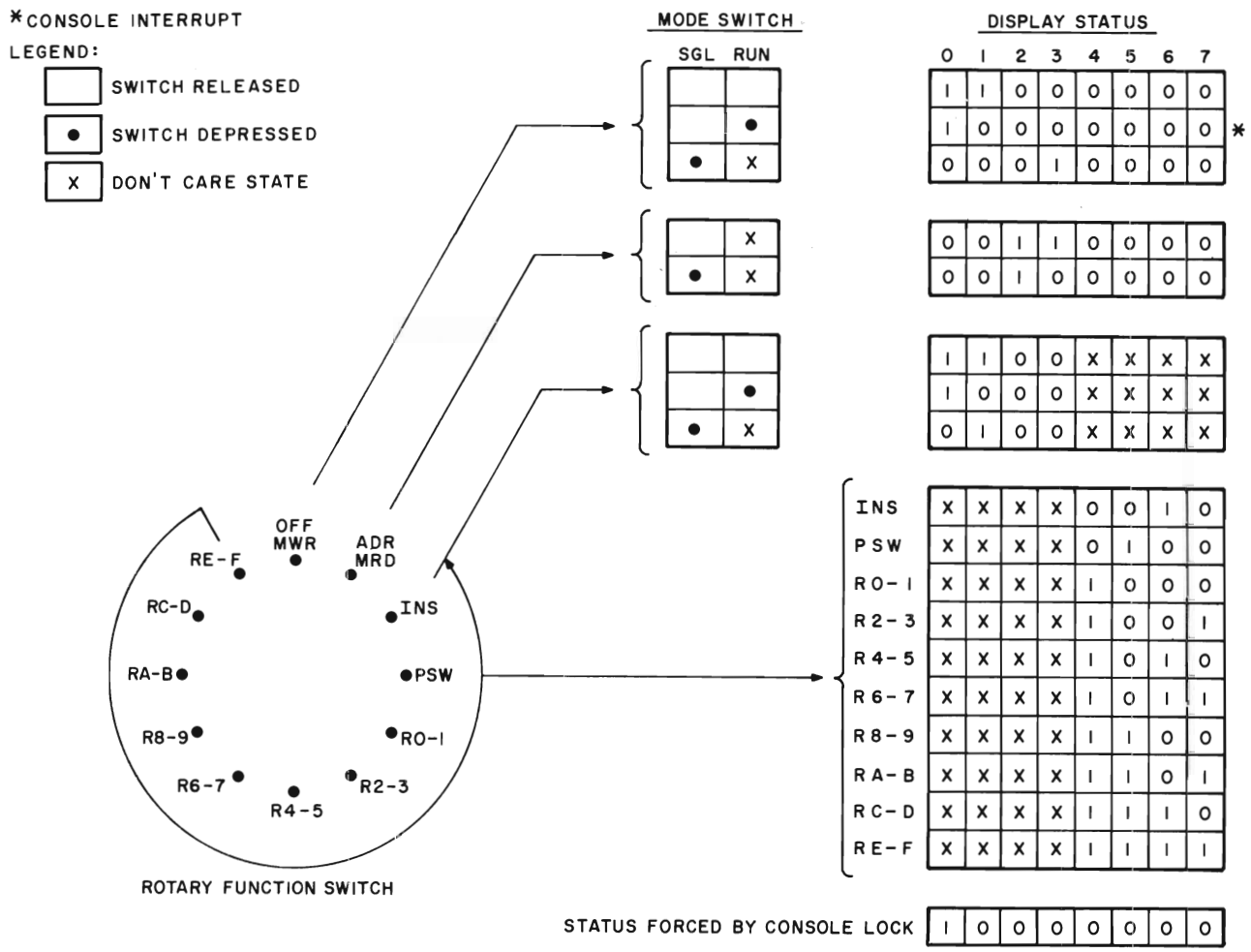
The one-stage byte counter at 21A6 is cleared by SCLR0F on Initialize, Output Command, or when the display is addressed while in the Normal Mode. When the Data Request control line (DRG1) goes high, the least significant byte enable goes high to gate Bits 8:15 of the data switches onto the SD 00:07 lines. (The switches are shown on Sheet 2 of 09-051D08.) When the DRG1 line goes low, the flip-flop at 21A6 toggles set. The next time DRG1 goes high, Bits 0:7 of the data switches are gated onto the SD00:07 lines. DRG0 generates STRB0 (24G5) which gates the SD00:07 lines through the 19-038 dual four-to-one line multiplexors onto Bits 8:15 of the D Bus.

5.5 Status Input

The status byte encoding is shown on Sheet 1 of 09-051D08. The register display rotary Function switch is encoded into the least significant four bits of the status byte. The Control switches, SGL and RUN, in conjunction with the first two positions of the rotary Function switch, OFF/MWR and ADR/MRD, form the most significant four bits of the status byte. The status byte is gated onto the SD00:07 lines by the SRG0 lead. SRG0 generates STRB0 to gate the SD00:07 lines onto Bits 08:15 of the D Bus. Table 3 lists the status codes for the switch positions.

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TABLE 3. DISPLAY STATUS BYTE ENCODING.



5.6 Control Logic

The EXEcute switch outputs, ESNO0 and ESNC0, are latched in the RS flip-flop at 21N4. The differentiated output sets the Console Attention flip-flop (CATN) at 21N7. This flip-flop is reset by ADSY0 when the Processor addresses the display.

When the SGL Control switch is latched and the rotary Function switch is in a position other than OFF/MWR or ADR/MRD, the SSGL1 lead is high. When EXEcute is depressed, the SNGL flip-flop toggles set. SNGL resets when SSGL1 is low and EXEcute is depressed.

6. TELETYPE CONTROLLER

The built-in Teletype device controller is used to interface an ASR/KSR 33 or 35 Teletype to the Processor. It converts serial eight level ASCII code (see Figure 19) to a parallel form for processing by the computer.

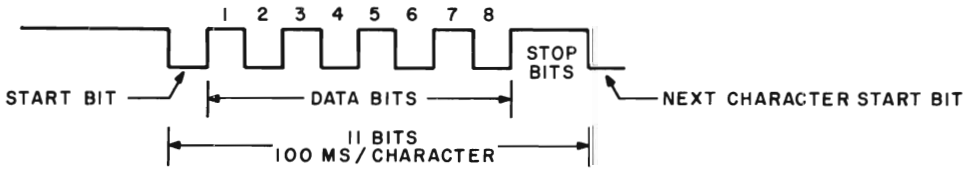


Figure 19. Serial ASCII Code U (Even Parity)

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6.1 Block Diagram Analysis

Figure 20 is a block diagram of the Teletype controller. The control circuits consist of Command flip-flops (Read or Write, etc), circuits to direct the flow of information (Teletype Terminal to/from Processor), and the circuits to control the timer when transmitting/receiving to/from the Teletype Terminal.

The serial information received from the terminal, is sampled by the timer and strobed into the Shift Register. When the entire character has been shifted in, the data is placed in a byte Buffer Register from which the Processor takes the parallel data. When transmitting to the terminal, the information is placed directly in the Shift Register and then shifted out (serially) to the terminal.

6.2 Multiplexor Bus Communication

Communication between the Processor and the Teletype controller is via the low order eight bits of the D Bus. The bus receivers are shown on Sheet 22. The Data Lines D08:15 are buffered to form the DAL 00:07 leads. The device address, X'02', is detected by the gate at 22G1. On the trailing edge of ADRS1, the Address flip-flop toggles set, enabling the other control lines.

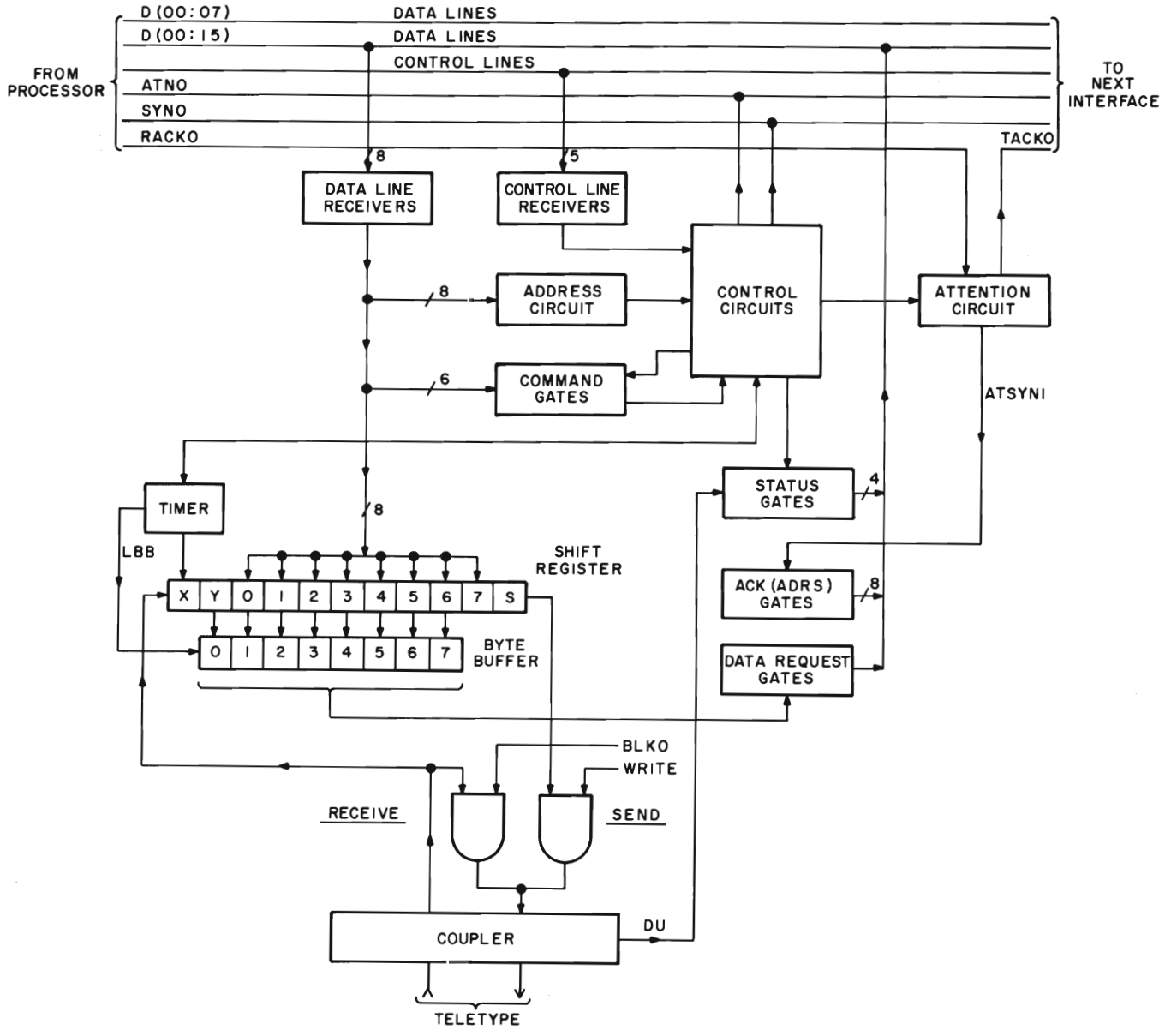


Figure 20. Teletype Controller Block Diagram

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6.3 Data Output

The interface is conditioned to the Write Mode by an Output Command with D Bus Bit-12 set. The Read flip-flop at 22R5 resets. When the Data Available line (DA0) goes low, DAG0A (23B6) and TDAG0 (23B6) go low. DAG0A causes the 19-035 four-bit counter at 23M7 to be loaded with a '5'. TDAG0 resets the RDY flip-flop at 23E3. The two Stop Bit flip-flops (STP)(24D4) are set, the Start Bit flip-flop (STRT)(24E3) is reset and the data to be output (on DAL 00:07) is loaded into the two 19-030 four-bit shift registers (Sheet 24). When the DA0 control line is removed, the TMG flip-flop (23G4) toggles set. As soon as TMG sets, the oscillator at 23K1 starts. The CLK1 output (23M1) is a 300 nanosecond pulse occurring every 2.27 milliseconds or 440 Hz. CLK1 steps the two-stage counter (C1 and C2) to divide the frequency by four. Thus, the TDR0 signal at 23L5 is a 300 nanosecond pulse occurring every 9.09 milliseconds. Each pulse increments the four-bit counter at 23M7 and, as long as the counter does not equal all ones, shifts the 11 bit Shift Register (Sheet 24) left one position. The Counter counts up from 5 so that by the time it equals 15, the Shift Register has shifted ten places.

The DRS0 lead from the least significant bit of the Shift Register is gated with READ0 and TMG1 at 22C7 forming the TRNS0 lead to the Teletype.

When the Counter increments from all ones to all zeros, the Carry Output (EOC0) goes low. EOC0 clears the TMG flip-flop stopping the oscillator.

While TMG is set, BSY1 is high (23S9) indicating that the interface is busy serializing the eight bit character sent to it. See Figure 21.

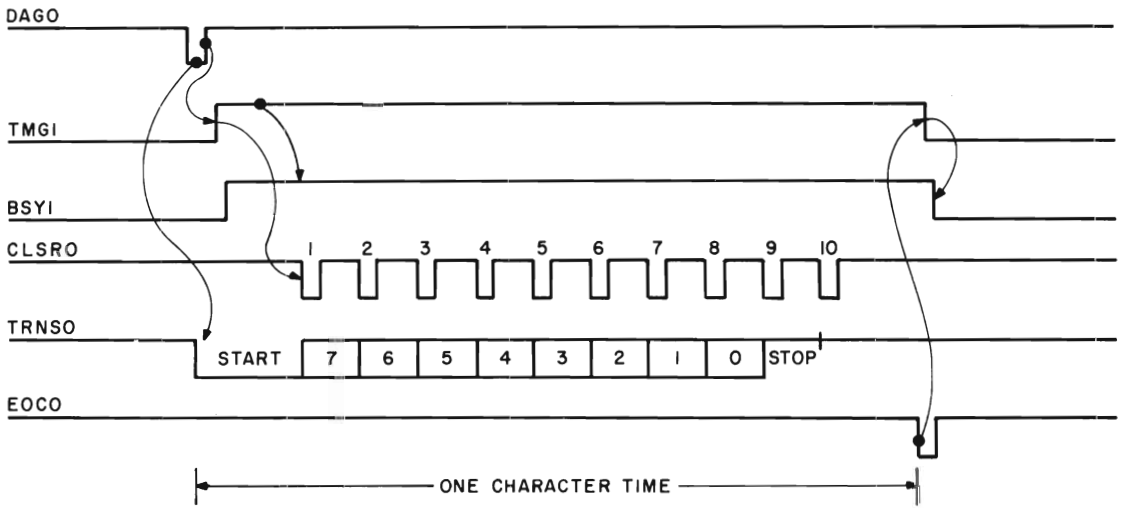


Figure 21. Write Timing

6.4 Data Input

The interface is conditioned to the Read Mode by Initialize or by an explicit Output Command with D Bus Bit-13 set. The Read flip-flop (22R5) is set. In the Read Mode, the interface remains busy (BSY1=1) until a complete character is received from the Teletype. The data input line (DD0)(22F8) is quiescently high. When the Teletype starts to transmit a character, the DD0 line goes low for one bit period, 9.09 milliseconds, to signify the start of a character. Following this start bit are eight data bits and at least two Stop bits. See Figure 22.

DD0 causes the RDY flip-flop at 23E3 to momentarily set. This transition is differentiated to produce the ST0 pulse (23G4). ST0 sets TMG, clears RDY, and loads the four-bit counter at 23M7 with '5'. When TMG sets, the oscillator at 23K1 starts. After 4.5 millisecond, the first TDR0 pulse occurs. TDR0 produces CLSR0 which shifts the state of the DD1 line into the 11-bit Shift Register (24D1). The first bit that shifts in is the start bit that started the timer. After ten shifts, the start bit will be in Bit-7 of the Data Register. The EOC0 pulse generates LBB1 (23R6) to clock the eight bits from the Shift Register into the byte buffer (24G1).

The signal BSY1 is high until the LBB1 pulse toggles the BSY flip-flop at 22L2 set. When the Processor takes the data from the byte buffer, the signal DRG0A clears the BSY flip-flop at 22L2 and BSY1 again goes active.

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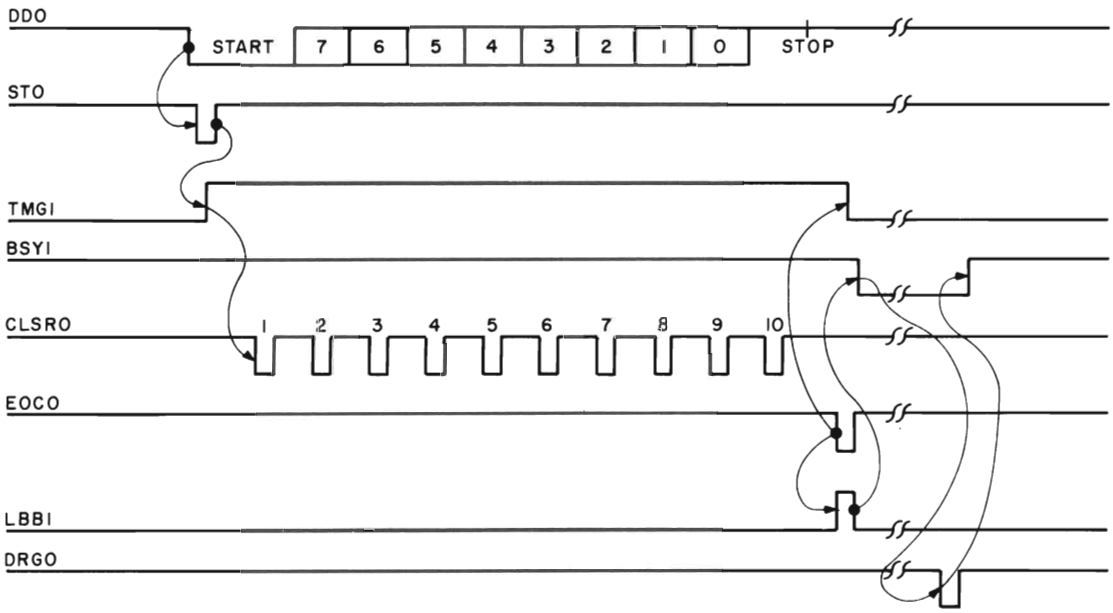


Figure 22. Read Timing

6.5 Status and Commands

The interface is initialized to the Read Mode and is consequently busy until a character is processed. If another character is processed before a Data Request is received, the ERR flip-flop (22M2) toggles set to indicate the overflow condition.

The Block Command sets the BLK flip-flop (22L4). In Block Mode, serial data received from the Teletype is not echoed back. In the Unblock Mode, serial data received is turned around by the gate at 22C8 and transmitted back to the Teletype.

In the Write Mode, the interface is busy only for the time that TMG is set.

The Device Unavailable status bit (DU) is active when the Teletype is off-line or powered down. The DU network on Sheet 22 senses the open circuit condition from Pin 10 of the stub cable and raises the DU1 lead.

The Break status occurs when a Stop Bit is not received from the Teletype. When the EOC0 pulse occurs, the input data line should be high to set the RDY flip-flop (23E3). If TMG resets, and RDY did not get set, the BRK1 signal at 22D9 goes high.

Teletype status is gated onto Data Lines D08:15 by the 19-038 Dual four-to-one line multiplexors on Sheet 24, when the ADRSA1 and ADRSB1 gating leads are both low. These leads are generated at 23F6 as follows:

	ADRSA1	ADRSB1
TTY Status Request	0	0
TTY Interrupt Acknowledge	0	1
TTY Data Request	1	0
Display Data Request	1	1
Display Status Request	1	1

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TABLE 4. TELETYPE STATUS AND COMMAND BYTE

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE	ERR		BRK		BSY	EX		DU
COMMAND BYTE	DISABLE	ENABLE	UNBLOCK	BLOCK	WRITE	READ		

ERR — The Error bit is set when a character is not taken from the controller buffer before another character is assembled.

BRK — The Break bit is set at the end of one character time when the line is held in the space condition for a period greater than a character period.

BSY — Read Mode - The Busy bit is normally set and is reset when data is available for transfer to the Processor. Write Mode - The Busy bit is normally reset and is set when data is being transferred to the terminal.

EX — The Examine bit is set when BRK or ERR is set.

DU — The Device Unavailable bit is set when the terminal is powered down or in Local Mode.

DISABLE — Disables device interrupts; allows queuing of interrupts.

ENABLE — Enables device interrupts.
Note: A command byte with both Bits 0 and 1 set Disarms the interface (no interrupt queuing).

UNBLOCK — Allows Printer to print data entered via keyboard or tape reader.

BLOCK — Disables the Unblock feature.

WRITE — The interface is placed in the Write Mode.

READ — The interface is placed in the Read Mode.

6.6 Interrupt Circuit

The Teletype controller is prevented from queuing interrupts when the Arm flip-flop is reset (24B3). The interface is disarmed by SCLR0 or by the Disarm Output Command. The Arm flip-flop sets whenever an Output Command Enable or Disable is received. If armed, the ATN flip-flop sets whenever an Output Command Enable or Disable is received. If armed, the ATN flip-flop (24B7) also sets on the negative going transition of BSY1. If EBL is also set (24B8), the ATN0 lead at 24C9 goes low.

The Processor responds to an ATN by executing an Acknowledge Interrupt. The ACKA000 lead (20N6) goes low. This lead is connected to the RACK0 input (24A1) to the Teletype controller if the Teletype is to be first in priority. When RACK0 goes low, if ATN and EBL are set, the signal ATSYN0 goes low. If either ATN or EBL is reset, the TACK0 lead to the next device controller in the daisy chain goes low.

ATSYN0 toggles the ATN flip-flop reset and gates the Teletype's device number onto Data Lines D08:15, by way of the DAL 00:07 inputs to the 19-038 multiplexors on Sheet 24.

7. MAINTENANCE

This section describes maintenance procedures which may be used to check and, if necessary, adjust the Processor.

7.1 Clock Timing

There is only one adjustment associated with the system clocks. The variable Capacitor C9 on the I/O mother-board is very stable and should not require field adjustment. The adjustment should only be changed after the test indicates that it is out of tolerance and there are no faulty components in the system.

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1. Force the RD Register to all ones by grounding the DISR0 signal at Pin 217-1 on the ROM board and depress the Initialize switch.

NOTE

Exercise care in grounding points in the digital system as some components may be damaged if the wrong pins are grounded.

2. Use an oscilloscope to check that the period of the SCL0 at Pin 211-1 on the I/O mother board is 250 nanoseconds. Adjust Capacitor C9 to get the 250 nanosecond period. The pulse width is dependent on a decoded state of the clock counter. Check the associated logic if there is a discrepancy.

3. Check that the following system clocks occur at the same time as SCL0:

DCL0	121-0
RCL0	225-1
RDSTB0	228-0

If a discrepancy occurs, check the associated logic.

4. Check that T21 and T21NS1 occur approximately 60 nanoseconds after the rising edge of SCL0 and last for approximately 60 nanoseconds. These clocks are available on the I/O mother-board at Pins 229-0 and 123-0 respectively. These clocks are also decoded states of the clock counter.

5. Check that T2SYS1 on the ROM mother board (12-087) is a 30 nanosecond pulse occurring during T21.

6. Check that STCLK1 is a 30 nanosecond pulse occurring during DCL0 and approximately 25 nanoseconds after the falling edge of DCL0 (06-107 on the ALU mother-board).

7. Remove the ground from Pin 217-1 on the ROM back panel.

7.2 Memory Timing Adjustments

Refer to Figures 15 and 16. Timing adjustments are checked by grounding Console Attention (CATN0), Pin 238-1 on the I/O Control Board at Position 05 in the Processor chassis. The Control Console rotary Function switch should be placed in the Memory Read (MRD) position with the Single (SNG) switch depressed. Sync may be obtained from the START1 Test Point on the Memory Control board at Position 04 of the Processor chassis.

The E flip-flop Test Point F on the memory control board should be set for 480 nanoseconds. The adjustment for this is the trimmer capacitor in the memory pulse generating oscillator. After adjustment, remove the ground from CATN0.

This adjustment is performed at the factory and no field adjustment should be required.

7.3 Teletype Controller

Refer to the vendor operating and service manuals for maintenance information on the terminal being used. The overall operation of the terminal and interface can be checked by running the 06-004 test program.

The only adjustment on the Teletype controller is the potentiometer (R63) on the oscillator. A check of the timing can be made as follows:

1. Initialize the interface.

2. Connect an oscilloscope to C21, Pin 6 of IC 14
   Vertical scale: 2 volts/centimeter
   Horizontal scale: 10ms/centimeter

3. Generate a continuous stream of data from the terminal by tape or by the REPEAT key function of the keyboard.

4. Adjust the oscillator for the waveform shown on Figure 23.

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7.4 Overall Processor Test

Use the 06-106 Model 5 Test Program to perform a comprehensive test of the Processor.

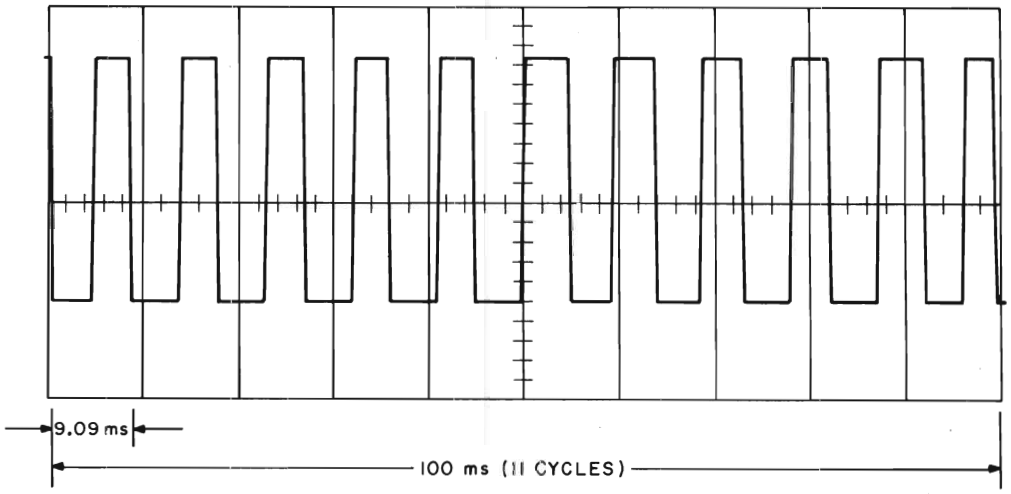


Figure 23. Character Timer Adjustment

8. MNEMONICS

The following list provides a brief description of each mnemonic found in the Model 70 Processor. The source of each signal on Schematic Drawing 01-051D08, is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ABRT0	Abort Phase Two sequence	4N4
ACKA00	Acknowledge Interrupt Control Line	20N5
AD	TTY Address flip-flop	22J1
ADMH1	TTY Address Select	22H1
ADR	Display Address flip-flop	21L5
ADRS0	Address Control Line	20L5
ADRSA1	Display/TTY D Bus gating lead	23E6
ADRSB1	Display/TTY D Bus gating lead	23E5
ALRM131	Data Parity Fail Alarm	17K7
ALRM141	Instruction Parity Fail Alarm	17L7
ARLM151	Early Power Fail Alarm	17N7
AMOD0	Address Modification	9A2
AR00:15	Arithmetic Register	Sheet 12
ARST1	Automatic Restart	18J1

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MNEMONIC	MEANING	SCHEMATIC LOCATION
AST0	TTY Timer Start	23G3
ASYN0	Display Address Sync	21B4
ASYN0A	TTY Address Sync	23B5
ATN0	I/O Attention Test Line	18N1, 24C8
ATSYN0	TTY Interrupt Acknowledge Sync	24B5
B	B Bus	Sheets 11,13, 16,20,29
B130	B Bus Bit-13	4F4
BANK	Bank flip-flop	12M9
BLKDT0	Block Serial Data Transfer	22N4
BRA1	Branch	18H8
BRK1	Line Break	22D9
BSY	Busy flip-flop	22L2
BSY1	Busy	23M9
C1, C2	TTY Time Counter flip-flops	23J4, 23J5
CATN0	Console Attention	21N9
CC121:151	Condition Code Bits 12:15	Sheet 17
CEMT0	Counter Empty	27C9
CG	Gated ALU Carry	Sheet 14
CI1	Carry In	14A5
CL070	Control Line 7	19D5
CLK0	System Clock Oscillator Output	19B6
CLK1	TTY Timer Clock	23M1
CLKOFF0	Clock Off	19B6
CLKSTP0	Clock Stop	19M4
CLMF	Clear Memory flip-flops	30H8
CLR0	Clear Function	9N4
CLRA0	Clear ROM Address Higher	5C3
CLRB0	Clear ROM Address Lower	5B3
CLRBK0	Clear Bank and Utility flip-flops	12K9
CLRIR0	Clear Instruction Register	9A7
CLRST0	Clear Memory Timer	30J3

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MNEMONIC	MEANING	SCHEMATIC LOCATION
CLSR0	Data Register Clock	23R6
CMD0	Command Control Line	20M5
CMDG0	Gated Command Line (Display)	21D9
CMDG0A	Gated Command Line (TTY)	23B8
CMND1	Command	13G7
CMODE	Counter Mode flip-flop	13M8
CP	Propogated ALU Carry	Sheet 14
CRY0	Carry	15A5
CS1	Cross Shift	8M6
CSL0	Command Shift Left	13J8
CSR0	Command Shift Right	13G8
CSV1	Carry Save	14D7
CTEST1	Command Test	17M3
CTF1	Change Test Flags	14S9
CTLT21	Counter is Less than Two	13K7
CTONE1	Counter Equals One	27C9
CTR121:151	Counter Bits 12:15	Sheet 27
CWR0	Change Write to Read	27R9
D	D Bus Bits	Sheets 16,20,24
D1	DO Micro-Instruction	8C5
DA0	Data Available Control Line	20M5
DAG0	Gated Data Available (Display)	21C8
DAG0A	Gated Data Available (TTY)	23B6
DAL	Data Available Lines	Sheet 22
DC0	Data Channel Request	18R1
DCAK0	Data Channel Acknowledge	20K5
DCL0	Destination Clock	19M9
DD0	Device Data (TTY)	22F8
DDC1	DO or Command	8B5
DECTR0	Decrement the Counter	13F8,18E9
DIFF1	Different Signs	17G3

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MNEMONIC	MEANING	SCHEMATIC LOCATION
DISB0	Disable Memory Start	9E8
DISR0	Disable ROM	6A7
DIV0	Command Divide	13J8
DLAYA0	ER0/LR0 Delay	30F4
DLAYB1	ER0/INH0 Delay	30G8
DLAYC1	ER0/W0 Delay	30F8
DR0	Data Request Control Line	20N5
DR001B:071B	TTY Data Buffer Register	Sheet 24
DRD0	Data Channel Read/Write Test Line	18M1
DRD081	DO and RD Bit-8	8J9
DRG1	Gated Data Request (Display)	21C8
DRG0A	Gated Data Request (TTY)	23B7
DRS0	Data Register Start Bit	24E4
DST0	I/O Device Clock Stop	4A4
DT21	Delayed T21	9N5
DTEST0	True Interrupt Test on Phase 2 DO	18M9
DUA0	Device Unavailable	30D4
EBL	Abort Enable flip-flop	4S3
EN	ROM Page Enable	Sheet 6
EN0	External Memory Request Enable	30L4
ENABL1	TTY Interrupt Enable	24E8
EOC0	TTY End Of Character Detect	23M7
EPF0	Early Power Fail	19G3
ER0A	Early Read, memory timing lead	30G4
ER1	Early Read, memory timing lead	30E6
ERR1	TTY Interface Overflow Error	22M2
ESNC0	Execute Switch Normally Closed Contact	21N3
ESNO0	Execute Switch Normally Open Contact	21M3
EX1	Examine Status	22N1
EXES1	Execute Switch Depressed	21N5
EXTCLK0	External Clock Input	19E6

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MNEMONIC	MEANING	SCHEMATIC LOCATION
FAST0	Fast External Interrupt Test Line	18B5
FLR	Flag Register	Sheet 17
FMDBY	Memory Data Register Busy flip-flop	30N4
FMDUA	Memory Data Unavailable flip-flop	30J4
FPMBY	Processor Memory Busy flip-flop	30M4
FRCLOC0	Force Location Counter to be Source and Destination	9J4
FRNS1	Flag Register Bits 14 and 15 Not Set	17N5
FST1	Fast External Interrupt Test Line	18B8
FSYN0	False Sync	4F2
GA	Gated AR Input to ALU	Sheet 12
GB	Gated B Bus Input to ALU	Sheet 14
GCMND1	Clocked Command Micro-Instruction	13L7
GDEST1	Gated Destination Enable	10D3
GDEST1A	Gated Destination Enable	18D2
GDRL0	Gated Data Request Lines (Display)	23B5
GDROM0	Gate DROM Output	9H7
GIO1	Gated I/O Control Line	4A2
GMD160	Gated MD Bit-16	27R5
GMSIR1	Gate MS Bus to IR	28A3
GMSMD1	Gate MS Bus to MDR	26B2
GO	GO flip-flop	19D9
GOBRA0	GO Branch	18H9
GR	Gate Read Register Stack Enable	Sheet 10
GTP20	Go to Phase 2	9D8
GTP30	Go to Phase 3	9G7
GW	Gate Write Register Stack Enable	Sheet 10
HDEST0	Load SRH	8D7
HIDU0	ROM Read Inhibit	8A1
HW0	Halfword I/O Test Line	9K1
ILEG0	Illegal Instruction Detect	8K8
INH0	Inhibit, memory timing lead	30C9

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MNEMONIC	MEANING	SCHEMATIC LOCATION
INHINC0	Inhibit RAL Increment	5R2
INIT0	Initialize Switch	19A4
INTA0	Interrupt Set A	17R9, 18N3
INTB0	Interrupt Set B	18R4
IR	Instruction Register	Sheet 28
IRA1	Clear, Jam, and Alarm DO Option Timing Lead	9M3
JACC0	Jam Alarms to Condition Code	9L4
JCL1	ROM Address Jam Clock	9H7
KILDST0	Kill Destinations	4N4, 13N9
KSKIP0	Reset Skip flip-flop	9F7
LA0	Load Display Byte A	21F9
LARCLK1	AR Loading Clock	12A2
LAR1	Load AR	8F9
LARYS0	Load AR from YS	9C3
LB0	Load Display Byte B	21F9
LBB1	Load TTY Byte Buffer	23N6
LC0	Load Display Byte C	21F9
LCC0	Load Condition Code from FLR	9M4
LD0	Load Display Byte D	21F9
LD01	Load Destination Address 0 (RAH)	18D8
LD10	Load Destination Address 1 (RAL)	18E8
LDIO1	Load I/O	20K3
LDCTR0	Load CTR	8C7
LDCLR0	Load FLR or CLR	17R4
LDFLR0	Load FLR	17S3
LFLR0	Load FLR	8D7
LINE	I/O Control Line flip-flop	4C4
LIR0	Load IR	8D7
LLOC0	Load LOC	8G8
LMAR0	Load MAR	8G9
LMAS1	Load MAS	25A3

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MNEMONIC	MEANING	SCHEMATIC LOCATION
LMDH1	Load MDR High 0:7	26A5
LMDL1	Load MDR Low 8:15	26A7
LMDR1	Load MDR	8F8
LOAD1	Load Micro-Instruction	8D5
LPSW0	Load PSW	8H8
LR0	Late Read, memory timing lead	30E6
LRAH0	Load RAH	18C8
LRAL0	Load RAL	18K9
LSRL0	Load SRL	8D7
LYD0	Load YS, YD or YDP1	8C7
M1	ALU Control Line	13J5
MA	Memory Address Bus	Sheet 25
MALF1	Machine Malfunction	17R9
MAR	Memory Address Register	Sheet 25
MB0	Memory Busy	30M3
MBCL0	Memory Busy Clear	30C4
MBCLIP	Memory Busy Clear Pulse	30C6
MCLR1	Memory Clear Input	30A1
MD	Memory Data Bus	Sheet 26
MD0	Multiply or Divide	13H9
MDR	Memory Data Register	Sheet 26
MDRCLR0	MDR Clear	26A2
MNB1	Memory Enable	30M7
MPY0	Multiply	13H7
MS	Memory Strobe Bus	Sheet 26
MSK1	Mask IR4 and CC Test Line	29R8
MSST0	Memory Contention Clock Stop	4L2
MST0	Memory Contention Clock Stop	4J2
MWPW0	Memory Write or Priviliged Write	8B9
NA0	No AR to ALU	13R4
NOCS0	No Cross Shift	9K3

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MNEMONIC	MEANING	SCHEMATIC LOCATION
NOMEM0	Surpress Memory Read	9E9
OP	Operation Length flip-flop	4L9
OSC1	Oscillator Output	19C8
P00	Phase Zero	9K4
P10	Phase One	9D7
P21	Phase Two	9F4
P30	Phase Three	9G5
PC0	Phase Counter Bit-0	9F3
PC1	Phase Counter Bit-1	9F3
PERR1	Parity Error Detect	27J6
PF0	RAL Increment Internal Carry	5R8
PFDT0	Power Fail Detect	19D4
PFF1	Parity Fail	27J9
PHEN1	Phase Change Enable	9F9
PMB	Processor Memory Busy flip-flop	30R5
POFF0	Power Off (Switch Contact)	19A4
POW0	Command Power Down	19L2
POWDN0	Power Down	19J2
PPF0	Primary Power Fail	19J3
PR5	Pullup Resistor	12N9
PRTECT0	Memory Protect Test	27N9
PSEL0	Processor Selected	30L8
PSTART0	Processor Memory Start	30N7
PSW	Program Status Word	Sheet 29
RA1	User's Stack Read Enable	10H8
RACK0	Receive Acknowledge Control Line	24A1
RACLR0	ROM Address Register Clear	9B7
RAH	ROM Address Higher	Sheet 5
RAL	ROM Address Lower	Sheet 5
RB1	User's Stack Read Enable	10F8
RCL0	ROM Address Clock	19L9

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MNEMONIC	MEANING	SCHEMATIC LOCATION
RD	ROM Data Register	Sheet 8
RDSTB0	RD Strobe	19L9
RDY0	TTY Ready	23E3
READ	TTY Read flip-flop	22R5
READ	Memory Read flip-flop	27N9
REQ0	External Memory Request	30L1
RMA1	Micro Stack Read Enable	10F4
RMB1	Micro Stack Read Enable	10F4
RMS0	Read Micro Stack	10D5
RR0	RR User Instruction	4M8
RS0	RS User Instruction	4M8
RUN	Run flip-flop	8J7
RYD1	Read YD	10A5
RYS1	Read YS	10C5
S	S Bus	Sheet 14
S01, S11, S12	ALU Control Lines	Sheet 13
SCL0	System Clock	13G1, 19J9
SCLR0	System Clear	19N1
SD	Display Status and Data Bus	Sheet 21
SFLR120	Set FLR12 (C)	17D4
SFLR130	Set FLR13 (V)	17G4
SFLR140	Set FLR14 (G)	17J3
SFLR150	Set FLR15 (L)	17L4
SHI0	Input High Data Switches	21A9
SHCA1	Shifter Control Line	12B9
SHCB1	Shifter Control Line	12C9
SHL1	Shift Left	8N6
SHOT1	Bit Shifted Out	13C9
SHR1	Shift Right	8N6
SLO0	Input Low Data Switches	21A9
SNGL0	Single Mode	21H8

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MNEMONIC	MEANING	SCHEMATIC LOCATION
SR0	Status Request Control Line	20R5
SRAH	Set RAH	Sheet 4
SRAL	Set RAL	Sheets 4, 9
SRD	Set RD	Sheets 6, 7, 8
SRDY0	TTY Set Ready	23D3
SRG0	Gated Status Request (Display)	21B7
SRG0A	Gated Status Request (TTY)	23B7
SRH	Shift Register Higher	Sheet 15
SRHM01	SRH Mode Control Lead	15L4
SRHM11	SRH Mode Control Lead	15M4
SRL	Shift Register Lower	Sheet 15
SRLCI1	SRL Carry In	15S4
SRLM01	SRL Mode Control Lead	15R4
SRLM11	SRL Mode Control Lead	15N4
SSGL1	Set SNGL flip-flop	21H7
SSKIP0	Set Skip	9B7
SSMEM1	Solid State Memory Control Line	30J1
ST0	TTY Data Start	23J3
START1	Memory Start	30G2
STBR1	Store or Branch	4N8
STF0	Set Test Flags	8R7
STFL0	Set Test Flags	8R9
STOP0	Clock Stop (Phase Zero)	9C4
STPA0	Memory Contention Clock Stop	4J4
STPC0	MPY, DIV, and RPT Clock Stop	13R9
STPSYS	Stop System flip-flop	19J4
STRB1	Display/TTY D Bus Strobe	23E6
SUB0	Subtract	13K5
SV0	Set V Flag	4F4
SVAC0	Save Adder Carry	8S7, 13B4
SVSC0	Save Shifted Carry	8S6, 13A4

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MNEMONIC	MEANING	SCHEMATIC LOCATION
SYD	Decoded YD Field Bits	Sheet 10
SYN0	System Synchronize	4E1, 23G7
SYNCH0	Receive Synchronize	4D4
SYS	Decoded YS Field Bits	Sheet 10
SYSCL1	System Clock	19E8
T21	Time 2 (Clock)	19J9
T21NS1	Unskipped T21	19K9
T21SY1	T21 and SYSCL1	9A6
TACK0	Transmit Acknowledge	24A9
TDAG0	TTY Gated Data Available	23B6
TDR0	Toggle TTY Data Register	23L5
TEST1	Test Micro-Instruction	18M8
TESTA	Abort Test flip-flop	4M3
TFA	Clock Timer flip-flop A	19G7
TFB	Clock Timer flip-flop B	19G8
TIR0	Toggle IR	28S3
TMG0	TTY Timing Gate	23G4
TP1	Toggle TTY Data Register	23H1
TRA	RAL	Sheet 5
TRNS1	TTY Data Transmit	22C8
TTEST0	True Testable Function	18H5
UDIO0	Unload I/O	18D5
UIR41	Unload IR 08:11	18F3
ULAR1	Unload AR 00:07	13N5
ULAR1A	Unload AR 08:15	13N5
UMDR1	Unload MDR	18C4
USRH0	Unload SRH	18E5
USRL0	Unload SRL	18D5
USTRB0	Unload Register to B Bus	18C5
UT	Utility flip-flop	12L9
W0	Write, memory timing lead	30B9

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MINEMONIC	MEANING	SCHEMATIC LOCATION
WA1	Write User Stack Enable	10S8
WAIT0	Wait flip-flop	8L7
WAIT1	Wait flip-flop	21R4
WB1	Write User Stack Enable	10R8
WMA1	Write Micro Stack Enable	10G4
WMB1	Write Micro Stack Enable	10G4
WMS0	Write Micro Stack	10J5
WRT0A	Memory Write Control Line	27L2
WYD1	Write YD	10H5
WYS1	Write YS	10J5
X0	Conditional Cross Shift	9R9
XMBS0	External Memory Busy (Slave)	30M5
XMBY0	External Memory Busy	30L5
XSTART0	External Memory Start	30L6

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MODEL 70 MICRO-INSTRUCTION REFERENCE MANUAL

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MODEL 70
MICRO-INSTRUCTION
REFERENCE MANUAL

1. INTRODUCTION TO MICRO-PROGRAMMING

The INTERDATA Processor is a very fast micro-programmable machine controlled by a Read-Only-Memory (ROM). Micro-programs in the ROM direct the flow of information within the registers and core storage of the machine. These micro-programs are a sequence of micro-instructions. Each micro-instruction causes one machine function to be executed; such as transferring the contents of one register to another, addition, subtraction, and logical operations between registers; input/output operations; or core memory accesses. Each micro-instruction constitutes one 16-bit word of ROM. The ROM is a high speed, non-volatile, solid-state device organized into pages of 256 words each.

2. THE MICRO-PROGRAMMED PROCESSOR

The Processor is designed to execute micro-instructions stored in a Read-Only-Memory (ROM). Each micro-instruction performs one hardware function. A series of these micro-instructions (a micro-program) can solve highly complex problems. The Micro-Program in the Processor is an emulator. That is, the program completely simulates the instruction set, interrupt handling features, and display functions of a quite different machine. This emulated computer is similar to the IBM 360 family of Processors and has a very powerful instruction set.

Special hardware is built into the Processor to assist the micro-program in its emulation task. When executing instructions of the emulated machine, the micro-program directs the hardware to read the instruction to be performed from core memory. The instruction decoding circuitry then steers the Processor to a micro-subroutine that has been designed to perform the emulated instruction. The loop is then closed by incrementing the instruction location counter and returning to the point that will fetch the next instruction from core memory.

The Read-Only-Memory is a very fast, non-volatile, solid-state device. The Processor is designed to match the ROM's performance, executing most micro-instructions in 250 nanoseconds. The combination of special hardware and micro-instructions running at many times core speed allows most emulated instructions to be executed in the time it takes to fetch them from core.

3. BLOCK DIAGRAM ANALYSIS

Refer to Figure 1 during the following description. Processor operation is controlled by the Read-Only-Memory (ROM). Locations in ROM are addressed by a 12-bit register comprising an 8-bit incrementing address register (RAL) and a 4-bit non-incrementing page register (RAS). RAS is loaded from the "outer rank" page register (RAH) when RAL is loaded.

Information read out of ROM is placed in a 16-bit data register (RD). Bits 0 through 3 of RD are the micro-instruction operation code. The meaning of the remaining bits in RD depends on the particular micro-operation to be performed.

There are three 16-bit general purpose micro-registers labeled MR0, MR1, and MR2. Two additional 16-bit micro-registers, SRH and SRL, are available for general use. SRH and SRL may also be used together as a 32-bit shift left/shift right register for multiply, divide, and double-precision shifts.

The Program Status Word (PSW) is a 16-bit register which indicates the system status relative to the user program being emulated. Bits 0 through 11 of PSW define machine status. Bits 12 through 15, the Condition Code (CC), may only be loaded from the Flag Register (FLR). When PSW is loaded, Bits 12 through 15 of the S Bus are captured in the FLR. This permutes the user status to the micro-code level. The Location Counter (LOC) is a 16-bit appendum to PSW which holds the address of the next user instruction to be performed.

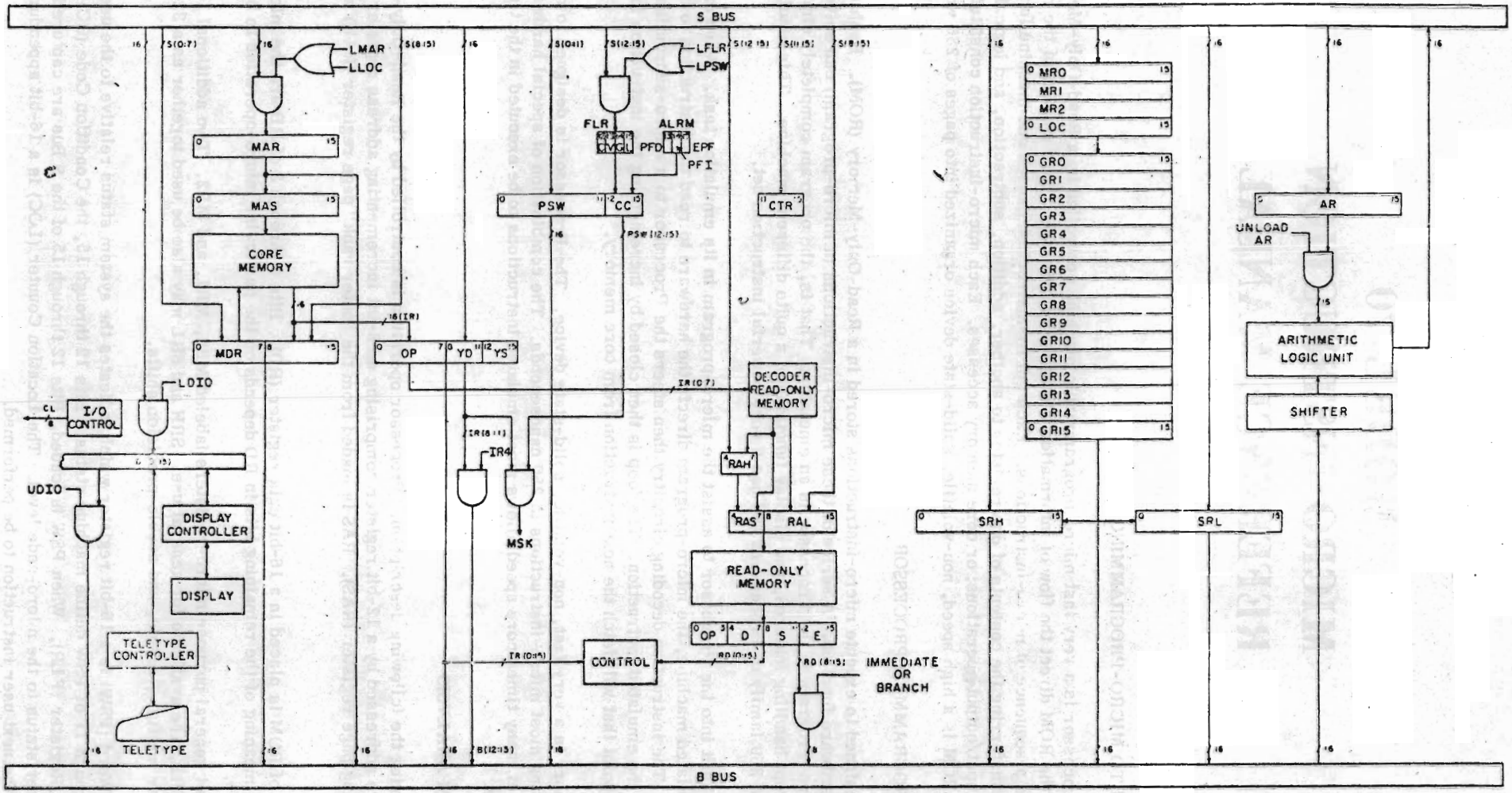


Figure 1. Model 70 Digital System

The Memory Address Register (MAR) is a 16-bit buffer used to address core memory locations. Memory is actually addressed by the Memory Address Slave Register (MAS). When memory is not busy, MAS is automatically loaded from MAR. The 16-bit Memory Data Register (MDR) holds data read from or written into core memory. MDR is separated into two bytes, MDH and MDL, which may be loaded separately for efficient byte handling.

The 16-bit Instruction Register (IR) holds the instruction word of the current user instruction. Bits 8 through 11 may be unloaded to the B Bus Bits 12 through 15 (IR4).

The user's sixteen 16-bit General Registers (GR0 through GR15) are not directly addressable by the micro-program. The General Registers are addressed by IR Bits 8 through 11 (YD) or by IR Bits 12 through 15 (YS). The micro-program can only access the General Registers by specifying the field of IR, YD, or YS, that contains the appropriate General Register address.

The Counter Register (CTR) is a 5-bit decrementing register. It is always initialized to a value of 16; however, it may be preset to any value from 0 to 31 to control the number of repetitions of a single micro-instruction or a sequence of micro-instructions. The Counter is used in the multiply and divide hardware to control the number of shifts.

The 16-bit A Register (AR) holds the second operand for arithmetic and logical micro-operations. It is one of two direct inputs to the Arithmetic Logic Unit (ALU). The other input is the output of the B Bus Shifter. The Shifter can shift B Bus data left or right one position, rotate eight positions, or gate directly into the ALU. The ALU comprises a 16-bit parallel adder/subtracter logic network. The arithmetic or logical result is gated to the 16-bit S Bus.

Bits 0 through 7 of IR, the user's operation code, are used to address locations in the Decoder Read-Only-Memory (DROM). DROM is a separate Read-Only-Memory that has 256 12-bit words. DROM is interrogated prior to entering the micro-subroutine that executes a user instruction. The DROM readout is jammed into the ROM address registers. The DROM readout corresponds to the starting micro-program address for a given user instruction.

Input/Output operations are accomplished by activating one of eight control lines and gating the S Bus onto the Data Lines or gating the Data Lines onto the B Bus.

4. WORD FORMATS

4.1 General

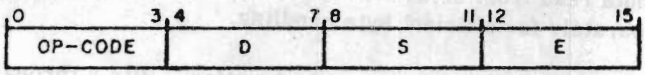
The Processor executes 16 basic micro-instructions (see Table 1). Bits 0 through 3 of the ROM Data Register (RD) specify the operation to be performed.

TABLE 1. BASIC MICRO-INSTRUCTIONS

OP-CODE	MICRO-INSTRUCTION	
0123	Symbolic	Meaning
0000	D	DO
0001	C	COMMAND
0010	T	TEST
0011	B	BRANCH
0100	L	LOAD
0101	L	LOAD IMMEDIATE
0110	O	OR
0111	O	OR IMMEDIATE
1000	N	AND
1001	N	AND IMMEDIATE
1010	X	EXCLUSIVE OR
1011	X	EXCLUSIVE OR IMMEDIATE
1100	A	ADD
1101	A	ADD IMMEDIATE
1110	S	SUBTRACT
1111	S	SUBTRACT IMMEDIATE

Micro-instructions can have any one of four machine language formats, depending on the operation specified by the OP-CODE. The formats are listed in the following paragraphs by the micro-instructions which use them.

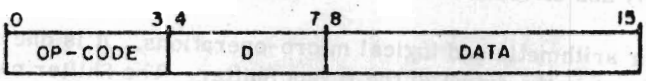
4.2 Add, Subtract, And, Or, Exclusive Or, and Load



Bit 3 of the Op-Code in this format is always reset.

D = Destination field. The result of the operation is placed into the register whose address is in this field.
S = Source field. The address of the register containing the first operand is in this field. The second operand is contained in the A Register (AR).
E = Extended operation field. Instruction options are specified in this field.

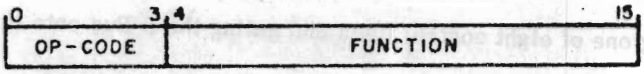
4.3 Add Immediate, Subtract Immediate, And Immediate, Or Immediate, Exclusive Or Immediate, and Load Immediate



Bit 3 of the op-code in this format is always set.

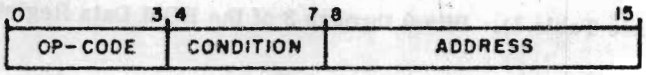
D = Destination field. The result of the operation is placed into the register whose address is in this field.
DATA = The first operand is contained in this field. The second operand is contained in the A Register (AR).

4.4 Do, Command, and Test



FUNCTION = Specifies the function to be performed or tested.

4.5 Branch



CONDITION = specifies the condition to be tested.
ADDRESS = if the specified condition is true, the program is transferred to the address specified by this field.

5. SOURCE AND DESTINATION REGISTERS

Source registers are only available to non-immediate micro-instructions, RD Bit 3 = 0. The sources that may be addressed are shown in Table 2.

TABLE 2. ADDRESSABLE SOURCES

RD Bits	SYMBOLIC REGISTER	RD Bits	SYMBOLIC REGISTER
8 9 10 11		8 9 10 11	
0 0 0 0	MR0	1 0 0 0	NULL
0 0 0 1	MR1	1 0 0 1	IR
0 0 1 0	MR2	1 0 1 0	MDR
0 0 1 1	LOC	1 0 1 1	IO
0 1 0 0	PSW	1 1 0 0	IR4
0 1 0 1	MAR	1 1 0 1	YS
0 1 1 0	SRH	1 1 1 0	YD
0 1 1 1	SRL	1 1 1 1	YDP1

The source registers may be used freely in the micro-program. The following paragraphs point out special cases.

MAR can be used as a source register at any time. However, MAR may or may not contain the same data as MAS depending on the state of memory busy. In the latter case, when memory becomes un-busy, whatever is in MAR is copied into MAS.

SRH and SRL are special purpose shift registers. The Command micro-instruction specifying Multiply, Divide, Shift Right or Shift Left, uses SRH and SRL as a 32-bit shift register; SRH containing the most significant 16 bits and SRL the least significant 16 bits. When the NULL source, Address '8', is used, zeros are gated to all 16 bits of the B Bus. When MDR is specified as the source, the execution of the micro-instruction is suspended until memory data is available.

When I/O (Address 'B') appears as the source, an input operation is to be performed. Only in a Load micro-instruction can I/O be a source. The nature of the input request is encoded into the Extended Operation Field of the Load instruction. When the device responds, the data is gated onto the B Bus. Completion of the micro-instruction is suspended until the device responds.

Specifying IR4 causes Bits 8 through 11 of IR to be gated onto the B Bus Bits 12 through 15. Zeros are gated onto B Bus Bits 0 through 11.

The user's 16 general purpose registers do not have individual source addresses. Instead, common symbolic addresses - YS (Address 'D'), YD (Address 'E') and YDP1 (Address 'F') cause the General Registers to be selected from IR Bits 8 through 11 or 12 through 15. When YS appears as the source, the General Register whose address is in IR Bits 12 through 15 is gated onto the B Bus. When YD appears as the source, the General Register whose address is in IR Bits 8 through 11 is gated onto the B Bus. When YDP1 (User's Destination plus 1) appears as the source, the odd member of the even/odd pair of General Registers addressed by IR Bits 8 through 11 is gated onto the B Bus.

The destinations that may be addressed are shown in Table 3.

TABLE 3. ADDRESSABLE DESTINATIONS

RD BITS	SYMBOLIC REGISTER
4 5 6 7	
0 0 0 0	RAH * MR0 **
0 0 0 1	RAL * MR1 **
0 0 1 0	PSW * MR2 **
0 0 1 1	LOC
0 1 0 0	FLR
0 1 0 1	MAR
0 1 1 0	SRH
0 1 1 1	SRL
1 0 0 0	AR
1 0 0 1	IR
1 0 1 0	MDR
1 0 1 1	IO
1 1 0 0	CTR
1 1 0 1	YS
1 1 1 0	YD
1 1 1 1	YDP1

* The Bank flip-flop must be reset to load RAH, RAL, or PSW
** The Bank flip-flop must be set to load MR0, MR1, or MR2

The destination registers may be used by the micro-program noting the following restrictions or special cases.

Loading RAH loads only the outer rank page register of the ROM address register. The ROM decodes the page from the inner rank (RAS). When RAL is loaded, RAH is copied into RAS so that all 12 bits of ROM address change simultaneously.

When PSW is loaded, Bits 12 through 15 of the S Bus are captured in the FLR. PSW Bits 12 through 15 (the condition code) can only be loaded from the FLR on a Do micro-instruction.

When LOC is loaded, MAR is loaded simultaneously.

Anytime memory iis not Busy, MAR is copied into MAS.

Loading the FLR in an instruction that normally sets flags causes an OR-ing of the resulting flags and S Bus data.

If an attempt is made to load MDR when memory is Busy, execution of that micro-operation is suspended until memory becomes not Busy. If MDR is the destination in a cross-shift operation, only the high byte (MDH) is loaded if MAR is even and the cross-shift function is performed. If MAR is odd, only the low byte (MDL) is loaded and the cross-shift function is not performed. The portion of the MDR (i.e. MDH or MDL) not loaded remains unchanged. If MDR is the destination and cross-shift is not exercised, both bytes (MDH and MDL) are loaded.

When I/O appears as the destination, an output operation is to be performed. Only in a Load micro-instruction can I/O be a destination. The nature of the output operation is encoded into the Extended operation field of the Load instruction. The S Bus is gated onto the Data Lines. Completion of the micro-instruction is suspended until the device responds or a false SYN is generated.

When YS is the destination, S Bus data is copied into the General Register whose address is in IR Bits 12 through 15.

When YD is the destination, the General Register whose address is in IR Bits 8 through 11 is loaded.

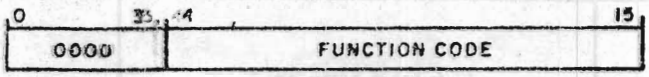
When YDP1 is the destination, the odd member of the even/odd pair of General Registers addressed by IR Bits 8 through 11 is loaded.

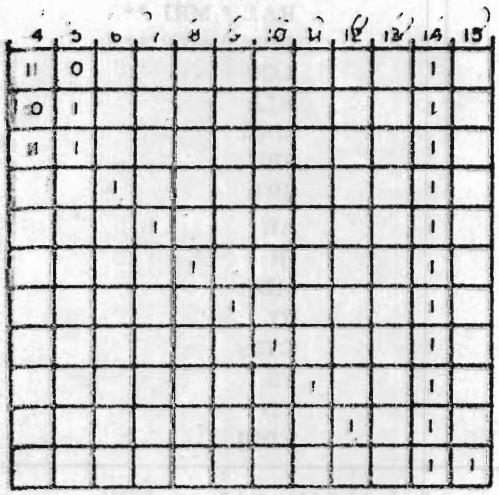
6. MICRO-INSTRUCTIONS

This section describes each micro-instruction. For each instruction, the assembler format is shown. The machine instruction format is diagrammed, a description of the instruction is provided, and options within the instruction are described.

6.1 Do

D FUNCTION





	SYMBOLIC MEANING
MR	MEMORY READ
MW	MEMORY WRITE
PW	PRIVILEDGED WRITE
INC	INCREMENT LOC
JAM	COPY FLR TO CC
PC	PHASE CHANGE
CLR	CLEAR
SWA	SET WAIT
CWA	CLEAR WAIT
ALRM	LOAD ALARM FLAGS
POW	POWER DOWN

The Do micro-instruction is always written with Bit 14 set.

All zeros in RD are interpreted as illegal unless RD is zero because of initialization. A blanking flip-flop (RUN) covers the initialize period. When the Processor is initialized, the ROM Address Registers and RD are cleared and the RUN flip-flop is reset. Location X'000' in ROM contains all zeros. When this instruction is read, the RUN flip-flop is still reset and the Processor does nothing. The next instruction in sequence (Address X'001') is executed and the RUN flip-flop sets. The next time all zeros occur in RD, the illegal condition will exist, forcing the Processor to Phase Three and ROM address to X'100'.

The DO micro-instruction is executed in one clock period unless a memory cycle is requested (MR, MW, PW) and memory is Busy or phase change is specified and the new phase is Phase zero.

In the former case, the DO micro-instruction can take realistically 1, 2, or 3 clocks depending on when the current memory cycle began. In the latter case, the time depends upon the state of Memory Busy and the type of user instruction to be performed.

The type of user instruction is identified by the most significant four bits of the op-code in IR. Table 4 shows the user repertoire. From Table 4, the following list of op-codes by category is derived.

OP CODES

RR Instructions:	0n
	1n
	2n
	3n
	8n
	9n
RX Instructions:	4n
	5n
	6n
	7n
	An
	Bn
	Dn
	Fn
RS Instructions:	Cn
	En

If an RR instruction is to be performed, the DO micro-instruction requires 2 or 3 clocks. If an instruction other than RR is to be performed, the DO micro-instruction requires 4 or 5 clocks.

TABLE 4. INSTRUCTION REPERTOIRE

Op Code MSD →

Op Code LSD ↓

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0			BTBS		STH		STE			SRLS			BXH	STM		
1	BALR		BTFS		BAL		AHM			SLLS			BXLE	LM	SVC	
2	BTCR		BFBS		BTC					STBR			LPSW	STB	SINT	
3	BFCR		BFFS		BFC					LBR			THI	LB		
4	NHR		LIS		NH		ATL			EXBR			NHI	CLB		
5	CLHR		LCS		CLH		ABL			EPSR			CLHI	AL		
6	OHR		AIS		OH		RTL			WBR			OHI	WB		
7	XHR		SIS		XH		RBL			RBR			XHI	RB		
8	LHR		LER		LH		LE			WHR			LHI	WH		
9	CHR		CER		CH		CE			RHR			CHI	RH		
A	AHR		AER		AH		AE			WDR			AHI	WD	RRL	
B	SHR		SER		SH		SE			RDR			SHI	RD	RLL	
C	MHR		MER		MH		ME			MHUR			SRHL	MHU	SRL	
D	DHR		DER		DH		DE			SSR			SLHL	SS	SLL	
E	ACHR				ACH					OCR			SRHA	OC	SRA	
F	SCHR				SCH					AIR			SLHA	AI	SLA	
	RR	RR	RR	RR	RX	RX	RX	RX	RR	RR	RX	RX	RS	RX	RS	RX

When phase change is specified, the new state of the Phase Pointer and the new ROM address depends upon the current phase, the type of user instruction to be executed, and whether or not an interrupt is pending. These factors are summarized in Table 5.

The Phase Pointer has four states. One of these, Phase Zero, exists in hardware only and does not have an associated set of micro-code.

In Phase Zero, the user instruction is loaded into MDR and IR simultaneously. The AR is loaded from YS and the OP flip-flop is set to reflect the length of the user instruction: 0 if RR, 1 if RX or RS. If the user instruction is RX or RS, a second memory read is started to fetch the second half of the instruction word. If the user instruction is not RR, the YS field of IR distinguishes Indexed instructions from unindexed. If the YS field is zero, the instruction is not indexed. If the user instruction is RR or unindexed RS, Phase Zero is exited and the Phase Two entry point is derived from the DROM. If the user instruction is RX or indexed RS, Phase Zero is exited and the appropriate Phase One entry point is generated. There are three micro-sequences associated with Phase One. These sequences are shown below:

```
ROM     ROM
ADRS    DATA
                *INDEXED      RS  ENTRY
0002    CAA3    AMODRS    A     MDR, MDR      INDEX 'A' FIELD
0003    00C2              D     PC+CLR        GO TO PHASE 2
                *NO INDEX     RX  ENTRY
0004    45A3    NMODRX    L     MAR, MDR      ADRS 'A'
0005    08C2              D     MR+PC+CLR     GO TO PHASE 2
                *INDEXED  RX  ENTRY
0006    C5A3    AMODRS    A     MAR, MDR      ADRS 'A' +(X2)
0007    08C2              D     MR+PC+CLR     GO TO PHASE 2
```

The Do micro-instruction exiting Phase One of an RX instruction would normally execute in three clocks because a memory read is requested and memory is still busy from the read cycle started as Phase Zero was exited. If the user op-code is 40, 41, 42, or 43, the Do micro-instruction takes only 1 clock. These user instructions (STH, BAL, BTC, and BFC) do not require a second operand so the memory read is not attempted. An unnecessary memory read does occur on STM, STE, AL, and RH instructions.

TABLE 5. DECODE PHASE CHANGES

CURRENT PHASE	INTERRUPTS ?	NEXT INSTR	INDEXED ?	NEW PHASE	NEW ROM ADDRESS
1				2	From DROM
2	Yes			3	'010'
2	No	RR		0 then 2	From DROM
2	No	RS	No	0 then 2	From DROM
2	No	RS	Yes	0 then 1	'002'
2	No	RX	No	0 then 1	'004'
2	No	RX	Yes	0 then 1	'006'
3		RR		0 then 2	From DROM
3		RS	No	0 then 2	From DROM
3		RS	Yes	0 then 1	'002'
3		RX	No	0 then 1	'004'
3		RX	Yes	0 then 1	'006'

The Phase Two sequence starting address is derived from the Decoder Read-Only-Memory. There are as many Phase Two sequences as there are unique entries in the DROM. Illegal instruction handling is explained in Section 8.

There are three Phase Three entry points: Location X'100' for the Illegal Instruction (RD=0), Location X'010' for Interrupts, and X'00A' for aborted sequences. When Phase 2 is exited, the hardware automatically tests for interrupts. The interrupts tested for are Primary Power Fail (PPF), Machine Malfunction (MALF), Console Attention (CATN), Console Single Mode (SNGL), Data Channel Request (DC), and I/O Attention (ATN). If an interrupt is found pending when the Do micro-instruction that exits Phase Two is executed, the Phase Pointer is set to Phase Three, the INC and MR specifications in the Do micro-instruction are suppressed, and ROM address is forced to X'010'.

The micro-sequence at X'010' determines the nature of the interrupt and executes the appropriate service sequence.

When Phase Two is entered, an Enable flip-flop (EBL) is set. As long as EBL is set, the occurrence of a Data Channel Request (DC) or regular I/O Interrupt (ATN) or a Machine Malfunction (MALF) will cause the user instruction sequence to be aborted. The Processor enters Phase Three and ROM address is forced to X'00A'. The micro-routine at X'00A' decrements the Location Counter by 2 if the user instruction was RR or by 4 if RX or RS, and then enters the common interrupt polling subroutine at X'010'. (Instruction type can be known by testing the OP flip-flop.) After the interrupt is serviced, the user instruction is re-started from the beginning.

The Enable flip-flop is reset whenever the micro-program loads a General Register, loads PSW or LOC, does a Memory Write or Priviledged Write or an I/O operation. When Enable resets, the instruction is not interruptable until the terminating Do micro-instruction is executed.

OPTIONS

The function code bits specify the function(s) to be performed. The Phase Change function has been described; the other functions are described below:

MR Memory Read

MW Memory Write

PW Priviledged Write

A memory cycle consists of two half cycles: Read and Write; in that order. The Read cycle places the contents of the addressed location into MDR. The addressed location then contains zeros (destructive read-out). During the Write cycle, the contents of MDR are written into the addressed location.

Memory Read (MR) is a combination of the Read/Write cycles. The memory location is read-out then restored from MDR. Memory Write (MW) or Priviledged Write (PW) work like this; the memory location is read-out but the data is not saved. Instead, the contents of MDR are written into the addressed location.

Memory Write (MW) and Priveledged Write (PW) commands operate identically if the memory system does not include the Memory Protect option. If the Memory Protect option exists, the PW command unconditionally writes to memory. However, the MW command is subject to memory protect and will be converted to an MR command if the address is in a protected area of memory and if PSW 7 is set. If PSW 7 is reset, the Memory Protect feature is disabled.

INC - Increment LOC - The Location Counter is incremented by two. The result is also copied into MAR.

JAM - Copy FLR to CC - The Condition Code (Bits 12:15) of PSW is loaded from the Flag Register (FLR).

CLR - Clear - The Bank flip-flop and Utility flip-flop are cleared. The Flag Register is cleared. The counter is set to 16.

SWA - Set Wait Alarm - The Wait indicator is set.

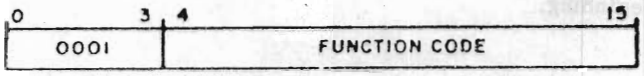
CWA - Clear Wait Alarm - The Wait indicator is reset.

ALRM - Copy Alarm Bits - The bits set in the Alarm Register are copied to the Condition Code Register. If JAM is also specified, the Alarm Bits are "ORed" with the Flag Register Bits. The Alarm Register bits are then reset. See Section 8.

POW - Power Down - The system is initialized.

6.2 Command

C FUNCTION



4	5	6	7	8	9	10	11	12	13	14	15	SYMBOLIC	MEANING
1	0											MR	MEMORY READ
0	1											MW	MEMORY WRITE
1	1											PW	PRIVILEGED WRITE
		1	1							1	1	MPY	MULTIPLY
		1		1						0	1	DIV	DIVIDE
		1			1							RPT	REPEAT
		0	1									SRI	SHIFT RIGHT
		0		1								SLI	SHIFT LEFT
						1	0					SUT	SET UTILITY
						0	1					CUT	RESET UTILITY
						1	1					TUT	TOGGLE UTILITY
								1				SB	SET BANK
									1			CB	CLEAR BANK
										1		CI	CARRY IN
											1	CO	CARRY OUT

The Command micro-instruction results in the performance of the machine functions specified by the Function Code Bits. The functions are described below.

MR Memory Read

MW Memory Write

PW Priviledged Write

MPY - Multiply - The Processor multiplies the 16 bit multiplicand in AR by the 16 bit multiplier in SRL. The 32-bit product resides in SRH and SRL. To achieve this, the following setup conditions must exist. The counter contains 16; SRH contains zero; SRL and AR contain the operands; and the Carry Flag is reset. The C MPY instruction executes in sixteen Processor clock periods (16t). After the C MPY instruction, the 32-bit product in SRH and SRL must be shifted right one more position.

DIV - Divide - The Processor divides the 32 bit dividend in SRH and SRL by the 16 bit divisor in AR. To achieve this, the following setup conditions must exist. The counter contains 16; SRH/SRL contains a positive dividend that is less than 65,536 times the divisor. The AR contains the divisor in two's complement negative form; and the Carry Flag is reset. The C DIV instruction executes in 16t. After the C DIV instruction, the quotient resides in SRL and the remainder is in SRH.

RPT - Repeat - If the counter is not zero, the next sequential micro-instruction is repeated the number of times specified in the Counter Register. If the counter is zero, the next sequential micro-instruction is skipped. Any reasonable instruction may be repeated that does not result in a Branch (Branch, Load RAL or Decode Phase Change).

SRI - Shift Right - The 32-bit shift register (SRH/SRL) is shifted right one position. Carry in and out are specifiable.

SLI - Shift Left - The 32-bit shift register (SRH/SRL) is shifted left one position. Carry in and out are specifiable.

SUT - Set Utility

CUT - Reset Utility

TUT - Toggle (complement) Utility

The Utility flip-flop has no hardware function assigned to it. It is for program control and may be tested with the test micro-instruction.

SB - Set Bank

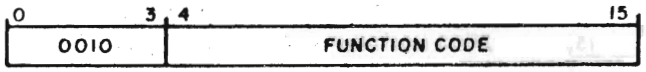
CB - Clear Bank

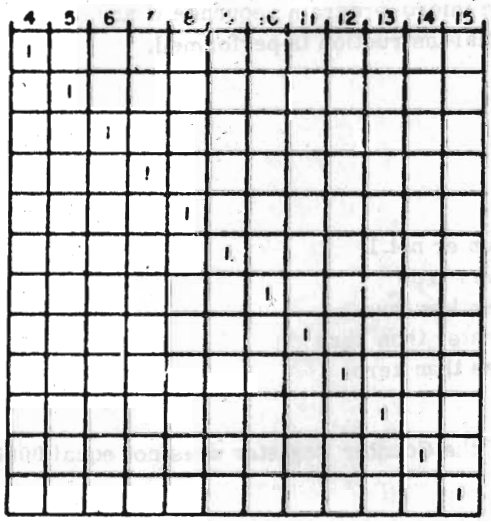
The Bank flip-flop controls the addressing of certain registers.

If no functions are specified, the Assembler leaves the function code field reset.

6.3 Test

T FUNCTION





	SYMBOLIC MEANING
FAST	FAST I/O INTERRUPT
ATN	I/O ATTENTION
ARST	AUTO RESTART
CATN	CONSOLE ATTENTION
SNGL	CONSOLE SINGLE MODE
UT	UTILITY FLIP-FLOP
MALF	MACHINE MALFUNCTION
PPF	PRIMARY POWER FAIL
DC	DATA CHANNEL REQUEST
DRD	DATA CHANNEL READ
MSK	MASK BITS
OP	USER OPERATION LENGTH

If any of the machine functions specified by the function code bits are true, the Greater than (G) flag is set and the Less than (L) flag is reset. If none of the tested functions are true, the Less than (L) flag is set and the Greater than (G) flag is reset. The Testable functions are:

FAST - High Speed Interrupt - This flip-flop is AC set when the FAST0 interrupt line becomes active. This interrupt line is separate from the normal ATN line and may have any priority the micro-programmer decides. The FAST0 interrupt may be enabled by a PSW bit (PSW04) by back-panel strapping. After the micro-program tests the FAST flip-flop, the flip-flop automatically resets.

ATN - I/O Attention - An external device is requesting Processor service and PSW Bit 1 is set.

ARST - Automatic Restart - This is a hardwire strap option with significance only to the emulator.

CATN - Console Attention - The console EXEcute Switch has been depressed.

SNGL - Console Single Mode - The SNGL flip-flop in the display controller is set.

UT - Utility flip-flop set

MALF - Machine Malfunction - One of the bits in the Machine Malfunction Alarm Register is set. The alarm bits are Parity Error Phase Zero or One, Parity Error Phase Two, and Early Power Fail Detect.

PPF - Primary Power Fail - This signal occurs one millisecond after Early Power Fail Detect. The Micro-Code has one millisecond before system initialize occurs.

DC - Data Channel Request

DRD - Data Channel Read/Write

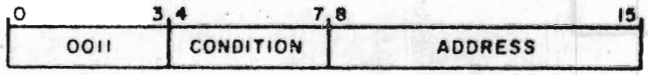
A special halfword device on the data channel is requesting memory access. The state of DRD determines Read or Write, 0 or 1, respectively.

MSK - Mask Bits - The AND of the Condition Code Bits (PSW 12:15) with IR4 (IR8:11) is tested.

OP - User Operation Length - This flip-flop is adjusted in Phase Zero. It is set to one if the user instruction is RX or RS. It is set to zero if the user instruction is RR.

6.4 Branch

B COND, ADDRESS



The Branch micro-instruction results in a transfer in the micro-program sequence if any of the specified conditions are true. If none of the conditions are true, the next sequential instruction is performed.

The condition is specified by RD Bits 4 through 7.

RD BIT	CONDITION	
4 5 6 7	SYMBOLIC	MEANING
0 0 0 0	CTR	Branch if Counter not 1
1 X X X	C	Branch if Carry true
X 1 X X	V	Branch if Overflow true
X X 1 X	G	Branch if Greater than zero
X X X 1	L	Branch if Less than zero

The Branch on Counter instruction results in a transfer if the Counter Register does not equal 00001_2. The counter is decremented by one regardless of its previous state.

The conditions C, V, G, or L may be specified singularly or in combination. Each condition bit is matched against the corresponding bit in the Flag Register. If a match is made, the ADDRESS field is copied to RAL, and RAS is loaded from RAH. If no match is made, the next instruction in sequence is executed. The instruction requires two Processor clocks (2t) if a branch is made. If no branch, the instruction takes 1t.

6.5 Load

L D, S, E



The contents of the register specified by the Source (S) Field are copied into the register specified by the Destination (D) Field.

If neither the Source nor Destination field specify I/O, the E field has the following meaning:

E 12 13 14 15	SYMBOLIC	MEANING
0 0 X X		No shifts.
0 1 X X	SR	Shift Right. The source data is shifted right one bit position and copied into the Destination Register.
1 0 X X	SL	Shift Left. The source data is shifted left one bit position and copied into the Destination Register.
1 1 X X	CS	Cross Shift. The source data is rotated eight bit positions and copied into the Destination Register. If MDR is the Source or Destination, the cross-shift will occur only if MAR is even. If MDR is the Destination and MAR is even, only the high byte (MDH) of MDR is loaded. If MAR is odd, only the low byte (MDL) of MDR is loaded. The byte not loaded remains unchanged.
X X 0 0	NC	No Carry. The Carry Flag is unaltered.
X X 0 1	CO	Carry Out but not in. If a one is shifted out, the Carry Flag is set. If a zero is shifted out, the Carry Flag is reset.
X X 1 0	CI	Carry In but not out. The state of the Carry Flag is shifted into the most significant bit if Shift Right or the least significant bit if Shift Left.
X X 1 1	C	Carry In and Out.

If no options are specified, the Assembler sets the E Field to 0011.

If the Destination (D) Field specifies I/O, an output operation is to be performed. The E Field has the following meaning:

E 12 13 14 15	SYMBOLIC	MEANING
0 0 X X		No shift.
0 1 X X	SR	Shift Right.
1 0 X X	SL	Shift Left.
1 1 X X	CS	Cross Shift.
X X 0 0	DCAK	Data Channel Acknowledge. The source data is present on the Data Lines and the Address and Data Channel Acknowledge Control lines are active. The highest priority interrupting Data Channel device becomes the On Line device.
X X 0 1	ADRS	Address. The source data is present on the Data Lines and the Address Control Line is active. The device that detects its address becomes On Line and responds with a Sync.
X X 1 0	DA	Data Available. The source data is present on the Data Lines and the Data Available Control Line is active. The On Line device accepts the data and responds with a Sync.
X X 1 1	OC	Output Command. The source data is present on the Data Lines and the Output Command Control Line is active. The On Line device accepts the command data and responds with a Sync.

If no options are specified, the Assembler sets the E Field to 0000.

If the Source (S) Field specifies I/O, an input operation is to be performed. The E Field has the following meaning:

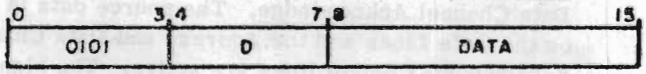
E (12 13 14 15)	SYMBOLIC	MEANING
0 0 X X		No Shifts.
0 1 X X	SR	Shift Right.
1 0 X X	SL	Shift Left.
1 1 X X	CS	Cross Shift.
X X 0 0		Illegal Function.
X X 0 1	ACK	Acknowledge Interrupt. The Acknowledge Interrupt Control Line is active. The highest in priority interrupting device responds by placing its address on the Data Lines. The input data is copied to the Destination Register.
X X 1 0	DR	Data Request. The Data Request Control Line is active. The On Line device responds by placing data on the Data Lines. The input data is copied to the Destination Register.
X X 1 1	STAT	Status Request. The Status Request Control Line is active. The On Line device responds by placing status data on the Data Lines. The input data is copied to the Destination Register.

The Carry Flag is not affected by I/O operations that specify shifts unless the FLR is the explicit destination. If, on any I/O operation, the device fails to respond within 45 microseconds, a false Sync is generated which sets the Overflow Flag and, if the E Field specifies Status Request, forces the Input status to '0004'. The instruction is aborted.

The halfword I/O capability requires special micro-code attention. When a halfword device controller is addressed, the HW control line is active. This control line affects the Processor only when a DR or DA operation is executed and allows the Processor to input/output one 16-bit halfword of data. All other I/O operations are strictly byte oriented. If a DR or DA operation is executed to a halfword device, cross shift is suppressed if it was specified in the LOAD micro-instruction and RAL Bit 14 is forced to a one. Forcing RAL Bit 14 makes the Processor skip two micro-instructions if the least significant hex digit of the address of the DR or DA instruction is 0, 3, 4, 7, 8, B, C, or F. If the least significant address digit is 1, 2, 5, 6, 9, A, D or E, no skip occurs.

6.6 Load Immediate

L D, DATA



The eight bits from the DATA Field are copied into the register specified by the Destination (D) Field. The most significant eight bits are zeroed.

6.7 Or

O D, S, E



The contents of the A Register (AR) are logically added to the contents of the register specified by the Source (S) Field. The logical sum is loaded into the register specified by the Destination (D) Field.

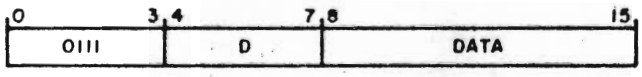
The E Field has the following meaning:

E (12 13 14 15)	SYMBOLIC	MEANING
1 X X X	NA	No AR. The AR is not unloaded. Zeros are ORed with the source data.
X 0 X X	NF	No Flags. The G and L flags are not modified.
X 1 X X		G and L are modified to reflect the algebraic magnitude of the result.
X X 0 0	NC	No Carry. Carry is not modified.
X X 1 0	CI	Carry In but not out. No affect.
X X 0 1	CO	Carry Out but not in. The Carry flag is reset.
X X 1 1	C	Carry In and Out. The Carry Flag is reset.

If no options are specified, the E Field is set to 0111.

6.8 OR Immediate

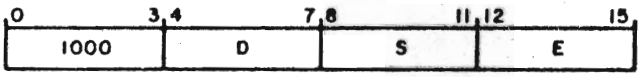
0 D, DATA



The contents of the A Register (AR) are logically added to the eight bits of the Data Field. The most significant eight bits of the B Bus are zero. The logical sum is loaded into the register specified by the Destination (D) Field.

6.9 And

N D, S, E



The contents of the A Register (AR) are logically multiplied by the contents of the register specified by the Source (S) Field. The logical product is loaded into the register specified by the Destination (D) Field.

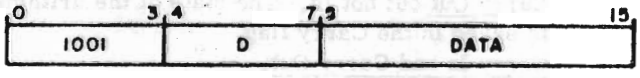
The E Field has the following meaning.

E (12 13 14 15)	SYMBOLIC	MEANING
1 X X X	NA	No AR. The AR is not unloaded. The result will be zero.
X 0 X X	NF	No Flags. The G and L flags are not modified.
X 1 X X		G and L are modified to reflect the algebraic magnitude of the result.
X X 0 0	NC	No Carry. Carry is not modified.
X X 1 0	CI	Carry In but not Out. No affect.
X X 0 1	CO	Carry Out but not In. The Carry flag is reset.
X X 1 1	C	Carry In and Out. The Carry flag is reset.

If no options are specified, the E Field is set to 0111.

6.10 And Immediate

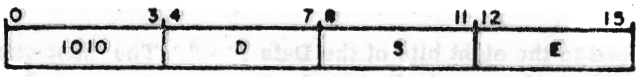
N D, DATA



The contents of the A Register (AR) are logically multiplied by the eight bits of the Data Field. The most significant eight bits of the B Bus are zero. The logical product is loaded into the register specified by the Destination (D) Field.

6.11 Exclusive Or

X D, S, E



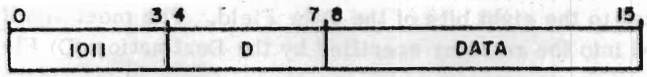
The contents of the A Register (AR) are logically subtracted from the contents of the register specified by the Source (S) Field. The logical difference is loaded into the register specified by the Destination (D) Field. The E Field has the following meaning:

E (12 13 14 15)	SYMBOLIC	MEANING
X X X	NA	No AR. The AR is not unloaded. The source data is unaltered.
X 0 X X	NF	No Flags. The G and L flags are not modified.
X 1 X X		The G and L flags are modified to reflect the algebraic magnitude of the result.
X X 0 0	NC	No Carry. Carry is not modified.
X X 1 0	CI	Carry In but not Out. No affect.
X X 0 1	CO	Carry Out but not In. The Carry flag is reset.
X X 1 1	C	Carry In and Out. The Carry flag is reset.

If no options are specified, the E Field is set to 0111.

6.12 Exclusive Or Immediate

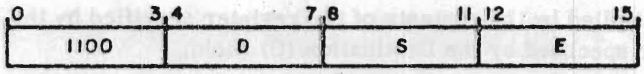
X D, DATA



The contents of the A Register (AR) are logically subtracted from the eight bits of the Data Field. The most significant eight bits of the B Bus are zero. The logical difference is loaded into the register specified by the Destination (D) Field.

6.13 Add

A D, S, E



The contents of the A Register (AR) are algebraically added to the contents of the register specified by the Source (S) Field. The sum is loaded into the register specified by the Destination (D) Field.

The E Field has the following meaning:

E (12 13 14 15)	SYMBOLIC	MEANING
1 X X X	NA	No AR. The AR is not gated to the ALU. Zeros are added to the Source data.
X 0 X X	NF	No Flags. The G, L, and V flags are not modified.
X 1 X X		The G and L flags are adjusted to reflect the algebraic magnitude of the result. The V flag is adjusted to reflect the overflow condition.
X X 0 0	NC	No Carry. The Carry flag does not participate, nor is it modified.
X X 1 0	CI	Carry In but not Out. The Carry flag is added with the least significant bit of the sum.
X X 0 1	CO	Carry Out but not In. The state of the arithmetic carry is saved in the Carry flag.
X X 1 1	C	Carry In and Carry Out.

If no options are specified, the E Field is set to 0111.

6.14 Add Immediate

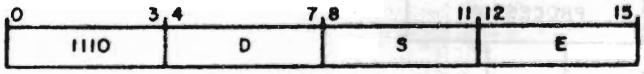
A D, DATA



The contents of the A Register (AR) are algebraically added to the eight bits of the Data Field. The most significant eight bits of the B Bus are zero. The sum is loaded into the register specified by the Destination (D) Field.

6.15 Subtract

S D, S, E



The contents of the A Register (AR) are algebraically subtracted from the contents of the register specified by the Source (S) Field. The difference is loaded into the register specified by the Destination (D) Field.

The E Field has the following meaning:

E 12 13 14 15	SYMBOLIC	MEANING
1 X X X	NA	No AR. The AR is not gated to the ALU. Zeros are subtracted from the Source data.
X 0 X X	NF	No Flags. The G, L, and V flags are not modified.
X 0 X X		The G and L flags are adjusted to reflect the algebraic magnitude of the result. The V flag is adjusted to reflect the overflow condition.
X X 0 0	NC	No Carry. The Carry flag does not participate nor is it modified.
X X 1 0	CI	Carry In but not Out. The Carry flag represents the borrow situation from Bit 15 of the Source data. This borrow participates in the subtraction.
X X 0 1	CO	Carry Out but not In. The state of the arithmetic carry (borrow) is saved in the Carry flag.
X X 1 1	C	Carry In and Carry Out.

If no options are specified, the E Field is set to 0111.

6.16 Subtract Immediate

S D, DATA



The contents of the A Register (AR) are algebraically subtracted from the eight bits of the Data Field. The most significant eight bits of the B Bus are zero. The difference is loaded into the register specified by the destination (D) Field.

7. MULTIPLEXOR CHANNEL

The Multiplexor Channel is a byte or halfword oriented I/O system which communicates with up to 255 peripheral devices. The Multiplexor Bus consists of 30 lines; 16 bi-directional Data Lines, 9 Control Lines, 5 Test Lines, and an Initialize Line.

A list of the lines in the Multiplexor Bus follows.

Data Lines	D00:15	(Processor ⟷ Device)	16 Lines
Control Lines	SR	(⟶)	1 Line
	DR	(⟶)	1 Line
	CMD	(⟶)	1 Line
	DA	(⟶)	1 Line
	ADRS	(⟶)	1 Line
	ACK	(⟶)	1 Line
	DACK	(⟶)	1 Line
	CL07	(⟶)	1 Line
Test Lines	ATN	(⟵)	1 Line
	SYN	(⟵)	1 Line
	HW	(⟵)	1 Line
	DC	(⟵)	1 Line
	DRD	(⟵)	1 Line
Initialize	SCLRO	(⟶)	1 Line

Figure 2 is a block diagram of the Multiplexor Channel. The following general definitions apply to the lines in the Multiplexor Bus.

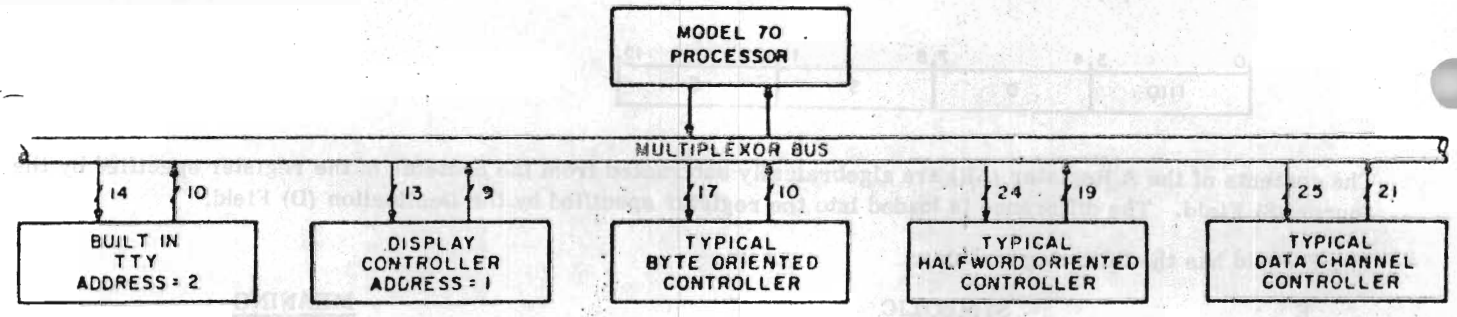


Figure 2. Multiplexor Channel Block Diagram

7.1 Data Lines D00:15

The Data Lines are used to transfer one 8-bit byte or one 16-bit halfword of data between the Processor and the Device. One byte of data is transferred from the Processor to the Device over D08:15 when accompanied by either an Address (ADRS) or a Command (CMD) control line. One byte of data or one halfword of data is transferred from the Processor to the Device when accompanied by the Data Available (DA) control line. The Device, in response to an Acknowledge (ACK) control line or a Sense Status (SSR) control line, sends one byte of address or status information to the Processor over D08:15. In response to a Data Request (DR) control line, the Device sends either an 8-bit byte or a 16-bit halfword of data to the Processor. The device always sends a Synchronize (SYN) signal to the Processor to indicate that it has either received the data from the Processor or that it has sent the data to the Processor. The SYN signal is removed immediately after the Processor removes the control line.

7.2 Control Lines

CONTROL LINE	FUNCTION	DESCRIPTION
0	ADRS (Address)	The Processor presents an address byte on D08:15. The Device Controller that decodes its Device Numbe becomes addressed or on line and responds with a SYN.
1	DA (Data Available)	The Processor presents data on D00:15 for the device. The Device Controller accepts the low order byte or the entire halfword and responds with a SYN.
2	DR (Data Request)	The Device Controller presents data to D08:15 or D00:15, followed by a SYN. If the Device Controller is halfword oriented, the HW test line is also active.
3	STAT (Status Request)	The Device Controller presents the device status byte to D08:15, followed by a SYN.
4	CMD (Command)	The Processor presents a command byte on D08:15 for the device. The Device Controller accepts the command byte and responds with a SYN.
5	ACK (Acknowledge)	The Device Controller nearest the Processor that originated an ATN presents its address on D08:15, followed by a SYN.
6	DCAK (Data Channel Acknowledge)	The micro-program should present an address of zero on D00:15. The ADRS and DCAK control lines are simultaneously active. The Data Channel Controller nearest the Processor that originated a DC becomes addressed and responds with a SYN. Addressing device zero (a null address) leave all other Device Controllers un-addressed.
7	CL070	This control line is activated by the Processor when a power fail condition is detected by the Processor if the power fail option is equipped. The line is held active until the SCLR0 signal occurs.

7.3 Test Lines

ATN — Attention. Any Device desiring to interrupt the Processor will activate the ATN line and hold this line until an ACK is received from the Processor.

HW — Halfword. Any halfword-oriented Device, other than Data Channel devices, will activate the HW line when it becomes addressed and hold this line for as long as it is addressed. When the HW test line is active and a Micro-Program does a DA or DR I/O operation, if Cross Shift was specified on that I/O Load, Cross Shift is suppressed so the 16 bits of data are not modified and ROM Address Register Bit 14 (RAL14) is forced to a one. If RAL14 was already set, RAL remains unchanged.

DC — Data Channel Request. Any Data Channel Device desiring to interrupt the Processor will activate the DC line and hold this line until a DCAK is received from the Processor.

DRD — Data Channel Read. The selected Data Channel Device controls the state of the DCR line - low for Read, high for Write, from the Device.

SYN — Synchronize. This signal is generated by the Device to inform the Processor that it has properly responded to a control line.

SCLR — System Clear. This is a metallic contact to ground that occurs during Power Fail, Power Up, or Initialize.

NOTE

All Control Lines, except ACK and DCAK, are connected in parallel to an External Interrupt. The ACK line is connected in series with all Devices. The DCAK line is connected in series with all Data Channel devices. If no interrupt is pending in the first Controller ACK or DCAK arrives at, the signal is passed on daisy chain fashion to the next Controller and so on until it is captured by the interrupting Controller. See definitions of ACK and DCAK.

7.4 Micro-Programming Input/Output

Input/Output operations are initiated when a Load micro-instruction specifying IO as the source or destination is executed. A Device Controller must be addressed before any data can be transferred. To address a device, the device number must reside in some register.

```
L    SRL,  'nn'          DEVICE NUMBER
L    IO, SRL, ADRS       ADDRESS THE DEVICE
B    V, ERROR            FALSE SYNC
```

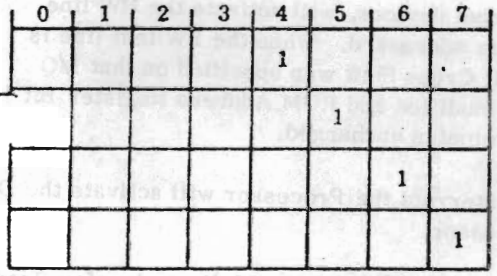
If the device is operational, it responds with a SYN. If SYN is not received within approximately 45 microseconds, a false sync (FSYN) is generated which sets the V flag in FLR and aborts the micro-instruction. If the Micro-programmer is going to be concerned about the lack of response from a device, he may follow up the ADRS micro-instruction with a Branch on Overflow.

If FSYN occurs on ADRS, one can be confident that it will also occur on subsequent I/O operations to the same device. Thus, the micro-programmer may wait until later to catch the FSYN condition.

Sample Input/Output sequences for some standard devices follow. Obviously, routines for every device cannot be shown and the routines shown may not fit every possible application. Device characteristics can be found in the documentation for each device. The micro-programmer must understand that device documentation is slanted towards the Model 70 user repertoire and timing problems may occur when a device is driven with micro-code.

The following general significance is attached to the status byte from a device.

DEVICE STATUS



Busy. The device Controller is not ready to transfer data.

Examine status. Either an FSYN has occurred or an unusual status exists. The entire status byte must be examined.

End Of Medium. This bit is set at the termination of the device medium, such as end of card. Not all devices use this bit.

Device Unavailable. The device is powered down or otherwise off line.

When device status is requested, it is convenient to use the Flag Register (FLR) as the destination. Branch instructions can then test the low order four status bits.

TELETYPE PAPER TAPE INPUT

The following instructions start the tape reader:

```
        L   SRL, '02'          TTY DEVICE NUMBER
        L   IO, SRL, ADRS      ADDRESS THE DEVICE
        L   SRL, '98'          COMMAND BYTE
        L   IO, SRL, CMD       SELECTS WRITE MODE
SENSE0  L   FLR, IO, STAT
        B   VGL, ERROR
        B   C, SENSE0
        L   SRL, '91'          X-ON CHARACTER
        L   IO, SRL, DA
```

As soon as the TTY processes the X-ON Character, the tape reader will begin advancing the tape.

```
SENSE1  L   FLR, IO, STAT      WAIT FOR X-ON
        B   VGL, ERROR         CHARACTER TO BE
        B   C, SENSE1          PROCESSED
        L   SRL, '94'
        L   IO, SRL, CMD       SWITCH TO READ MODE

SENSE2  L   FLR, IO, STAT      STATUS REQUEST
        B   VGL, ERROR         BAD STATUS
        B   C, SENSE2          LOOP IF BUSY
        L   SRL, IO, DR        READ DATA
```

After processing the data byte in SRL, return to SENSE2 to receive next data byte.

```
        .
        .
        .
```

The following instructions stop the TTY reader

```
        L   SRH, '98'          COMMAND BYTE
        L   IO, SRH, CMD       SWITCH TO WRITE MODE
SENSE3  L   FLR, IO, STAT      STATUS REQUEST
        B   VGL, ERROR
        B   C, SENSE3
        L   SRH, '93'          X-OFF CHARACTER
        L   IO, SRH, DA        OUTPUT IT
SENSE4  L   FLR, IO, STAT      WAIT FOR CHARACTER
        B   C, SENSE4          TO BE PROCESSED
        .
        .
        .
```

The Busy loops at SENSE1 and SENSE4 are not really necessary. It is generally recommended, however, that the Processor waits on Busy before switching a device from the Write Mode to the Read Mode. It is also good practice to leave a device in an un-Busy condition when the routine has finished.

TELETYPE PAPER TAPE OUTPUT

Start the TTY punch

```
            L   SRH, '02'          TTY DEVICE NUMBER
            L   IO, SRH, ADRS      ADDRESS THE DEVICE
            L   SRH, '98'          COMMAND BYTE
            L   IO, SRH, CMD       SELECT WRITE MODE
SENSE1      L   FLR, IO, STAT      STATUS REQUEST
            B   VGL, ERROR         BAD STATUS
            B   C, SENSE1          LOOP IF BUSY
            L   SRH, '92'          TAPE ON CHARACTER
            L   IO, SRH, DA        OUTPUT IT
SENSE2      L   FLR, IO, STAT
            B   VGL, ERROR         BAD STATUS
            B   C, SENSE2          LOOP IF BUSY
            .
```

Load data to output into SRH, then

```
            .
            L   IO, SRH, DA
            .
```

Loop back to SENSE2 to output subsequent data bytes

```
            .
            .
```

Stop the TTY punch

```
SENSE3      L   FLR, IO, STAT      WAIT FOR LAST
            B   C, SENSE 3         CHARACTER
            L   SRH, '94'          TAPE OFF CHARACTER
            L   IO, SRH, DA
SENSE4      L   FLR, IO, STAT      WAIT FOR CHARACTER
            B   C, SENSE4          TO BE PROCESSED
            .
            .
```

HIGH SPEED PAPER TAPE READER

The following instructions start the HSPTR

```
            L   SRH, '03'          HSPTR DEVICE NUMBER
            L   IO, SRH, ADR       ADDRESS THE DEVICE
            L   SRH, '99'          COMMAND BYTE
            L   IO, SRH, CMD       READ MODE
SENSE1      L   FLR, IO, STAT      STATUS REQUEST
            B   VGL, ERROR         BAD STATUS
            B   C, SENSE1
            L   SRH, IO, DR
            .
            .
```

After processing the data, return to SENSE1 to read next byte

```
            .
            .
```

Stop the HSPTR

```
            L   SRH, 'A9'          COMMAND BYTE
            L   IO, SRH, CMD       DSBL, STOP, INCR, READ
```

HIGH SPEED PAPER TAPE PUNCH

```
                L   SRH, '03'
                L   IO, SRH, ADR
                L   SRH, '92'
                L   IO, SRH, CMD
SENSE1          L   FLR, IO, STAT
                B   VGL, ERROR
                B   C, SENSE1
```

Load data to output into SRH

```
                .
                .
                .
                L   IO, SRH, DA
```

Loop back to SENSE to output subsequent data bytes:

```
                .
                .
                .
SENSE2          L   FLR, IO, STAT       WAIT FOR LAST
                B   VGL, ERROR          CHARACTER TO BE
                B   C, SENSE 2          PROCESSED
                L   SRH, 'A9'
                L   IO, SRH, CMD        DSBL, STOP, INCR, READ
```

8. INTERRUPT SYSTEM

The interrupt structure provides rapid response to external and internal events that require special software attention. The descriptions that follow are oriented towards the emulator.

8.1 Internal Interrupts

Seven different internal interrupts may be generated. Of these, the Fixed-Point Divide Fault, Floating-Point Arithmetic Fault, Queue Service and Supervisor Call Interrupts are created by the emulator and the Illegal Instruction, Protect Mode Violation and Machine Malfunction Interrupts are generated in the hardware.

8.1.1 Illegal Instruction Interrupt. The Illegal Instruction Interrupt occurs when an instruction not in the user repertoire is attempted. When Phase Two is entered, the Decoder Read-Only Memory (DROM) is interrogated. DROM is addressed by the Operation Code Field (Bits 0:7) of IR. Each legal user instruction has an associated 12-bit word in DROM. This word is the starting address of the micro-routine that will execute the user's instruction. Illegal op-codes have an associated DROM word of all zeros. The DROM read-out is jammed into RAH, RAS, and RAL as Phase Two is entered.

ROM location X'000' contains all zeros. When ROM location X'000' is read-out, the zero condition of RD forces the Processor to Phase Three and sets the ROM Address Registers to X'100'. The micro-routine at X'100' decrements the Location Counter (LOC) by 2 if the attempted instruction was RR or by 4 if RX or RS. Then the current program status word (PSW and LOC) is stored in the old PSW save area for the Illegal Instruction Interrupt, and the New PSW for the Illegal Instruction Interrupt becomes the current PSW.

8.1.2 Protect Mode Violation Interrupt. When PSW Bit 7 is reset, the Processor is in Supervisor Mode and all user instructions are executable.

The Protect Mode Violation Interrupt occurs when execution of a Priviledged instruction is attemped while the Processor is in the Protect Mode (PSW Bit 7=1). An instruction is priviledged if it performs Input/Output or changes the Status Field (Bits 0:11) of PSW. The high order bit of DROM read-out, Bit 4, must be a one for the priviledged instructions. If PSW Bit 7 is set, RAH Bit 4 is allowed to set on DROM read-out Bit 4. The ROM Address Registers then specify non-existent ROM outside of the 2K allowed. Reading non-existent ROM yields a zero RD, resulting in an Illegal Instruction Interrupt.

8.1.3 Machine Malfunction Interrupt. The Machine Malfunction Interrupt occurs on Memory Parity errors or on Primary Power Fail if PSW Bit 2 is set. The emulator will also generate a Machine Malfunction Interrupt on Power Up if PSW Bit 2 is set.

Testable Primary Power Fail occurs if the Power Fail Detector circuit determines that primary line voltage is low or the Initialize Switch is depressed or the Power Switch is turned off. When any of the above events occur, a one millisecond timer is started and, if PSW Bit 2 is set, the Power Fail bit of the Machine Malfunction Alarm Register is set. See Figure 3. After the one millisecond time-out, the signal PPF is generated. The user may use the one millisecond interval to do any necessary system shut-down procedures.

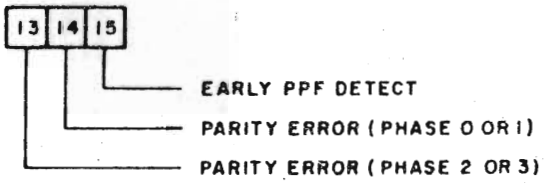


Figure 3. Machine Malfunction Alarm Register

During this interval, PSW Bit 2 may be set again as the Machine Malfunction Interrupt is only taken once. After the time-out, the signal PPF occurs causing the micro-program to save the PSW and LOC and the General Registers and then initialize the system.

If the Memory Parity option is present, the Parity Bit of each halfword in memory is set or reset to maintain odd parity. The Parity Bit is generated on every Memory Write or Priviledged Write and checked on every Memory Read.

If a parity error occurs and PSW Bit 2 is set, the parity error flags in the Alarm Register are set to indicate the Phase the Processor was in when the error occurred.

When Phase 2 is exited, the state of the Machine Malfunction Alarm Register, along with other interrupts, is tested. If any alarm bit is set, the Processor is forced to Phase 3 and the ROM Address Registers are set to X'010'.

The Interrupt Service Subroutine sorts interrupts by priority. Machine Malfunction is second to Primary Power Fail. If PPF is not active, the Machine Malfunction Interrupt is tested. If any bit in the Alarm Register is set, a PSW swap is performed and the bits that are set in the Alarm Register are ORed into the New PSW condition code. The Alarm Register is then cleared. This is done by the ALRM function of the DO Micro-instruction.

8.2 External Interrupts

If individually enabled by the user, a peripheral Device Controller is allowed to request Processor service when the device is ready to transfer data. The Processor has two separate classes of interrupts directly related to peripheral device handling. These are Data Channel Requests and Normal I/O Interrupts over the Multiplexed I/O Bus. If PSW Bit 1 is reset, normal I/O device interrupt signals are ignored. The signal remains pending, however, until PSW Bit 1 is set and the interrupt acknowledged.

8.2.1 Data Channel. The Data Channel feature of the Processor provides a means for a customer designed Device Controller to gain rapid access to core memory. When a memory access is required, the Controller activates the Data Channel Request Line (DC). This line is separate from the normal I/O ATN line and is not masked by PSW Bit 1. The micro-program tests the DC line before testing ATN, thereby placing it higher in priority.

The Processor acknowledges the Data Channel Interrupt by addressing Device Number 0 and also by activating the DCAK line.

The Data Channel Acknowledge (DCAK) line is daisy-chained through all devices connected to the Data Channel. The Device Controller closest to the Processor that originated a Data Channel interrupt captures the DCAK signal. That device becomes the On-Line device and controls the DRD Line. The DRD Line tells the micro-program whether a Memory Read (DRD = 1) or Memory Write (DRD = 0) is to be performed. If a Memory Read is requested, the micro-program does a data request. The Device Controller should then present a 16-bit memory address to the Data Lines. This address is copied into the Memory Address Register, memory is read and the memory data is gated out to the 16 Data Lines. If a memory write is requested, the micro-program does two data requests. The first collects the 16-bit address and the second brings in the 16-bits of data. The data is then written into core. If another memory cycle is desired, the device re-activates the DC line. Data Channel device controllers should not activate the HW line.

8.2.2 Normal I/O Interrupt. The Processor may service a normal I/O Interrupt in a variety of ways depending on the state of PSW Bit 4 and in-core tables. The interrupt handling is a function of the emulator and is described in the Reference Manual, Publication Number 29-219.

9. ADDITIONAL SPECIFICATIONS

The following is a list of Micro-programming constraints and general information:

1. On power up or following a C POW Micro-instruction, the Initialize relay is closed until voltages are at nominal levels. While the Initialize relay is closed, the signal SCLR (System Clear) sets up the Initialized state:

BANK	=	0
UT	=	0
RUN	=	0
RAH	=	0
RAS	=	0
RAL	=	0
RD	=	0
CTR	=	16
FLR	=	0
Phase	=	3

2. When Micro-programming arithmetic operations, remember that the A Register is the second operand and the Source Register is the first operand. This is important in subtract; the A Register is the subtrahend.

3. When micro-programming multiple-precision operations, the low order halfword(s) of the operands are considered to be all magnitude. The sign bit of a multiple-precision operand is Bit 0 of the most significant halfword.

   The hardware provides a cumulative flag affect to facilitate multiple-precision operations. Once the G or L flag becomes set, the G and L flags will never again be both zero unless the flag register is explicitly cleared. For this reason, prior to examining the least significant 16 bits of an operand, a D CLR must have occurred or the Flag Register loaded with zero. If G and L remain reset, the halfword was zero. If either G or L set, the halfword was not zero. As successively more significant halfwords are examined, if G and L stay reset, the partial operand is zero. Otherwise, G or L set indicates non-zero. When the most significant 16 bits are examined, G and L are still reset if the entire operand is zero or, if not zero, the G and L flags reflect the sign of the entire operand.

BEFORE G	BEFORE L	RESULT OF ARITHMETIC OR LOGICAL OPERATION	AFTER G	AFTER L
0	0	0000 0000 0000 0000	0	0
0	0	0000 0011 0101 0000	1	0
0	0	1000 1110 0100 1100	0	1
0	1	0000 0000 0000 0000	1	0
0	1	0000 0011 0101 0000	1	0
0	1	1000 1110 0100 1100	0	1
1	0	0000 0000 0000 0000	1	0
1	0	0000 0011 0101 0000	1	0
1	0	1000 1110 0100 1100	0	1

4. Flags are not changed in any immediate operation unless the FLR is the explicit destination.

5. If the FLR is the destination in an instruction that normally sets flags, the FLR will contain the OR of the low order 4-bits of the result and the result flags.

6. Specifying Carry Out (CO) is reasonable only on shifts or Add or Subtract. If Carry Out is specified on the logical operations (N, O, X), Carry will reset. Specifying Carry In (CI) has no affect on logical operations.

7. To implement a transfer within a micro-program, special care should be taken in the loading of the ROM address registers (RAH, RAL). The ROM decodes the address from the RAL and the page from the inner rank RAS. RAS is loaded from RAH whenever RAL is loaded or a Branch is taken. Loading RAH has no immediate affect on the address for the ROM. Before loading RAL, RAH must contain the correct page number. Addresses generated the D0 micro-instruction set both RAH and RAS.

8. RAL should not be the destination in an I/O operation.

9. The instruction L MAR, MDR, C8 can not be reliably executed.

```
                    * 05-038
                    * MODEL 70 DROM DATA
0000  0000               DC    '000'
0001  0108               DC    '108'       BALR
0002  010C               DC    '10C'       BTCR
0003  0114               DC    '114'       BFCR
0004  0132               DC    '132'       NHR
0005  0138               DC    '138'       CLHR
0006  013E               DC    '13E'       OHR
0007  0144               DC    '144'       XHR
0008  014A               DC    '14A'       LHR
0009  0150               DC    '150'       CHR
000A  015B               DC    '15B'       AHR
000B  0163               DC    '163'       SHR
000C  022C               DC    '22C'       MHR
000D  0253               DC    '253'       DHR
000E  015A               DC    '15A'       ACHR
000F  0162               DC    '162'       SCHR
```

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INTERDATA, INC.

```
                        ORG     '20'
0020  029                DC      '291'       LBS
0021  029                DC      '291'       BTFS
0022  028                DC      '285'       BFBS
0023  028                DC      '285'       BFFS
0024  01E8               DC      '1E8'       LIS
0025  01E8               DC      '1E8'       LCS
0026  01EF               DC      '1EF'       AIS
0027  01F3               DC      '1F3'       SIS
0028  02A2               DC      '2A2'       LER
0029  028                DC      '287'       CER
002A  028                DC      '287'       AER
002B  0286               DC      '286'       SER
002C  028                DC      '287'       MER
002D  028                DC      '287'       DER
002E  00                 DC      '000'       FXR TRAP
002F  00                 DC      '000'       FLR TRAP
```

```
                        ORG     '40'
0040    012E            DC      '12E'           STH
0041    0109            DC      '109'           BAL
0042    0110            DC      '110'           BTC
0043    0118            DC      '118'           BFC
0044    0134            DC      '134'           NH
0045    013A            DC      '13A'           CLH
0046    0140            DC      '140'           OH
0047    0146            DC      '146'           XH
0048    014C            DC      '14C'           LH
0049    014F            DC      '14F'           CH
004A    015E            DC      '15E'           AH
004B    0166            DC      '166'           SH
004C    022B            DC      '22B'           MH
004D    0252            DC      '252'           DH
004E    015D            DC      '15D'           ACH
004F    0165            DC      '165'           SCH
```

```
                    ORG     '60'
0060  0294           DC      '294'       STE
0061  016A           DC      '16A'       AHM
0062  0000           DC      '000'       AU TRAP
0063  0000           DC      '000'       SU TRAP
0064  0592           DC      '592'       ATL
0065  0592           DC      '592'       ABL
0066  0453           DC      '453'       RTL
0067  0453           DC      '453'       RBL
0068  02A5           DC      '2A5'       LE
0069  02BB           DC      '2BB'       CE
006A  02BB           DC      '2BB'       AE
006B  02BA           DC      '2BA'       SE
006C  02BB           DC      '2BB'       ME
006D  02BB           DC      '2BB'       DE
006E  0000           DC      '000'       FX TRAP
006F  0000           DC      '000'       FL TRAP
```

```
                        ORG     '90'
0090    0172            DC      '172'       SRLS
0091    0178            DC      '178'       SLLS
0092    018F            DC      '18F'       STBR
0093    0199            DC      '199'       LBR
0094    01A6            DC      '1A6'       EXBR
0095    08DD            DC      '8DD'       EPSR  *
0096    0A00            DC      'A00'       WBR   *
0097    0A01            DC      'A01'       RBR   *
0098    0C00            DC      'C00'       WHR   *
0099    0C07            DC      'C07'       RHR   *
009A    09A8            DC      '9A8'       WDR   *
009B    09AF            DC      '9AF'       RDR   *
009C    024B            DC      '24B'       MHUR
009D    09B8            DC      '9B8'       SSR   *
009E    09C3            DC      '9C3'       OCR   *
009F    09B7            DC      '9B7'       AIR   *
```

```
                        ORG     'C0'
00C0  011C              DC      '11C'           BXH
00C1  011C              DC      '11C'           BXLE
00C2  08DA              DC      '8DA'           LPSW
00C3  016F              DC      '16F'           THI
00C4  0134              DC      '134'           NHI
00C5  013A              DC      '13A'           CLHI
00C6  0140              DC      '140'           OHI
00C7  0146              DC      '146'           XHI
00C8  014C              DC      '14C'           LHI
00C9  014F              DC      '14F'           CHI
00CA  015E              DC      '15E'           AHI
00CB  0166              DC      '166'           SHI
00CC  0172              DC      '172'           SRHL
00CD  0178              DC      '178'           SLHL
00CE  017E              DC      '17E'           SRHA
00CF  0186              DC      '186'           SLHA
```

```
                        ORG     'D0'
00D0    00A9            DC      '0A9'           STM
00D1    00C0            DC      '0C0'           LM
00D2    0195            DC      '195'           STB
00D3    0198            DC      '198'           LB
00D4    019F            DC      '19F'           CLB
00D5    09CA            DC      '9CA'           AL      *
00D6    0A06            DC      'A06'           WB      *
00D7    0A07            DC      'A07'           RB      *
00D8    0C01            DC      'C01'           WH      *
00D9    0C0E            DC      'C0E'           RH      *
00DA    09AB            DC      '9AB'           WD      *
00DB    09B2            DC      '9B2'           RD      *
00DC    024A            DC      '24A'           MHU
00DD    09BD            DC      '9BD'           SS      *
00DE    09C6            DC      '9C6'           OC      *
00DF    09BC            DC      '9BC'           AI      *
```

```
                        ORG     'E0'
00E0  0000              DC      '000'
00E1  0486              DC      '486'       SVC
00E2  0857              DC      '857'       SINT *
00E3  0000              DC      '000'
00E4  0000              DC      '000'
00E5  0000              DC      '000'
00E6  0000              DC      '000'
00E7  0000              DC      '000'
00E8  0000              DC      '000'
00E9  0000              DC      '000'
00EA  0439              DC      '439'       RRL
00EB  0446              DC      '446'       RLL
00EC  0416              DC      '416'       SRL
00ED  041E              DC      '41E'       SLL
00EE  0426              DC      '426'       SRA
00EF  042F              DC      '42F'       SLA
00F0                    END
```

```
                * COPYRIGHT INTERDATA INC., MAY 1972                                    R7000020
                * MAY 5, 1972  IRA GABBERT                                              R7000030
                *                                                                       R7000040
0000  0000  INITIAL DC    '0000'          IRAP                                        R7000050
0001  5198        L     RAL,L(INTENT)     POWER UP                                    R7000060
                *                                                                       R7000070
                *                                                                       R7000080
                *                                                                       R7000090
                * PHASE 1 ENTRY POINT, INDEXED RS                                      R7000100
0002  CAA7  AMODRS  A     MDR,MDR         FORM EFFECTIVE OPERAND                      R7000110
0003  00C2        D     PC,CLR            GO TO PHASE 2                               R7000120
                *                                                                       R7000130
                *                                                                       R7000140
                * PHASE 1 ENTRY POINT, UNINDEXED RX                                    R7000150
0004  45A3  NMODRX  L     MAR,MDR         'A' TO MAR                                  R7000160
0005  08C2        D     PC,MR,CLR         FETCH OP,GO TO PHASE 2                      R7000170
                *                                                                       R7000180
                *                                                                       R7000190
                * PHASE 1 ENTRY POINT, INDEXED RX                                      R7000200
0006  C5A7  AMODRX  A     MAR,MDR         'A+(X2)' TO MAR                             R7000210
0007  08C2        D     PC,MR,CLR         FETCH OP, GO TO PHASE 2                     R7000220
0008  0000        DC    '0000'          FILLER                                        R7000230
0009  0000        DC    '0000'          FILLER                                        R7000240
```

```
                * COMMON PHASE 3 ENTRY POINT                                    R7000255
                *                                                               R7000260
000A  5802  ABORT   L     AR,'2'                                                R7000270
000B  1814          C     CUT+CB                                                R7000280
000C  E334          S     LOC,LOC,NC                                            R7000290
000D  2001          T     OP                  TEST FORMAT                       R7000300
000E  3110          B     L,P3HELP            SHORT FORMAT                      R7000310
000F  E334          S     LOC,LOC,NC          LONG FORMAT                       R7000320
                *                                                               R7000330
                * DETERMINE NATURE OF INTERRUPT                                 R7000340
                *                                                               R7000350
0010  21B0  P3HELP  T     MALF+PPF+CATN+SNGL                                    R7000360
0011  3238          B     G,HELP                                                R7000370
0012  2008          T     DC                                                    R7000380
0013  32E1          B     G,DCR               DATA CHANNEL REQUEST              R7000390
                *                                                               R7000400
                * ASSUME I/O ATTENTION                                          R7000410
0014  444C  TEST    L     FLR,PSW,CS+NC       TEST PSW04                        R7000420
0015  3828          B     C,HSSVC             IMMEDIATE INTERRUPT               R7000430
                *                                                               R7000440
                * IF PSW04 RESET, NORMAL INTERRUPT SERVICE                      R7000450
0016  5540          L     MAR,L(OIPSW)                                          R7000460
                *                                                               R7000470
                * GENERALIZED PSW SWAP                                          R7000480
                *                                                               R7000490
0017  4A43  GENSWP  L     MDR,PSW             STORE OLD STATUS                  R7000500
0018  1C00          C     PW                  PROTECT OVERRIDE                  R7000510
0019  5802          L     AR,'2'                                                R7000520
001A  C550          A     MAR,MAR,NF+NC                                         R7000530
001B  4A33          L     MDR,LOC                                               R7000540
001C  1C14          C     PW+CB+CUT           STORE OLD LOCCNT                  R7000550
001D  C354          A     LOC,MAR,NC                                            R7000560
001E   A02          D     MR+INC              FETCH NEW STATUS                  R7000570
                *                                                               R7000580
                *                                                               R7000590
001F  42A0  LPST    L     PSW,MDR,NC          LOAD STATUS                       R7000600
0020  3902          D     MR+JAM              LOAD CC, FETCH NEW LOC            R7000610
0021  43A3          L     LOC,MDR             LOAD LOCCNT                       R7000620
                *                                                               R7000630
0022  444F  TEST1   L     FLR,PSW,CS          TEST PSW 06                       R7000640
0023  3249          B     G,USRE8L            QUEUE SVC ENABLE                  R7000650
                *                                                               R7000660
0024  4849  TEST2   L     AR,PSW,SL+CO        TEST PSW 00                       R7000670
0025  385A          B     C,WAIT                                                R7000680
                *                                                               R7000690
0026  4533  P3EXIT  L     MAR,LOC             ADRS NEXT INSTR                   R7000700
0027  9AC2          D     PC+MR+INC+CLR       GO                                R7000710
                *                                                               R7000720
                *                                                               R7000730
                *                                                               R7000740
0028  4681  HSSVC   L     SRH,IO,ACK          ACKNOWLEDGE                       R7000750
                *                                                               R7000760
0029  4868  IOSVC   L     AR,SRH,SL+NC        2X DEVICE NUMBER                  R7000770
002A  D5D0          A     MAR,L(SPTA8L)       INDEX SVC PNTR TABLE              R7000780
002B  1814          C     MR+CUT+CB           FETCH SERVICE POINTER             R7000790
                *                                                               R7000800
                *                                                               R7000810
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002C  5005  DOIT    L     RAH,H(ISBSVC)   OFF PAGE ----                R7000820
002D  5802          L     AR,'2'                                        R7000830
002E  44A3          L     FLR,MDR         TEST SVC PNTR BIT 15          R7000840
002F  45A3          L     MAR,MDR                                       R7000850
0030  3100          D     L,ISBSVC        PROCESS ISB                   R7000860
                  * IMMEDIATE INTERRUPT                                 R7000870
0031  4A43          L     MDR,PSW         STORE OLD STATUS              R7000880
0032  1C00          C     PW              PROTECT OVERRIDE              R7000890
0033  C550          A     MAR,MAR,NF+NC                                 R7000900
0034  4A33          L     MDR,LOC                                       R7000910
0035  1C00          C     PW              STORE LOCATION COUNT          R7000920
0036  C354          A     LOC,MAR,NC                                    R7000930
0037  0A02          D     MR+INC          FETCH NEW PSW STATUS          R7000940
0038  42A0          L     PSW,MDR,NC                                    R7000950
                  * NO NEW LOC VALUE IS NEEDED                          R7000960
                  * NEXT SEQUENTIAL ADRS CONTAINS FIRST                 R7000970
                  * INSTRUCTION OF SERVICE SUBROUTINE.                  R7000980
                  *                                                     R7000990
0039  4BC2          D     PC+MR+INC+JAM+CLR DO IT                       R7001000
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                *                                                                   R7001020
003A  4012  ENTHLP  D     CWA             RESET WAIT INDICATOR                      R7001030
                *                                                                   R7001040
0038  2010  HELP    T     PPF                                                       R7001050
003C  329E          B     G,PWRDWN                                                  R7001060
003D  5538          L     MAR,L(OMPSW)                                              R7001070
003E  2020          T     MALF                                                      R7001080
003F  32F0          B     G,MMFSWP        MACHINE MALFUNCTION INTERRUPT             R7001090
                *                                                                   R7001100
0040  2180          T     CATN+SNGL                                                 R7001110
0041  3268          B     G,CONSER                                                  R7001120
                *                                                                   R7001130
0042  2130  TEST3   T     PPF+MALF+CATN                                             R7001140
0043  3238          B     G,HELP                                                    R7001150
0044  2008  TEST4   T     DC                                                        R7001160
0045  32E1          B     G,DCR           DATA CHANNEL REQUEST                      R7001170
                *                                                                   R7001180
0046  2400          T     ATN                                                       R7001190
0047  3214          B     G,TEST                                                    R7001200
0048  5124          L     RAL,L(TEST2)                                              R7001210
                *                                                                   R7001220
                * QUEUE SERVICE INTERRUPT ENABLED, TEST LIST                        R7001230
                *                                                                   R7001240
0049  5580  USRE8L  L     MAR,'80'                                                  R7001250
004A  1804          C     MR+CB           FETCH POINTER                             R7001260
004B  58FF          L     AR,'FF'                                                   R7001270
004C  5400          L     FLR,'0'                                                   R7001280
004D  45A3          L     MAR+MDR         LIST START ADRS                           R7001290
004E  1800          C     MR                                                        R7001300
004F  5582          L     MAR,'82'        ADRS QUEUE SVC. PSW                       R7001310
0050  88A7          N     AR+MDR          TEST NO,USED TALLY                        R7001320
0051  3217          B     G,GENSWP        NOT EMPTY, DO SWAP                        R7001330
                *                                                                   R7001340
0052  5124          L     RAL,L(TEST2)    LIST EMPTY,NO INTERRUPT                   R7001350
                *                                                                   R7001360
                * CHECK FLPT ARITHMETIC FAULT ENABLE                                R7001370
                *                                                                   R7001380
0053  5528  FLPEN8  L     MAR,L(OFPSW)                                              R7001390
0054  444F          L     FLR,PSW,CS      TEST PSW 05                               R7001400
0055  3417          B     V,GENSWP        DO SWAP                                   R7001410
0056  5126          L     RAL,L(P3EXIT)                                             R7001420
                *                                                                   R7001430
                * SIMULATE INTERRUPT                                                R7001440
                *                                                                   R7001450
0057  58FF  SINT    L     AR,'FF'                                                   R7001460
0058  86A7          N     SRH,MDR         ISOLATE DEVICE NR.                        R7001470
0059  5129          L     RAL,L(IOSVC)                                              R7001480
                *                                                                   R7001490
                * INTERRUPTABLE WAIT                                                R7001500
                *                                                                   R7001510
005A  C062  WAIT    D     SWA+CLR         SET WAIT INDICATOR                        R7001520
005B  2538  WAIT1   T     MALF+PPF+CATN+DC+ATN                                      R7001530
005C  3158          B     L,WAIT1         LOOP                                      R7001540
                *                                                                   R7001550
005D  3012          D     CWA             RESET WAIT INDICATOR                      R7001560
005E  5110          L     RAL,L(P3HELP)                                             R7001570
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                    * CONSOLE SERVICE                                                   R7001585
005F  4490  DISPLY  L     FLR,IR,NC                                                     R7001590
0060  3890          B     C,REGDIS      GENERAL REGISTER                                R7001600
0061  3489          B     V,PSWDIS      PROGRAM STATUS WORD                             R7001610
0062  3296          B     G,INSDIS      INSTRUCTION REGISTER                            R7001620
                    *                                                                   R7001630
                    * IDLE LOOP                                                        R7001640
                    *                                                                   R7001650
0063  0062  IDLE    D     SWA+CLR       SET WAIT INDICATOR                              R7001660
                    *                                                                   R7001670
0064  2010  IDLE1   T     PPF                                                           R7001680
0065  323A          B     G,ENTHLP                                                      R7001690
0066  2100          T     CATN                                                          R7001700
0067  3164          B     L,IDLE1       LOOP                                            R7001710
                    *                                                                   R7001720
0068  3012          D     CWA           RESET WAIT INDICATOR                            R7001730
0069  2080          T     SNGL                                                          R7001740
006A  3278          B     G,CLRWIT      VARIABLE,EXIT                                   R7001750
                    *                                                                   R7001760
                    *                                                                   R7001770
006B  5601  CONSER  L     SRH,'1'       DISPLAY DEVICE NR.                              R7001780
006C  4861          L     IO,SRH,ADRS                                                   R7001790
006D  4983          L     IR,IO,STAT    STATUS TO IR                                    R7001800
006E  2080          T     SNGL                                                          R7001810
006F  325F          B     G,DISPLY      VARIABLE MODE                                   R7001820
0070  44C3          L     FLR,IR4       INTERPRET                                       R7001830
0071  317F          B     L,MWSL        MEMORY WRITE OR ADDRESS                         R7001840
0072  327C          B     G,MREAD       MEMORY READ                                     R7001850
0073  345F          B     V,DISPLY      SINGLE OR HALT                                  R7001860
                    *                                                                   R7001870
                    * RUN MODE                                                         R7001880
0074  4490          L     FLR,IR,NC     TEST REGISTER SELECT                            R7001890
0075  3F78          B     CVGL,CLRWIT                                                   R7001900
                    *                                                                   R7001910
                    * NO REGISTER SELECTED                                             R7001920
0076  444C          L     FLR,PSW,CS+NC TEST PSW04                                      R7001930
0077  3829          B     C,IOSVC       CONSOLE INTERRUPT                               R7001940
                    * SPECIAL INTERRUPT HANDLER NOT ENABLED                           R7001950
                    *                                                                   R7001960
0078  4248  CLRWIT  L     PSW,PSW,SL+NC                                                 R7001970
0079  4244          L     PSW,PSW,SR+NC RESET WAIT BIT                                  R7001980
007A  4530          L     MAR,LOC,NC    ADRS NEXT INSTR                                 R7001990
007B  0AC2          D     P2N           GO                                              R7002000
                    *                                                                   R7002010
                    *                                                                   R7002020
007C  4533  MREAD   L     MAR,LOC       ADRS OF DATA                                    R7002030
007D  0A02          D     MR+INC        FETCH                                           R7002040
007E  5184          L     RAL,L(DISMEM) AND SHOW                                        R7002050
                    *                                                                   R7002060
                    *                                                                   R7002070
007F  4AB2  MWSL    L     MDR,IO,DR     LOW BYTE TO MDL                                 R7002080
0080  4533          L     MAR,LOC       ADRS TO MAR MUST BE EVEN                        R7002090
0081  4ABE          L     MDR,IO,DR+CS  HIGH BYTE TO MDH                                R7002100
0082  3287          B     G,SL          STATUS 02 = ADRS                                R7002110
                    *                                                                   R7002120
                    * MEMORY WRITE                                                     R7002130
0083  E02           D     PW+INC        STORE IT                                        R7002140
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                *                                                              R7002150
                * DISPLAY MEMORY REGISTERS                                     R7002160
0084  4653  DISMEM  L     SRH,MAR          2ND OUTPUT REGISTER                 R7002170
0085  47A3           L     SRL,MDR          1ST OUTPUT REGISTER                 R7002180
0086  518B           L     RAL,L(OUTDIS)                                        R7002190
                *                                                              R7002200
                *                                                              R7002210
0087  4AA4  SL       L     MDR,MDR,SR,NC    RESET BIT 15                        R7002220
0088  43A8           L     LOC,MDR,SL,NC    TO GUARANTEE EVEN                   R7002230
                *                                                              R7002240
                *                                                              R7002250
0089  4643  PSWDIS  L     SRH,PSW          2ND OUTPUT REGISTER                 R7002260
008A  4733           L     SRL,LOC          1ST OUTPUT REGISTER                 R7002270
                *                                                              R7002280
                * OUTPUT DATA TO DISPLAY                                       R7002290
                *                                                              R7002300
008B  4872  OUTDIS  L     IO,SRL,DA        DISPLAY 2, LOW                      R7002310
008C  487E           L     IO,SRL,DA,CS     DISPLAY 2, HIGH                     R7002320
008D  4862           L     IO,SRH,DA        DISPLAY 1, LOW                      R7002330
008E  486E           L     IO,SRH,DA,CS     DISPLAY 1, HIGH                     R7002340
008F  5163           L     RAL,L(IDLE)                                          R7002350
                *                                                              R7002360
                *                                                              R7002370
0090  4998  REGDIS  L     IR,IR,SL,NC                                          R7002380
0091  46D3           L     SRH,YS           2ND OUTPUT REGISTER                 R7002390
0092  5801           L     AR,'1'                                               R7002400
0093  6997           O     IR,IR                                                R7002410
0094  47D3           L     SRL,YS           1ST OUTPUT REGISTER                 R7002420
0095  518B           L     RAL,L(OUTDIS)                                        R7002430
                *                                                              R7002440
                *                                                              R7002450
0096  4533  INSDIS  L     MAR,LOC                                              R7002460
0097  1800           C     MR               FETCH MS 16 BITS                    R700247
0098  5802           L     AR,'2'                                               R700248
0099  46A3           L     SRH,MDR          2ND OUTPUT REGISTER                 R7002490
009A  C554           A     MAR,MAR,NC                                           R7002500
009B  1800           C     MR                                                   R7002510
009C  47A3           L     SRL,MDR          1ST OUTPUT REGISTER                 R7002520
009D  518B           L     RAL,L(OUTDIS)                                        R7002530
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                    * POWER DOWN SEQUENCE                                                   R7002545
009F  5526  PWRDWN  L       MAR,L(LOC)                                                      R7002550
009F  4A33          L       MDR,LOC                                                         R7002560
00A0  1C00          C       PW              SAVE LOCCNT                                     R7002570
00A1  5524          L       MAR,L(PSW)                                                      R7002580
00A2  4A43          L       MDR,PSW                                                         R7002590
00A3  1C00          C       PW              SAVE PSW                                        R7002600
00A4  5522          L       MAR,L(PNTR)                                                     R7002610
00A5  1820          C       MR+SUT          FETCH REGISTER SAVE POINTER                     R7002620
00A6  5200          L       PSW,'0'         FORCE SUPERVISOR MODE                           R7002630
00A7  5900          L       IR,'0'                                                          R7002640
00A8  45A3          L       MAR,MDR                                                         R7002650
                    *                                                                       R7002660
                    *                                                                       R7002670
                    * STORE MULTIPLE                                                        R7002680
                    *                                                                       R7002690
00A9  48C3  STM     L       AR,IR4          YD FIELD TO AR                                  R7002700
00AA  FC10          S       CTR,'10'        2'S COMP & SET COUNT                            R7002710
00AB  4633          L       SRH,LOC         SAVE LOC                                        R7002720
00AC  5810          L       AR,'10'                                                         R7002730
00AD  4353          L       LOC,MAR                                                         R7002740
                    *                                                                       R7002750
00AE  4AE3  STMLP   L       MDR,YD                                                          R7002760
00AF  0602          D       MW+INC          SAVE REGISTER                                   R7002770
00B0  C997          A       IR,IR           BUMP YD FIELD                                   R7002780
00B1  30AE          B       CTR,STMLP       DECREMENT CTR                                   R7002790
                    *                                                                       R7002800
00B2  4363          L       LOC,SRH         RESTORE LOC                                     R7002810
00B3  2040          T       UT                                                              R7002820
00B4  3126          B       L,P3EXIT                                                        R7002830
00B5  0003          D       POW             SYSTEM RESET                                    R7002840
                    *                                                                       R7002850
                    * PROCESSOR LOCKS ON POWER DOWN                                         R7002860
                    * POWER UP RESTART AT LOCATION '000'                                    R7002870
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                    * INITIALIZE/POWER UP SEQUENCE                                  R7002885
                    *                                                               R7002887
0086  5524  INTENT  L     MAR,L(PSW)                                                R7002890
0087  1800          C     MR                FETCH PSW VALUE                         R7002900
0088  42A0          L     PSW,MDR,NC        UPDATE STATUS                           R7002910
0089  5526          L     MAR,L(LOC)                                                R7002920
008A  0902          D     MR+JAM            UPDATE CC, FETCH LOC                    R7002930
008B  43A3          L     LOC,MDR                                                   R7002940
008C  5522          L     MAR,L(PNTR)                                               R7002950
008D  1820          C     MR+SUT            REGISTER SAVE POINTER                   R7002960
008E  5900          L     IR,'0'                                                    R7002970
008F  45A3          L     MAR,MDR                                                   R7002980
                    *                                                               R7002990
                    *                                                               R7003000
                    * LOAD MULTIPLE                                                 R7003010
                    *                                                               R7003020
00C0  48C3  LM      L     AR,IR4            YD FIELD TO AR                          R7003030
00C1  FC10          S     CTR,'10'          2'S COMP & SET COUNT                    R7003040
00C2  4633          L     SRH,LOC           SAVE LOC                                R7003050
00C3  5810          L     AR,'10'                                                   R7003060
00C4  4353          L     LOC,MAR                                                   R7003070
                    *                                                               R7003080
00C5  0A02  LMLOOP  D     MR+INC            FETCH                                   R7003090
00C6  4EA3          L     YD,MDR            LOAD REGISTER                           R7003100
00C7  C997          A     IR,IR             INCREMENT YD FIELD                      R7003110
00C8  B0C5          B     CTR,LMLOOP                                                R7003120
                    *                                                               R7003130
00C9  4363          L     LOC,SRH           RESTORE LOC                             R7003140
00CA  2040          T     UT                                                        R7003150
00CB  3126          B     L,P3EXIT                                                  R7003160
                    *                                                               R7003170
                    *                                                               R7003180
00CC  5601          L     SRH,'1'           DISPLAY DEVICE NR.                      R7003190
00CD  4861          L     IO,SRH,ADRS                                               R7003200
00CE  4983          L     IR,IO,STAT        DISPLAY STATUS TO IR                    R7003210
00CF  44C3          L     FLR,IR4           TEST MODE                               R7003220
00D0  37D7          B     VGL,NRUN          NOT RUN                                 R7003230
                    *                                                               R7003240
00D1  5538          L     MAR,L(OMPSW)                                              R7003250
00D2  2200          T     ARST              RESTART                                 R7003260
00D3  315F          B     L,DISPLY                                                  R7003270
00D4  494F          L     IR,PSW,CS                                                 R7003280
00D5  44C3          L     FLR,IR4           TEST PSW02                              R7003290
00D6  3217          B     G,GENSWP          DO SWAP                                 R7003300
                    *                                                               R7003310
00D7  2200  NRUN    T     ARST                                                      R7003320
00D8  3268          B     G,CONSER                                                  R7003330
00D9  515F          L     RAL,L(DISPLY)                                             R7003340
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                *                                                          R7003360
                * LOAD PROGRAM STATUS WORD                                 R7003370
                *                                                          R7003380
00DA  43A3  LPSW    L     LOC,MDR       A+(X2)                             R7003390
00D8  0A02          D     MR+INC        FETCH NEW PSW VALUE                R7003400
00DC  511F          L     RAL,L(LPST)                                      R7003410
                *                                                          R7003420
                *                                                          R7003430
                * EXCHANGE PROGRAM STATUS                                  R7003440
                *                                                          R7003450
00DD  4E43  EPSR    L     YD,PSW        STATUS TO R1                       R7003460
00DE  42D0          L     PSW,YS,NC     R2 TO PSW                          R7003470
00DF  0102          D     JAM           LOAD CC                            R7003480
00E0  5122          L     RAL,L(TEST1)                                     R7003490
                *                                                          R7003500
                * DATA CHANNEL REQUEST                                     R7003510
                *                                                          R7003520
00E1  4B80  DCR     L     IO,NULL,DCAK  DATA CHANNEL ACKNOWLEDGE           R7003530
00E2  2004          T     DRD           READ OR WRITE                      R7003540
00E3  31E8          B     L,DCREAD                                         R7003550
                *                                                          R7003560
                * DATA CHANNEL WRITE                                       R7003570
00E4  4582  DCWRIT  L     MAR,IO,DR     HALFWORD ADRS TO MAR               R7003580
00E5  1804          C     MR+CB         FETCH                              R7003590
00E6  4BA2          L     IO,MDR,DA     OUTPUT HALFWORD DATA               R7003600
00E7  5142          L     RAL,L(TEST3)                                     R7003610
                *                                                          R7003620
                * DATA CHANNEL READ                                        R7003630
00E8  4582  DCREAD  L     MAR,IO,DR     HALFWORD ADRS TO MAR               R7003640
00E9  4AB2          L     MDR,IO,DR     HALFWORD DATA TO MDR               R7003650
00EA  1C04          C     PW+CB         STORE IT                           R7003660
00EB  5142          L     RAL,L(TEST3)                                     R7003670
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                        ORG     '00F0'                                          R7003671
00F0  4A43  MMFSWP      L       MDR,PSW                                         R7003676
00F1  1C00              C       PW              SAVE PSW                        R7003677
00F2  5802              L       AR,'2'                                          R7003678
00F3  C550              A       MAR,MAR,NF+NC                                   R7003679
00F4  4A33              L       MDR,LOC                                         R7003680
00F5  1C14              C       PW+CB+CUT       SAVE LOC                        R7003681
00F6  C354              A       LOC,MAR,NC                                      R7003682
00F7  9A02              D       MR+INC                                          R7003683
00F8  42A0              L       PSW,MDR,NC      LOAD NEW STATUS                 R7003684
00F9  090A              D       MR+JAM+ALRM     FLR OR ALARM TO CC              R7003685
00FA  43A3              L       LOC,MDR         LOAD NEW LOC                    R7003686
00FB  5122              L       RAL,L(TEST1)                                    R7003687
                        *                                                       R7003688
                        *                                                       R7003690
                        *                                                       R7003697
0022  PNTR      EQU     '0022'                                                  R7003700
0024  PSW       EQU     '0024'                                                  R7003710
0026  LOC       EQU     '0026'                                                  R7003720
0028  OFPSW     EQU     '0028'                                                  R7003730
0030  OTPSW     EQU     '0030'                                                  R7003740
0038  OMPSW     EQU     '0038'                                                  R7003750
0040  OIPSW     EQU     '0040'                                                  R7003760
0048  ODPSW     EQU     '0048'                                                  R7003770
00D0  SPTABL    EQU     '00D0'                                                  R7003780
                        *                                                       R7003790
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                        ORG   '0100'                                          R7003800
                    *                                                         R7003810
                    * ILLEGAL INSTRUCTION INTERRUPT                           R7003820
                    *                                                         R7003830
0100  5802  ILLEG   L     AR,'2'                                              R7003840
0101  2001          T     OP                                                  R7003850
0102  3104          B     L,ILEG1         RR                                  R7003860
0103  5804          L     AR,'4'                                              R7003870
0104  E334  ILEG1   S     LOC,LOC,NC      DECREMENT LOCCNT                    R7003880
0105  5530          L     MAR,L(OTPSW)                                        R7003890
0106  5000          L     RAH,H(GENSWP)                                       R7003900
0107  5117          L     RAL,L(GENSWP)   PSW SWAP                            R7003910
                    *                                                         R7003920
                    *                                                         R7003930
                    *                                                         R7003940
                    * BRANCH INSTRUCTIONS                                     R7003950
                    *                                                         R7003960
                    * BRANCH AND LINK                                         R7003970
0108  45D3  BALR    L     MAR,YS          ADRS TO MAR                         R7003980
0109  4E33  BAL     L     YD,LOC          LINK TO YD                          R7003990
010A  4353          L     LOC,MAR         DO BRANCH                           R7004000
010B  0AC2          D     P2N             GO                                  R7004010
                    *                                                         R7004020
                    * BRANCH ON TRUE CONDITION                                R7004030
010C  2002  BTCR    T     MSK                                                 R7004040
010D  310F          B     L,NRRB          NO BRANCH, EXIT                     R7004050
010E  43D3          L     LOC,YS          DO BRANCH                           R7004060
010F  0AC2  NRRB    D     P2N             GO                                  R7004070
                    *                                                         R7004080
0110  2002  BTC     T     MSK                                                 R7004090
0111  3130          B     L,NRXB          NO BRANCH EXIT                      R7004100
0112  4353          L     LOC,MAR         DO BRANCH                           R7004110
0113  0AC2          D     P2N             GO                                  R7004120
                    *                                                         R7004130
                    * BRANCH ON FALSE CONDITION                               R7004140
0114  2002  BFCR    T     MSK                                                 R7004150
0115  320F          B     G,NRRB          NO BRANCH,EXIT                      R7004160
0116  43D3          L     LOC,YS          DO BRANCH                           R7004170
0117  0AC2          D     P2N             GO                                  R7004180
                    *                                                         R7004190
0118  2002  BFC     T     MSK                                                 R7004200
0119  3230          B     G,NRXB          NO BRANCH,EXIT                      R7004210
011A  4353          L     LOC,MAR         DO BRANCH                           R7004220
011B  0AC2          D     P2N             GO                                  R7004230
                    *                                                         R7004240
                    *                                                         R7004250
                    * BRANCH ON INDEX                                         R7004260
011C  4890  BXLH    L     AR,IR,NC                                            R7004270
011D  449C          L     FLR,IR,CS+NC    OP DONW                             R7004280
011E  98F0          N     AR,'F0'                                             R7004290
011F  68C3          O     AR,IR4,NF       YD FIELD=YS FIELD                   R7004300
0120  D910          A     IR,'10'                                             R7004310
0121  47E3          L     SRL,YD          SRL=INCREMENT                       R7004320
0122  D920          A     IR,'20'                                             R7004330
0123  4873          L     AR,SRL                                              R7004340
0124  CDD0          A     YS,YS,NF+NC     ADD INCREMENT TO INDEX              R7004350
0125  48D3          L     AR,YS                                               R7004360
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0126  312A          B     L,XLE     BXLE                          R7004370
      * BXH
0127  E8E5          S     AR,YD,CO  COMPARAND MINUS INDEX         R7004390
0128  382C          B     C,BRANCH  DO BRANCH                     R7004400
0129  0AC2  NOBRAN D     P2N       NO BRANCH, GO                 R7004410
      *                                                         R7004420
012A  E8E5  XLE     S     AR,YD,CO  COMPARAND MINUS INDEX         R7004430
012B  3829          B     C,NOBRAN                                R7004440
012C  43A3  BRANCH  L     LOC,MDR   DO BRANCH                     R7004450
012D  0AC2          D     P2N       GO                            R7004460
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                    *                                                        R7004480
                    * STORE HALFWORD                                         R7004490
012E  4AE3  STH     L       MDR,YD          1ST OP TO MDR                    R7004500
012F  1400          C       MW              STORE IT                         R7004510
0130  4533  NRXB    L       MAR,LOC         ADRS NEXT INSTR                  R7004520
0131  0AC2          D       P2N             GO                               R7004530
                    *                                                        R7004540
                    * AND HALFWORD                                           R7004550
0132  8EE7  NHR     N       YD,YD           EXECUTE AND                      R7004560
0133  0BC2          D       P2J             GO                               R7004570
                    *                                                        R7004580
0134  48A3  NH      L       AR,MDR          2ND OP TO AR                     R7004590
0135  8EE7          N       YD,YD           EXECUTE AND                      R7004600
0136  4533          L       MAR,LOC         ADRS NEXT INSTR                  R7004610
0137  0BC2          D       P2J             GO                               R7004620
                    *                                                        R7004630
                    * COMPARE LOGICAL HALFWORD                               R7004640
0138  E8E5  CLHR    S       AR,YD,CO        SUB TO SET FLAGS                 R7004650
0139  0BC2          D       P2J             GO                               R7004660
                    *                                                        R7004670
013A  48A3  CLH     L       AR,MDR          2ND OP TO AR                     R7004680
013B  E8E5          S       AR,YD,CO        SUB TO SET FLAGS                 R7004690
013C  4530          L       MAR,LOC,NC      ADRS NEXT INSTR                  R7004700
013D  0BC2          D       P2J             GO                               R7004710
                    *                                                        R7004720
                    * OR HALFWORD                                            R7004730
013E  9EE7  OHR     O       YD,YD           EXECUTE OR                       R7004740
013F  0BC2          D       P2J             GO                               R7004750
                    *                                                        R7004760
0140  48A3  OH      L       AR,MDR          2ND OP TO AR                     R7004770
0141  6EE7          O       YD,YD           EXECUTE OR                       R7004780
0142  4533          L       MAR,LOC         ADRS NEXT INSTR                  R7004790
0143  0BC2          D       P2J             GO                               R7004800
                    *                                                        R7004810
                    * EXCLUSIVE OR HALFWORD                                  R7004820
0144  AEE7  XHR     X       YD,YD           EXECUTE XOR                      R7004830
0145  0BC2          D       P2J             GO                               R7004840
                    *                                                        R7004850
0146  48A3  XH      L       AR,MDR          2ND OP TO AR                     R7004860
0147  AEE7          X       YD,YD           EXECUTE XOR                      R7004870
0148  4533          L       MAR,LOC         ADRS NEXT INSTR                  R7004880
0149  0BC2          D       P2J             GO                               R7004890
                    *                                                        R7004900
                    * LOAD HALFWORD                                          R7004910
014A  6EDF  LHR     O       YD,YS,NA        LOAD & SET FLAGS                 R7004920
014B  0BC2          D       P2J             GO                               R7004930
                    *                                                        R7004940
014C  6EAF  LH      O       YD,MDR,NA       LOAD & SET FLAGS                 R7004950
014D  4533          L       MAR,LOC         ADRS NEXT INSTR                  R7004960
014E  0BC2          D       P2J             GO                               R7004970
                    *                                                        R7004980
                    * COMPARE HALFWORD (ARITHMETIC)                          R7004990
014F  48A3  CH      L       AR,MDR          2ND OP TO AR                     R7005000
0150  A6E7  CHR     X       SRH,YD          COMPARE SIGNS                    R7005010
0151  3156          B       L,DIFFER                                         R7005020
                    * SIGNS ALIKE                                           R7005030
0152  6400          L       FLR,'0'                                          R7005040
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0153  E8E7          S     AR,YD          SUB TO SET FLAGS          R7005050
0154  4530          L     MAR,LOC,NC     ADRS NEXT INSTR           R7005060
0155  0BC2          D     P2J            GO                        R7005070
                  * IF SIGNS DIFFER, SET FLAGS TO 1ST OP           R7005080
0156  48E9  DIFFER  L     AR,YD,SL,CO    1ST OP SIGN TO C          R7005090
0157  68EC          O     AR,YD,NA,NC    SET GL                    R7005100
0158  4530          L     MAR,LOC,NC     ADRS NEXT INSTR           R7005110
0159  0BC2          D     P2J            GO                        R7005120
                  *                                               R7005130
                  * ADD (WITH CARRY) HALFWORD                      R7005140
015A  4440  ACHR    L     FLR,PSW,NC     PROPOGATE FLAGS           R7005150
015B  CEE7  AHR     A     YD,YD          EXECUTE ADD               R7005160
015C  0BC2          D     P2J            GO                        R7005170
                  *                                               R7005180
015D  4440  ACH     L     FLR,PSW,NC     PROPOGATE FLAGS           R7005190
015E  48A0  AH      L     AR,MDR,NC      2ND OP TO AR              R7005200
015F  CEE7          A     YD,YD          EXECUTE ADD               R7005210
0160  4530          L     MAR,LOC,NC     ADRS NEXT INSTR           R7005220
0161  0BC2          D     P2J            GO                        R7005230
                  *                                               R7005240
                  * SUBTRACT (WITH CARRY) HALFWORD                 R7005250
0162  4440  SCHR    L     FLR,PSW,NC     PROPOGATE FLAGS           R7005260
0163  EEE7  SHR     S     YD,YD          EXECUTE SUBTRACT          R7005270
0164  0BC2          D     P2J            GO                        R7005280
                  *                                               R7005290
0165  4440  SCH     L     FLR,PSW,NC     PROPOGATE FLAGS           R7005300
0166  48A0  SH      L     AR,MDR,NC      2ND OP TO AR              R7005310
0167  EEE7          S     YD,YD          EXECUTE SUBTRACT          R7005320
0168  4530          L     MAR,LOC,NC     ADRS NEXT INSTR           R7005330
0169  0BC2          D     P2J            GO                        R7005340
                  *                                               R7005350
                  * ADD HALFWORD TO MEMORY                         R7005360
016A  48E3  AHM     L     AR,YD          1ST OP TO AR              R7005370
016B  CAA7          A     MDR,MDR        EXECUTE ADD               R7005380
016C  1400          C     MW             STORE RESULT              R7005390
016D  4530          L     MAR,LOC,NC     ADRS NEXT INSTR           R7005400
016E  0BC2          D     P2J            GO                        R7005410
                  *                                               R7005420
                  * TEST HALFWORD IMMEDIATE                        R7005430
016F  48E3  THI     L     AR,YD          1ST OP TO AR              R7005440
0170  88A7          N     AR,MDR                                   R7005450
0171  0BC2          D     P2J            GO                        R7005460
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                *                                                          R7005480
                * SHIFT INSTRUCTIONS                                       R7005490
                *                                                          R7005500
                * SHIFT RIGHT HALFWORD LOGICAL LONG OR SHORT               R7005510
0172  48A3  SRHL    L     AR,MDR                                           R7005520
0173  9C0F          N     CTR,'F'         LOAD CTR                         R7005530
0174  1240          C     RPT                                              R7005540
0175  4EE5          L     YD,YD,SR+CO     DO SHIFT                         R7005550
0176  6EEC          O     YD,YD,NA+NC     SET FLAGS                        R7005560
0177  68C2          D     P2J             GO                               R7005570
                *                                                          R7005580
                * SHIFT LEFT HALFWORD LOGICAL LONG OR SHORT                R7005590
0178  48A3  SLHL    L     AR,MDR                                           R7005600
0179  9C0F          N     CTR,'F'         LOAD CTR                         R7005610
017A  1240          C     RPT                                              R7005620
017B  4EE9          L     YD,YD,SL+CO     DO SHIFT                         R7005630
017C  6EEC          O     YD,YD,NA+NC     SET FLAGS                        R7005640
017D  68C2          D     P2J             GO                               R7005650
                *                                                          R7005660
                * SHIFT RIGHT HALFWORD ARITHMETIC                          R7005670
017E  48A3  SRHA    L     AR,MDR                                           R7005680
017F  9C0F          N     CTR,'F'         LOAD CTR                         R7005690
0180  4EE9          L     YD,YD,SL+CO     MOVE SIGN TO CARRY               R7005700
0181  1240          C     RPT                                              R7005710
0182  4EE6          L     YD,YD,SR+CI     DO SHIFT                         R7005720
0183  4EE7          L     YD,YD,SR        COMPENSATE PRESHIFT              R7005730
0184  6EEC          O     YD,YD,NA+NC     SET FLAGS                        R7005740
0185  68C2          D     P2J             GO                               R7005750
                *                                                          R7005760
                * SHIFT LEFT HALFWORD ARITHMETIC                           R7005770
0186  48A3  SLHA    L     AR,MDR                                           R7005780
0187  9C0F          N     CTR,'F'         LOAD CTR                         R7005790
0188  4EE9          L     YD,YD,SL+CO     SIGN TO CARRY FLAG               R7005800
0189  4887          L     AR,NULL,SR      COPY TO AR 00                    R7005810
018A  1240          C     RPT                                              R7005820
018B  4EE9          L     YD,YD,SL+CO                                      R7005830
018C  4EE4          L     YD,YD,SR+NC     COMPENSATE PRESHIFT              R7005840
018D  6EE4          O     YD,YD,NC        INSERT SIGN, SET FLAGS           R7005850
018E  68C2          D     P2J             GO                               R7005860
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                    •                                                          R7005880
                    • BYTE HANDLING INSTRUCTIONS                               R7005890
                    •                                                          R7005900
                    • STORE BYTE                                               R7005910
018F  98FF  STBR    N       AR,'FF'                                            R7005920
0190  A6D7          X       SRH,YS          RESET LO SECOND OP                 R7005930
0191  48E3          L       AR,YD                                              R7005940
0192  98FF          N       AR,'FF'         ISOLATE LO 1ST OP                  R7005950
0193  6D67          O       YS,SRH          INSERT                             R7005960
0194  8AC2          D       P2N             GO                                 R7005970
                    •                                                          R7005980
0195  4AEF  STB     L       MDR,YD,CS       INSERT BYTE                        R7005990
0196  1400          C       MW              RESTORE HALFWORD                   R7006000
0197  4533          L       MAR,LOC         ADRS NEXT INSTR                    R7006010
0198  7AC2          D       P2N             GO                                 R7006020
                    •                                                          R7006030
                    • LOAD BYTE                                                R7006040
0199  9EFF  LBR     N       YD,'FF'         LOAD LO 2ND OP                     R7006050
019A  8AC2          D       P2N             GO                                 R7006060
                    •                                                          R7006070
019B  48AF  LB      L       AR,MDR,CS       2ND OP TO AR                       R7006080
019C  9EFF          N       YD,'FF'         LOAD LO ONLY                       R7006090
019D  4533          L       MAR,LOC         ADRS NEXT INSTR                    R7006100
019E  8AC2          D       P2N             GO                                 R7006110
                    •                                                          R7006120
                    • COMPARE LOGICAL BYTE                                     R7006130
019F  48E3  CLB     L       AR,YD           1ST OP                             R7006140
01A0  96FF          N       SRH,'FF'        ISOLATE LO                         R7006150
01A1  48AF          L       AR,MDR,CS       2ND OP                             R7006160
01A2  98FF          N       AR,'FF'         ISOLATE BYTE                       R7006170
01A3  F865          S       AR,SRH,CO       SUB TO SET FLAGS                   R7006180
01A4  4530          L       MAR,LOC,NC      ADRS NEXT INSTR                    R7006190
01A5  8BC2          D       P2J             GO                                 R7006200
                    •                                                          R7006210
                    • EXCHANGE BYTE                                            R7006220
                    •                                                          R7006230
01A6  4EDF  EXHR    L       YD,YS,CS        DO CROSS SHIFT                     R7006240
01A7  8AC2          D       P2N             GO                                 R7006250
                    •                                                          R7006260
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                    *                                                          R7006280
                    * BYTE INPUT/OUTPUT AND CONTROL                            R7006290
                    *                                                          R7006300
                    *                                                          R7006310
                    * WRITE DATA                                               R7006320
01A8  4BE1  WDR     L     IO,YD,ADRS      DEVICE ADRESS                        R7006330
01A9  4BD2          L     IO,YS,DA        OUTPUT DATA                          R7006340
01AA  0BC2          D     P2J             GO                                   R7006350
                    *                                                          R7006360
01AB  4BE1  WD      L     IO,YD,ADRS      DEVICE ADDRESS                       R7006370
01AC  4BAE          L     IO,MDR,DA+CS    OUTPUT DATA                          R7006380
01AD  4533          L     MAR,LOC         ADRS NEXT INSTR                      R7006390
01AE  0BC2          D     P2J             GO                                   R7006400
                    *                                                          R7006410
                    * READ DATA                                               R7006420
01AF  4BE1  RDR     L     IO,YD,ADRS      DEVICE ADDRESS                       R7006430
01B0  4DB2          L     YS,IO,DR        INPUT DATA                           R7006440
01B1  0BC2          D     P2J             GO                                   R7006450
                    *                                                          R7006460
01B2  4BE1  RD      L     IO,YD,ADRS      DEVICE ADDRESS                       R7006470
01B3  4ABE          L     MDR,IO,DR+CS    INPUT DATA                           R7006480
01B4  1400          C     MW              STORE                                R7006490
01B5  4533          L     MAR,LOC         ADRS NEXT INSTR                      R7006500
01B6  0BC2          D     P2J             GO                                   R7006510
                    *                                                          R7006520
                    * ACKNOWLEDGE INTERRUPT/SENSE STATUS                       R7006530
01B7  4EB1  AIR     L     YD,IO,ACK       INPUT DEVICE ADRS                    R7006540
01B8  4BE1  SSR     L     IO,YD,ADRS      DEVICE ADDRESS                       R7006550
01B9  4DB3          L     YS,IO,STAT      INPUT STATUS                         R7006560
01BA  44D0          L     FLR,YS,NC       COPY TO FLR                          R7006570
01BB  0BC2          D     P2J             GO                                   R7006580
                    *                                                          R7006590
01BC  4EB1  AI      L     YD,IO,ACK       INPUT DEVICE ADRS                    R7006600
01BD  4BE1  SS      L     IO,YD,ADRS      DEVICE ADDRESS                       R7006610
01BE  4ABF          L     MDR,IO,STAT+CS  INPUT STATUS                         R7006620
01BF  1400          C     MW              STORE                                R7006630
01C0  44AC          L     FLR,MDR,CS+NC   COPY TO FLR                          R7006640
01C1  4530          L     MAR,LOC,NC      ADRS NEXT INSTR                      R7006650
01C2  0BC2          D     P2J             GO                                   R7006660
                    *                                                          R7006670
                    * OUTPUT COMMAND                                          R7006680
01C3  4BE1  OCR     L     IO,YD,ADRS      DEVICE ADDRESS                       R7006690
01C4  4B03          L     IO,YS,CMD       OUTPUT COMMAND                       R7006700
01C5  0BC2          D     P2J             GO                                   R7006710
                    *                                                          R7006720
01C6  4BE1  OC      L     IO,YD,ADRS      DEVICE ADDRESS                       R7006730
01C7  4BAF          L     IO,MDR,CMD+CS   OUTPUT COMMAND                       R7006740
01C8  4533          L     MAR,LOC         ADRS NEXT INSTR                      R7006750
01C9  0BC2          D     P2J             GO                                   R7006760
                    *                                                          R7006770
                    *                                                          R7006780
                    * AUTOLOAD                                                 R7006790
                    *                                                          R7006800
01CA  4653  AL      L     SRH,MAR         END ADRS                             R7006810
01CB  5578          L     MAR,'78'        BINDV SPECIFICATION                  R7006820
01CC  1800          C     MR                                                   R7006830
01CD  47AF          L     SRL,MDR,CS                                           R7006840
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01CE  4871        L   IO,SRL,ADRS   DEVICE ADDRESS                R7006850
01CF  48A3        L   IO,MDR,CMD    OUTPUT COMMAND                R7006860
01D0  5580        L   MAR,,80,      START ADRS TO MAR             R7006870
                  *                                               R7006880
01D1  4483  INAL  L   FLR,IO,STAT   STATUS CHECK                  R7006890
01D2  37E6        B   VGL,END       BAD STATUS                    R7006900
01D3  38D1        B   C,INAL        JUST BUSY                     R7006910
                  *                                               R7006920
01D4  4782        L   SRL,IO,DR     READ CHARACTER                R7006930
01D5  677F        O   SRL,SRL,NA                                  R7006940
01D6  3FD8        B   CVGL,INFST    NON-ZERO                      R7006950
01D7  51D1        L   RAL,L(INAL)   SKIP LEADER                   R7006960
                  *                                               R7006970
01D8  1800  INFST C   MR            FETCH HALFWORD                R7006980
01D9  4A7F        L   MDR,SRL,CS    INSERT DATA BYTE              R7006990
01DA  1400        C   MW            RESTORE                       R7007000
01DB  5801        L   AR,'1'                                      R7007010
01DC  C554        A   MAR,MAR,NC     BUMP ADDRESS                  R7007020
01DD  4853        L   AR,MAR                                      R7007030
01DE  E865        S   AR,SRH,CO      COMPARE TO FINAL              R7007040
01DF  38E5        B   C,EXIT        DONE                          R7007050
                  *                                               R7007060
01E0  4483  LOOPIN L  FLR,IO,STAT                                 R7007070
01E1  37E6        B   VGL,END       BAD STATUS                    R7007080
01E2  38E0        B   C,LOOPIN      JUST BUSY                     R7007090
01F3  4782        L   SRL,IO,DR                                   R7007100
01E4  51D8        L   RAL,L(INFST)  LOOP                          R7007110
                  *                                               R7007120
01F5  5400  EXIT  L   FLR,'0'       CLEAR FLAGS                   R7007130
01E6  4530  END   L   MAR,LOC,NC    ADRS NEXT INSTR               R7007140
01E7  88C2        D   P2J           GO                            R7007150
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                    *                                                          R7007170
                    * SHORT FORM IMMEDIATES                                    R7007180
                    *                                                          R7007190
                    * LOAD IMMEDIATE SHORT                                     R7007200
01E8  580F  LIS     L     AR,'F'          MASK TO AR                           R7007210
01E9  8E97          N     YD,IR           LOAD                                 R7007220
01EA  48C2          D     P2J             GO                                   R7007230
                    *                                                          R7007240
                    * LOAD COMPLEMENT SHORT                                    R7007250
01EB  4893  LCS     L     AR,IR                                                R7007260
01EC  980F          N     AR,'F'          VALUE TO AR                          R7007270
01ED  EE84          S     YD,NULL,NC      2'S COMP & LOAD                      R7007280
01EE  08C2          D     P2J             GO                                   R7007290
                    *                                                          R7007300
                    * ADD IMMEDIATE SHORT                                      R7007310
01EF  4893  AIS     L     AR,IR                                                R7007320
01F0  980F          N     AR,'F'          VALUE TO AR                          R7007330
01F1  CEE7          A     YD,YD           EXECUTE ADD                          R7007340
01F2  48C2          D     P2J             GO                                   R7007350
                    *                                                          R7007360
                    * SUBTRACT IMMEDIATE SHORT                                 R7007370
01F3  4893  SIS     L     AR,IR                                                R7007380
01F4  980F          N     AR,'F'          VALUE TO AR                          R7007390
01F5  EEE7          S     YD,YD           EXECUTE SUBTRACT                     R7007400
01F6  08C2          D     P2J                                                  R7007410
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                        ORG     '0200'                                  R7007430
                * WRITE BLOCK/READ BLOCK                                R7007440
                *                                                       R7007450
0200  1020      WBR     C       SUT             QUEUE WRITE             R7007460
0201  46D3      RBR     L       SRH,YS          START ADRS              R7007470
0202  5801              L       AR,'1'                                  R7007480
0203  C997              A       IR,IR                                   R7007490
0204  4AD3              L       MDR,YS          END ADRS                R7007500
0205  510B              L       RAL,L(COMBK)                            R7007510
                *                                                       R7007520
0206  1020      WB      C       SUT             QUEUE WRITE             R7007530
0207  46A3      RB      L       SRH,MDR         START ADRS              R7007540
0208  5802              L       AR,'2'                                  R7007550
0209  C557              A       MAR,MAR                                 R7007560
020A  1800              C       MR                                      R7007570
                *                                                       R7007580
020B  4563      COMBK   L       MAR,SRH         START ADRS TO MAR       R7007590
020C  4863              L       AR,SRH                                  R7007600
020D  E6A7              S       SRH,MDR         END MINUS START         R7007610
020E  3828              B       C,FINIS         END LESS THAN START     R7007620
020F  5801              L       AR,'1'                                  R7007630
0210  48E1              L       IO,YD,ADRS      ADDRESS DIVICE          R7007640
0211  2040              T       UT                                      R7007650
0212  3120              B       L,STATRB        READ BLOCK              R7007660
                * WRITE BLOCK                                           R7007670
0213  1800      LOOPW   C       MR                                      R7007680
0214  4483      STATWB  L       FLR,IO,STAT                             R7007690
0215  3F18              B       CVGL,TESTW                              R7007700
0216  48AE              L       IO,MDR,DA+CS                            R7007710
0217  E667              S       SRH,SRH         DECREMENT COUNT         R7007720
0218  3828              B       C,FINIS         DONE                    R7007730
0219  C554              A       MAR,MAR,NC      INCREMENT ADRS          R7007740
021A  5113              L       RAL,L(LOOPW)                            R7007750
                *                                                       R7007760
021B  3729      TESTW   B       VGL,FIN         BAD STATUS              R7007770
021C  5114              L       RAL,L(STATWB)   JUST BUSY               R7007780
                *                                                       R7007790
                * READ BLOCK                                            R7007800
021D  E667      LOOPR   S       SRH,SRH         DECREMENT COUNT         R7007810
021E  3828              B       C,FINIS         DONE                    R7007820
021F  C554              A       MAR,MAR,NC      INCREMENT ADRS          R7007830
0220  1800      STATRB  C       MR              FETCH HALFWORD          R7007840
0221  4483      STATR1  L       FLR,IO,STAT                             R7007850
0222  3F26              B       CVGL,TESTR                              R7007860
0223  4ABE              L       MDR,IO,DR+CS    INSERT BYTE             R7007870
0224  1400              C       MW              RESTORE HALFWORD        R7007880
0225  511D              L       RAL,L(LOOPR)                            R7007890
                *                                                       R7007900
0226  3729      TESTR   B       VGL,FIN         BAD STATUS              R7007910
0227  5121              L       RAL,L(STATR1)   JUST BUSY               R7007920
                *                                                       R7007930
                *                                                       R7007940
0228  5400      FINIS   L       FLR,'0'         CLEAR FLAGS             R7007950
0229  4530      FIN     L       MAR,LOC,NC      ADRS NEXT INSTR         R7007960
022A  CBC2              D       P2J             GO
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                    * MULTIPLY HALFWORD                                                  R7007980
                    *                                                                    R7007990
 0228  48A3  MH       L      AR,MDR          2ND OP TO AR                               R7008000
 022C  1008  MHR      C      SB                                                         R7008010
022D  5402           L      FLR,'2'                                                    R7008020
 022E  6287           O      MR2,NULL        MULTIPLIER TO MR2                          R7008030
 022F  323C           B      G,MH1           IS POSITIVE                                R7008040
                    * MULTIPLIER NEGATIVE                                              R7008050
 0230  E284           S      MR2,NULL,NC     2'S COMP                                   R7008060
 0231  67FF           O      SRL,YDP1,NA                                                R7008070
 0232  3240           B      G,MH2           MULTIPLICAND IS POSITIVE                   R7008080
 0233  4873           L      AR,SRL                                                     R7008090
 0234  E784           S      SRL,NULL,NC     2'S COMP                                   R7008100
                    * MULTIPLY, LIKE SIGNS                                             R7008110
 0235  5600  MH3      L      SRH,'0'         CLEAR HI PRODUCT                           R7008120
 0236  4823           L      AR,MR2                                                     R7008130
 0237  1303           C      MPY             DO MULTIPLY                                R7008140
 0238  4E67           L      YD,SRH,SR       LOAD HI PRODUCT                            R7008150
 0239  4F76           L      YDP1,SRL,SR,CI  LOAD LO PRODUCT                            R7008160
 023A  4533           L      MAR,LOC         ADRS NEXT INSTR                            R7008170
 023B  0AC2           D      P2N             GO                                         R7008180
                    *                                                                  R7008190
 023C  67FF  MH1      O      SRL,YDP1,NA                                                R7008200
 023D  3235           B      G,MH3           POSITIVE MULTIPLICAND                      R7008210
 023E  4873           L      AR,SRL                                                     R7008220
 023F  E784           S      SRL,NULL,NC     2'S COMP                                   R7008230
                    * MULTIPLY, UNLIKE SIGNS                                           R7008240
 0240  5600  MH2      L      SRH,'0'         CLEAR HI PRODUCT                           R7008250
 0241  4823           L      AR,MR2                                                     R7008260
 0242  1303           C      MPY             DO MULTIPLY                                R7008270
 0243  4E67           L      YD,SRH,SR       HI PRODUCT                                 R7008280
 0244  4876           L      AR,SRL,SR,CI                                               R7008290
 0245  EF85           S      YDP1,NULL,CO    2'S COMP PRODUCT                           R7008300
 0246  48E0           L      AR,YD,NC                                                   R7008310
 0247  EE86           S      YD,NULL,CI                                                 R7008320
 0248  4533           L      MAR,LOC         ADRS NEXT INSTR                            R7008330
 0249  0AC2           D      P2N             GO                                         R7008340
                    *                                                                  R7008350
                    * MULTIPLY HALFWORD UNSIGNED                                       R7008360
                    *                                                                  R7008370
 024A  48A3  MHU      L      AR,MDR          2ND OP TO AR                               R7008380
 024B  47F3  MHUR     L      SRL,YDP1        1ST OP TO SRL                              R7008390
 024C  5600           L      SRH,'0'         CLEAR HI PRODUCT                           R7008400
 024D  1303           C      MPY                                                        R7008410
 024E  4E67           L      YD,SRH,SR       LOAD HI PRODUCT                            R7008420
 024F  4F77           L      YDP1,SRL,SR     LOAD LO PRODUCT                            R7008430
 0250  4533           L      MAR,LOC         ADRS NEXT INSTR                            R7008440
 0251  0AC2           D      P2N             GO                                         R7008450
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                    • DIVIDE HALFWORD                                                   R7008470
                    •                                                                   R7008480
0252  48A3  DH      L     AR,MDR          DIVISOR TO AR                                 R7008490
0253  1928  DHR     C     SUT+SB                                                        R7008500
0254  6287          O     MR2,NULL        LOAD MR2,TEST SIGN                            R7008510
0255  3170          B     L,OKDIV         NEGATIVE DIVISOR                              R7008520
0256  325E          B     G,COMSOR        POSITIVE                                      R7008530
                    • DIVISOR IS ZERO                                                   R7008540
                    •                                                                   R7008550
                    • CHECK DIVIDE FAULT ENABLE                                         R7008560
0257  1004  OVDIV   C     CB                                                            R7008570
0258  5000          L     RAH,H(GENSWP)                                                 R7008580
0259  5548          L     MAR,L(ODPSW)                                                  R7008590
025A  4744          L     SRL,PSW,SR+NC                                                 R7008600
025B  447C          L     FLR,SRL,CS+NC   TEST PSW 03                                   R7008610
025C  3817          B     C,GENSWP        DO SWAP                                       R7008620
025D  5126          L     RAL,L(P3EXIT)                                                 R7008630
                    •                                                                   R7008640
                    •                                                                   R7008650
025E  E284  COMSOR  S     MR2,NULL,NC     2'S COMP DIVISOR                              R7008660
025F  1010          C     CUT                                                           R7008670
0260  47F3          L     SRL,YDP1        LOAD DIVIDEND                                 R7008680
0261  66EF          O     SRH,YD,NA       TEST SIGN                                     R7008690
0262  3277          B     G,DIVQP         QUOTIENT WILL BE PLUS                         R7008700
0263  4873          L     AR,SRL                                                        R7008710
0264  E785          S     SRL,NULL,CO     2'S COMP DIVIDEND                             R7008720
0265  4860          L     AR,SRH,NC                                                     R7008730
0266  E686          S     SRH,NULL,CI                                                   R7008740
0267  1030  DIVQM   C     TUT                                                           R7008750
0268  4823          L     AR,MR2                                                        R7008760
0269  C267          A     MR2,SRH         TRIAL SUBTRACT                                R7008770
026A  3857          B     C,OVDIV         OVERFLOW                                      R7008780
026B  1281          C     DIV             DO DIVIDE                                     R7008790
026C  4873          L     AR,SRL                                                        R7008800
026D  E784          S     SRL,NULL,NC     2'S COMP QUOTIENT                             R7008810
026E  317D          B     L,BCKDV         OK                                            R7008820
026F  3FE9          B     CVGL,FIX                                                      R7008830
                    •                                                                   R7008840
0270  47F3  OKDIV   L     SRL,YDP1        LOAD DIVIDEND                                 R7008850
0271  66EF          O     SRH,YD,NA       TEST SIGN                                     R7008860
0272  3267          B     G,DIVQM         QUOTIENT WILL BE MINUS                        R7008870
0273  4873          L     AR,SRL                                                        R7008880
0274  E785          S     SRL,NULL,CO     2'S COMP DIVIDEND                             R7008890
0275  4860          L     AR,SRH,NC                                                     R7008900
0276  E686          S     SRH,NULL,CI                                                   R7008910
0277  4823  DIVQP   L     AR,MR2                                                        R7008920
0278  C267          A     MR2,SRH         TRIAL SUBTRACT                                R7008930
0279  3857          B     C,OVDIV         OVERFLOW                                      R7008940
027A  1281          C     DIV             DO DIVIDE                                     R7008950
027B  677F          O     SRL,SRL,NA      TEST SIGN                                     R7008960
027C  3157          B     L,OVDIV         OVERFLOW                                      R7008970
                    •                                                                   R7008980
027D  2040  BCKDV   T     UT              MAKE REMAINDER SIGN                           R7008990
027E  3181          B     L,EXDIV         SAME AS DIVIDEND SIGN                         R7009000
027F  4863          L     AR,SRH                                                        R7009010
0280  E684          S     SRH,NULL,NC     2'S COMP                                      R7009020
0281  4E63  EXDIV   L     YD,SRH          LOAD REMAINDER                                R7009030
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0282  4F73      L     YDP1,SRL      LOAD QUOTIENT                    R7009040
0283  4533      L     MAR,LOC       ADRS NEXT INSTR                  R7009050
0284  AC2       D     P2N           GO                               R7009060
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                    •                                                                   R7009080
                    • SHORT BRANCHES                                                    R7009090
                    •                                                                   R7009100
                    • BRANCH ON FALSE CONDITION FORWARD OR REVERSE                      R7009110
0285  2002  BFFR    T     MSK                                                           R7009120
0286  3293          B     G,NRSB          NO BRANCH                                     R7009130
0287  5802  DOFRB   L     AR,'2'                                                        R7009140
0288  E337          S     LOC,LOC         POINT TO HERE                                 R7009150
0289  489B          L     AR,IR,SL                                                      R7009160
028A  981E          N     AR,'1E'         DISPLACEMENT TO AR                            R7009170
028B  449F          L     FLR,IR,CS       OP DOWN                                       R7009180
028C  318F          B     L,FRWD          FORWARD                                       R7009190
                    • BACKWARD                                                          R7009200
028D  E334          S     LOC,LOC,NC      DECREMENT LOC                                 R7009210
028E  0AC2          D     P2N             AND GO                                        R7009220
                    •                                                                   R7009230
028F  C334  FRWD    A     LOC,LOC,NC      INCREMENT LOC                                 R7009240
0290  0AC2          D     P2N             AND GO                                        R7009250
                    • BRANCH ON TRUE CONDITION FORWARD OR REVERSE                       R7009260
0291  2002  BTFR    T     MSK                                                           R7009270
0292  3287          B     G,DOFRB         DO BRANCH                                     R7009280
0293  0AC2  NRSB    D     P2N             NO BRANCH, G                                  R7009290
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                    *                                                       R7009310
                    * FLOATING-POINT INSTRUCTIONS                           R7009320
                    *                                                       R7009330
                    * FLOATING-POINT STORE                                  R7009340
0294  48C8  STE       L     AR,IR4,SL+NC                                    R7009350
0295  4653            L     SRH,MAR           SAVE STORE ADRS               R7009360
0296  951C            N     MAR,'1C'                                        R7009370
0297  1800            C     MR                FETCH HI 1ST OP               R7009380
0298  4853            L     AR,MAR                                          R7009390
0299  4563            L     MAR,SRH                                         R7009400
029A  1400            C     MW                STORE HI                      R7009410
029B  D502            A     MAR,'2'                                         R7009420
029C  1800            C     MR                FETCH LO 1ST OP               R7009430
029D  4863            L     AR,SRH                                          R7009440
029E  D502            A     MAR,'2'                                         R7009450
029F  1400            C     MW                STORE LO                      R7009460
02A0  4533            L     MAR,LOC           ADRS NEXT INSTR               R7009470
02A1  0AC2            D     P2N               GO                            R7009480
                    *                                                       R7009490
                    * FLOATING-POINT LOAD                                   R7009500
02A2  489B  LER       L     AR,IR,SL                                        R7009510
02A3  951C            N     MAR,'1C'          ADRS 2ND UP                   R7009520
02A4  1800            C     MR                                              R7009530
                    *                                                       R7009540
02A5  5003  LE        L     RAH,H(NRMAL)                                    R7009550
02A6  4894            L     AR,IR,SR+NC                                     R7009560
02A7  9970            N     IR,'70'           MASK YD FIELD                 R7009570
02A8  58FF            L     AR,'FF'                                         R7009580
02A9  86A7            N     SRH,MDR           HI 2ND OP                     R7009590
02AA  4863            L     AR,SRH                                          R7009600
02AB  A7A3            X     SRL,MDR,NF        EXPONENT & SIGN               R7009610
02AC  4879            L     AR,SRL,SL+CO      SIGN TO CARRY                 R7009620
02AD  499A            L     IR,IR,SL+CI       SIGN TO IR15                  R7009630
02AE  6993            O     IR,IR,NF          EXPONENT TO IR                R7009640
02AF  4853            L     AR,MAR                                          R7009650
02B0  D502            A     MAR,'2'                                         R7009660
02B1  1808            C     MR+SB                                           R7009670
02B2  67AF            O     SRL,MDR,NA        LOAD LO 2ND OP                R7009680
02B3  3344            B     GL,NRMAL          NORMALIZE                     R7009690
                    * OPERAND ZERO, CLEAR & TERMINATE                       R7009700
02B4  1004            C     CB                                              R7009710
02B5  51EC            L     RAL,L(ZRORST)                                   R7009720
                    *                                                       R7009730
                    *                                                       R7009740
02B6  1020  SER       C     SUT                                             R7009750
02B7  489B  COMFRR    L     AR,IR,SL                                        R7009760
02B8  951C            N     MAR,'1C'          ADRS 2ND OP                   R7009770
02B9  1830            C     MR+TUT                                          R7009780
                    *                                                       R7009790
02BA  1030  SE        C     TUT                                             R7009800
02BB  46A3  COMFRX    L     SRH,MDR           LOAD HI 2ND OP                R7009810
02BC  5003            L     RAH,H(BREAK)                                    R7009820
02BD  5802            L     AR,'2'                                          R7009830
02BE  C554            A     MAR,MAR,NC                                      R7009840
02BF  1808            C     MR+SR             FETCH LO 2ND OP               R7009850
02C0  48C8            L     AR,IR4,SL+NC                                    R7009860
02C1  47A3            L     SRL,MDR           SRH,SRL=2ND OP                R7009870
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02C2 951C        N    MAR,'1C'                                  R7009880
02C3 1800        C    MR              FETCH HI 1ST OP           R7009890
02C4 5802        L    AR,'2'                                    R7009900
02C5 49A3        L    MR0,MDR                                   R7009910
02C6 C554        A    MAR,MAR,NC                                R7009920
02C7 1800        C    MR              FETCH LO 1ST OP           R7009930
02C8 4863        L    AR,SRH                                    R7009940
02C9 41A3        L    MR1,MDR         MR0,MR1=1ST OP            R7009950
02CA A807        X    AR,MR0          COMPARE SIGNS             R7009960
02CB 3200        B    G,BREAK         SIGNS ALIKE               R7009970
02CC 1030        C    TUT             SIGNS DIFFER              R7009980
                 *                                              R7009990
02CD 449F        L    FLR,IR,CS       TEST OP                   R7010000
02CE 3454        B    V,MEDE          MULTIPLY OR DEIVDE        R7010010
02CF 3206        B    G,AESE          ADD OR SUBTRACT           R7010020
                 *                                              R7010030
                 * FLOATING-POINT COMPARE                       R7010040
02D0 1004        C    CB                                        R7010050
02D1 5802        L    RAH,H(COMP)                               R7010060
02D2 4809  COMP  L    AR,MR0,SL,CO    ASIGN TO CARRY            R7010070
02D3 2040        T    UT                                        R7010080
02D4 31D7        B    L,ALIKE         SIGNS ALIKE               R7010090
                 *                                              R7010100
                 * SIGNS DIFFER, SET GL AND EXIT                R7010110
02D5 680C        O    AR,MR0,NA,NC                              R7010120
02D6 51E7        L    RAL,L(CEXIT)                              R7010130
                 *                                              R7010140
                 * SIGNS ALIKE, SUBTRACT TO COMPARE MAGNITUDES  R7010150
02D7 38D9  ALIKE B    C,COMPEM        2'S COMP IF NEGATIVE      R7010160
02D8 3FE2        B    CVGL,COMPR                                R7010170
                 *                                              R7010180
                 *                                              R7010190
02D9 1008  COMPEM C   SB                                        R7010200
02DA 4813        L    AR,MR1          TWO'S COMPLEMENT          R7010210
02DB E185        S    MR1,NULL,CO     BOTH OPERANDS             R7010220
02DC 4800        L    AR,MR0,NC                                 R7010230
02DD E086        S    MR0,NULL,CI                               R7010240
02DE 4873        L    AR,SRL                                    R7010250
02DF E785        S    SRL,NULL,CO                               R7010260
02E0 4860        L    AR,SRH,NC                                 R7010270
02E1 E686        S    SRH,NULL,CI                               R7010280
                 *                                              R7010290
02E2 5400  COMPR  L   FLR,'0'                                   R7010300
02E3 4873        L    AR,SRL          LO 2ND OP                 R7010310
02E4 E815        S    AR,MR1,CO       FROM LO 1ST OP            R7010320
02E5 4860        L    AR,SRH,NC       HI 2ND OP                 R7010330
02E6 E807        S    AR,MR0          FROM HI 1ST OP            R7010340
02E7 4530  CEXIT  L   MAR,LOC,NC      ADRS NEXT INSTR           R7010350
02E8 68C2        O    P2,I            GO                        R7010360
                 *                                              R7010363
02E9 5400  FIX    L   FLR,'0'                                   R7010364
02EA 677F        O    SRL,SRL,NA      TEST QUOTIENT             R7010365
02EB 3257        B    G,OVDIV         OVERFLOW                  R7010366
02EC 307D        B    CTR,BCKDV       ZERO IS OK                R7010367
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                        ORG   '0300'                                    R7010370
                *                                                       R7010380
                *                                                       R7010390
0300  449F      BREAK   L     FLR,IR,CS                                 R7010400
0301  3454              B     V,MEDE          MULTIPLY OR DIVIDE        R7010410
0302  3206              B     G,AESE          ADD OR SUBTRACT           R7010420
0303  1004              C     CB                                        R7010430
0304  5002              L     RAH,H(COMP)                               R7010440
0305  5102              L     RAL,L(COMP)     COMPARE                   R7010450
                *                                                       R7010460
                *                                                       R7010470
                * FLOATING POINT ADD AND SUBTRACT                       R7010480
0306  4208      AESE    L     MR2,MR0,SL+NC   1ST OP SIGN OUT           R7010490
0307  4873              L     AR,SRL                                    R7010500
0308  E817              S     AR,MR1          1ST OP MINUS 2ND OP       R7010510
0309  4868              L     AR,SRH,SL+NC                              R7010520
030A  E827              S     AR,MR2                                    R7010530
030B  380E              B     C,BGTRA         B GREATER THAN A          R7010540
                * B EQUAL TO OR LESS THAN A                             R7010550
030C  3017              B     CTR,CONT                                  R7010560
030D  0000              DC    '0000'          FILLER                    R7010565
                *                                                       R7010570
030E  429F      BGTRA   L     MR2,IR,CS                                 R7010580
030F  4225              L     MR2,MR2,SR+CO                             R7010590
0310  4886              L     AR,NULL,SR+CI   0000 IF ADD,8000 IF SUB   R7010600
                * SWAP OPERANDS SO MR0,1 > SRH,SRL                       R7010610
0311  4213              L     MR2,MR1                                   R7010620
0312  4173              L     MR1,SRL                                   R7010630
0313  4723              L     SRL,MR2                                   R7010640
0314  4203              L     MR2,MR0                                   R7010650
0315  A063              X     MR0,SRH,NF                                R7010660
0316  4623              L     SRH,MR2                                   R7010670
                *                                                       R7010710
                *                                                       R7010720
0317  4897      CONT    L     AR,IR,SR                                  R7010730
0318  9A70              N     MDR,'70'        MASK YD FIELD             R7010740
0319  480F              L     AR,MR0,CS       HI EXPONENT               R7010750
031A  927F              N     MR2,'7F'        STRIP SIGN                R7010760
031B  4A2F              L     MDR,MR2,CS                                R7010770
031C  4809              L     AR,MR0,SL+CO    TO IR 0:6                 R7010780
031D  49AA              L     IR,MDR,SL+CI    RESULT SIGN TO IR15       R7010790
                *                                                       R7010800
031E  486F              L     AR,SRH,CS       LO EXPONENT               R7010810
031F  987F              N     AR,'7F'                                   R7010820
0320  5400              L     FLR,'0'                                   R7010830
0321  EA27              S     MDR,MR2         EXPONENT DIFFERENCE       R7010840
0322  58FF              L     AR,'FF'                                   R7010850
0323  8003              N     MR0,MR0,NF      REMOVE                    R7010860
0324  8663              N     SRH,SRH,NF      EXPONENTS                 R7010870
0325  322F              B     G,EQENT         EXPONENTS DIFFFR          R7010880
                * EXPONENTS ALIKE                                       R7010890
                *                                                       R7010900
0326  4873      EXFUNC  L     AR,SRL                                    R7010910
0327  2040              T     UT              CHECK OPERATOR            R7010920
0328  313E              B     L,EXADD         SUM REQUIRED              R7010930
                *                                                       R7010940
                * DIFFERENCE REQUIRED                                   R7010950
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                    *                                                          R7010960
0329 5401 EXSUB     L       FLR,'0'                                            R7010970
032A E717           S       SRL,MR1                                            R7010980
032B 4869           L       AR,SRH,NC                                          R7010990
032C E607           S       SRH,MR0                                            R7011000
032D 3249           B       G,NRMAL         RESULT NOT ZERO                    R7011010
032F 30EC           B       CTR,ZRORST                                         R7011020
                    *                                                          R7011030
                    *                                                          R7011040
032F 5805 EQENT     L       AR,16'                                             R7011050
0330 4CA3           L       CTR,MDR         EXPONENT DIFFERENCE                R7011060
0331 EAA7           S       MDR,MDR         TEST                               R7011070
0332 3136           B       L,EQULIZ        SOME SIGNIFICANCE                  R7011080
0333 5603           L       SRH,'0'         WOULD LOSE                         R7011090
0334 5703           L       SRL,'0'         SIGNIFICANCE                       R7011100
0335 5C26           L       CTR,'26'        SO SET TO ZERO                     R7011110
                    *                                                          R7011120
                    *                                                          R7011130
0336 1103 EQULIZ    C       SR1             SHIFT SMALLER NUMBER               R7011140
0337 1103           C       SR1             RIGHT                              R7011150
0338 1103           C       SR1                                                R7011160
0339 1103           C       SR1                                                R7011170
033A 3035           B       CTR,EQULIZ                                         R7011180
                    * EXPONENTS EQUALIZED                                      R7011190
033B 4873           L       AR,SRL                                             R7011200
033C 2040           T       UT              TEST OPERATOR                      R7011210
033D 3229           B       G,EXSUB         DIFFERENCE REQUIRES                R7011220
                    *                                                          R7011230
                    * SUM REQUIRED                                             R7011240
                    *                                                          R7011250
033E 5408 EXADD     L       FLR,'0'                                            R7011260
033F C717           A       SRL,MR1                                            R7011270
0340 4869           L       AR,SRH,NC                                          R7011280
0341 C607           A       SRH,MR0                                            R7011290
0342 329F           B       G,CRYTST        RESULT NOT ZERO                    R7011300
0343 30EC           B       CTR,ZRORST                                         R7011310
                    *                                                          R7011320
                    *                                                          R7011330
                    * NORMALIZE                                                R7011340
                    *                                                          R7011350
0344 5200 NRMAL     L       MR2,'0'         SET COUNT = 0                      R7011360
                    *                                                          R7011370
0345 58F0 NRLOOP    L       AR,'F0'                                            R7011380
0346 5400           L       FLR,'0'                                            R7011390
0347 8867           N       AR,SRH          TEST MS DIGIT                      R7011400
0348 3250           B       G,NRMFIN        DONE                               R7011410
0349 5802           L       AR,'2'                                             R7011420
034A C227           A       MR2,MR2         BUMP COUNT                         R7011430
034B 1080           C       SL1                                                R7011440
034C 1080           C       SL1                                                R7011450
034D 1080           C       SL1                                                R7011460
034E 1080           C       SL1                                                R7011470
034F 3F45           B       CVGL,NRLOOP                                        R7011480
                    *                                                          R7011490
0350 482F NRMFIN    L       AR,MR2,CS                                          R7011500
0351 E997           S       IR,IR           DECREMENT EXPONENT                 R7011510
0352 38EA           B       C,EXPUF         EXPONENT UNDERFLOW                 R7011520
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0353  3FD6          B     CVGL,FEND                                    R7011530
                    *                                                  R7011540
                    *                                                  R7011550
                    * FLOATING-POINT MULTIPLY & DIVIDE                 R7011560
                    *                                                  R7011570
0354  58FF  MEDE    L     AR,'FF'                                      R7011580
0355  5400          L     FLR,'0'                                      R7011590
0356  8267          N     MR2,SRH       CHECK 2ND OP                   R7011600
0357  335B          B     GL,CFOP                                      R7011610
                    * SECOND OP IS ZERO                                R7011620
0358  449F          L     FLR,IR,CS     TEST OP                        R7011630
0359  31E5          B     L,DFAULT      DIVIDE FAULT                   R7011640
035A  30FA          B     CTR,MDCLR     ZERO                           R7011650
                    *                                                  R7011660
                    *                                                  R7011670
035B  5400  CFOP    L     FLR,'0'                                      R7011680
035C  8207          N     MR2,MR0       CHECK 1ST OP                   R7011690
035D  335F          B     GL,EXPON      NOT ZERO                       R7011700
035E  30FA          B     CTR,MDCLR     ZERO                           R7011710
                    *                                                  R7011720
                    *                                                  R7011730
035F  4208  EXPON   L     MR2,MR0,SL,NC 2X EXPONENTS                   R7011740
0360  4A68          L     MDR,SRH,SL,NC                                R7011750
0361  8807          N     MR0,MR0       MASK OUT                       R7011760
0362  8667          N     SRH,SRH       EXPONENTS                      R7011770
0363  55FE          L     MAR,'FE'                                     R7011780
0364  485F          L     AR,MAR,CS     'FE00'                         R7011790
0365  8227          N     MR2,MR2       JUST EXPONENTS                 R7011800
0366  8AA7          N     MDR,MDR                                      R7011810
0367  4994          L     IR,IR,SR,NC                                  R7011820
0368  5408          L     FLR,'8'                                      R7011830
0369  2040          T     UT            MOVE SIGN FROM UT              R7011840
036A  326C          B     G,CTEST       TO IR15                        R7011850
036B  5400          L     FLR,'0'                                      R7011860
036C  499A  CTEST   L     IR,IR,SL,CI                                  R7011870
036D  449F          L     FLR,IR,CS     TEST OP                        R7011880
036E  4586          L     MAR,NULL,SR,CI '8000'                        R7011890
036F  4853          L     AR,MAR                                       R7011900
0370  A220          X     MR2,MR2,NF,NC CONVERT EXPONENTS              R7011910
0371  AAA0          X     MDR,MDR,NF,NC TO 2'S COMPLEMENT              R7011920
0372  4890          L     AR,IR,NC                                     R7011930
0373  99E1          N     IR,'E1'       STRIP OP CODE                  R7011940
0374  48A0          L     AR,MDR,NC     2ND OP EXPONENT                R7011950
0375  31A2          B     L,CFDIV       DO DIVIDE                      R7011960
                    *                                                  R7011970
                    * MULTIPLY, ADD EXPONENTS                          R7011980
                    *                                                  R7011990
0376  5400          L     FLR,'0'                                      R7012000
0377  C827          A     AR,MR2                                       R7012010
0378  34E9          B     V,WRONG       OVERFLOW OR UNDERFLOW          R7012020
                    *                                                  R7012030
0379  C854          A     AR,MAR,NC     BACK TO EXCESS 64              R7012040
037A  6997          O     IR,IR                                        R7012050
                    *                                                  R7012060
037B  4273          L     MR2,SRL                                      R7012070
037C  4763          L     SRL,SRH                                      R7012080
037D  5600          L     SRH,'0'                                      R7012090
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037E  400F          L     MR0,MR0,CS                                    R7012100
037F  481F          L     AR,MR1,CS                                     R7012110
0380  98FF          N     AR,='FF'                                      R7012120
0381  6007          O     MR0,MR0                                       R7012130
0382  411F          L     MR1,MR1,CS                                    R7012140
0383  A117          X     MR1,MR1                                       R7012150
0384  5C18          L     CTR,='18'       COUNT=24                      R7012160
                    *                                                   R7012170
                    *                                                   R7012180
0385  1103  MPYLP   C     SR1*CI*CO       SHIFT MULTIPLIER              R7012190
0386  4227          L     MR2,MR2,SR                                    R7012200
0387  388A          B     C,ONE           MULTIPLIER BIT SET            R7012210
0388  3085          B     CTR,MPYLP                                     R7012220
0389  3F8F          B     CVGL,MEND                                     R7012230
                    *                                                   R7012240
038A  4813  ONE     L     AR,MR1          ADD MULTIPLICAND              R7012250
038B  C775          A     SRL,SRL,CO      TO PRODUCT                    R7012260
038C  4800          L     AR,MR0,NC                                     R7012270
038D  C667          A     SRH,SRH                                       R7012280
038E  3085          B     CTR,MPYLP                                     R7012290
                    *                                                   R7012300
                    *                                                   R7012310
038F  1102  MEND    C     SR1*CI          FINAL SHIFT                   R7012320
0390  52F0          L     MR2,='F0'                                     R7012330
0391  482F          L     AR,MR2,CS                                     R7012340
0392  5400          L     FLR,='0'                                      R7012350
0393  5C08          L     CTR,='8'                                      R7012360
0394  8267          N     MR2,SRH         TEST IF NORMALIZED            R7012370
0395  339B          B     GL,FINAL        YES                           R7012380
0396  5202          L     MR2,='2'                                      R7012390
0397  482F          L     AR,MR2,CS                                     R7012400
0398  E997          S     IR,IR           DECREMENT EXPONENT            R7012410
0399  38EA          B     C,EXPUF         EXPONENT UNDERFLOW            R7012420
039A  5C04          L     CTR,='4'                                      R7012430
                    *                                                   R7012440
039B  1240  FINAL   C     RPT                                           R7012450
039C  1101          C     SR1*CO          FOUR OR EIGHT                 R7012460
039D  C77F  ROUND   A     SRL,SRL,NA      AND ROUND                     R7012470
039E  C66F          A     SRH,SRH,NA                                    R7012480
                    *                                                   R7012490
                    * TEST FOR CARRY                                   R7012500
                    *                                                   R7012510
039F  446F  CRYTST  L     FLR,SRH,CS                                    R7012520
03A0  3FCF          B     CVGL,RTSHFT     DID CARRY                     R7012530
03A1  30D6          B     CTR,FEND        NO CARRY, EXIT                R7012540
                    *                                                   R7012550
                    * FLOATING-POINT DIVIDE                            R7012560
                    *                                                   R7012570
03A2  5400  CFDIV   L     FLR,='0'                                      R7012580
03A3  E827          S     AR,MR2          SUBTRACT EXPONENTS            R7012590
03A4  34E9          B     V,WRONG                                       R7012600
                    *                                                   R7012610
03A5  C854          A     AR,HAR,NC       BACK TO EXCESS 64             R7012620
03A6  6997          O     IR,IR                                         R7012630
                    *                                                   R7012640
                    * RESULT EXPONENT ESTABLISHED, CONTINUE DIVIDE      R7012650
                    *                                                   R7012660
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03A7  4213          L     MR2,MR1                                    R7012670
03A8  4873          L     AR,SRL          TWO'S COMP                 R7012680
03A9  E185          S     MR1,NULL,CO     DIVISOR                    R7012690
03AA  4720          L     SRL,MR2,NC                                 R7012700
03AB  4200          L     MR2,MR0,NC                                 R7012710
03AC  4860          L     AR,SRH,NC                                  R7012720
03AD  E086          S     MR0,NULL,CI                                R7012730
03AE  4623          L     SRH,MR2                                    R7012740
                    *                                                R7012750
03AF  4873          L     AR,SRL                                     R7012760
03B0  CA15          A     MDR,MR1,CO                                 R7012770
03B1  4860          L     AR,SRH,NC                                  R7012780
03B2  C207          A     MR2,MR0                                    R7012790
03B3  38B5          B     C,ADJST                                    R7012800
03B4  3FBD          B     CVGL,FSTRT                                 R7012810
                    *                                                R7012820
                    *                                                R7012830
03B5  5202  ADJST    L     MR2,'2'                                    R7012840
03B6  482F          L     AR,MR2,CS                                  R7012850
03B7  C997          A     IR,IR           INCREMENT EXPONENT         R7012860
03B8  38F1          B     C,EXPOF         OVERFLOW                   R7012870
03B9  5C04          L     CTR,'4'         SHIFT DIVISOR LEFT         R7012880
03BA  4119  ADJLP    L     MR1,MR1,SL+CO   ONE HEX POSITION           R7012890
03BB  400A          L     MR0,MR0,SL+CI                              R7012900
03BC  30BA          B     CTR,ADJLP                                  R7012910
                    *                                                R7012920
                    *                                                R7012930
                    *                                                R7012940
03BD  5200  FSTRT    L     MR2,'0'         CLEAR                      R7012950
03BE  5A00          L     MDR,'0'         QUOTIENT                   R7012960
03BF  5C1A          L     CTR,'1A'        COUNT=26                   R7012970
                    *                                                R7012980
                    *                                                R7012990
03C0  4873  FDVLP    L     AR,SRL                                     R7013000
03C1  C515          A     MAR,MR1,CO                                 R7013010
03C2  4860          L     AR,SRH,NC                                  R7013020
03C3  C807          A     AR,MR0                                     R7013030
03C4  38C6          B     C,QUOT                                     R7013040
03C5  3FC8          B     CVGL,SHFT                                  R7013050
                    *                                                R7013060
03C6  6684  QUOT     O     SRH,NULL,NC                                R7013070
03C7  4750          L     SRL,MAR,NC                                 R7013080
                    *                                                R7013090
03C8  4AAB  SHFT     L     MDR,MDR,SL                                 R7013100
03C9  4228          L     MR2,MR2,SL                                 R7013110
03CA  1082          C     SL1+CI                                     R7013120
03CB  30C0          B     CTR,FDVLP                                  R7013130
                    *                                                R7013140
                    *                                                R7013150
03CC  4625          L     SRH,MR2,SR+CO                              R7013160
03CD  47A7          L     SRL,MDR,SR                                 R7013170
03CE  3F9D          B     CVGL,ROUND                                 R7013180
                    *                                                R7013190
                    *                                                R7013200
03CF  5C04  RTSHFT   L     CTR,'4'                                    R7013210
03D0  1240          C     RPT                                        R7013220
03D1  1100          C     SR1                                        R7013230
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                    *                                                       R7013240
03D2  5202          L     MR2,'2'                                           R7013250
03D3  482F          L     AR,MR2,CS                                         R7013260
03D4  C995          A     IR,IR,CO        INCREMENT EXPONENT                R7013270
03D5  38F1          B     C,EXPOF                                           R7013280
                    *                                                       R7013290
                    *                                                       R7013300
                    * COMMON FLOATING-POINT EXIT                           R7013310
                    *                                                       R7013320
03D6  1008  FEND    C     SB                                                R7013330
03D7  4895          L     AR,IR,SR*CO     SIGN TO CARRY                     R7013340
03D8  4896          L     AR,IR,SR*CI     SIGN & EXPONENT                   R7013350
03D9  52FF          L     MR2,'FF'                                          R7013360
03DA  422F          L     MR2,MR2,CS      'FF00'                            R7013370
03DB  8827          N     AR,MR2          MASK                              R7013380
03DC  6663          O     SRH,SRH,NF      INSERT OVER FRACTION              R7013390
03DD  48CB          L     AR,IR4,SL                                         R7013400
03DE   502          A     MAR,'2'                                           R7013410
03DF  4494          L     FLR,IR,SR*NC                                      R7013420
03E0  6A7F          O     MDR,SRL,NA                                        R7013430
03E1  1C00          C     PW              STORE LO RESULT                   R7013440
03E2  45C8          L     MAR,IR4,SL*NC                                     R7013450
03E3  6A6F          O     MDR,SRH,NA                                        R7013460
03E4  1C04          C     PW*CB           STORE HI RESULT                   R7013470
03E5  C102  DFAULT  D     JAN             FLR TO CC                         R7013480
03E6  34F7          B     V,FFAULT                                          R7013490
03E7  4530          L     MAR,LOC,NC      ADRS NEXT INSTR                   R7013500
03E8  4BC2          D     P2J             GO                                R7013510
                    *                                                       R7013520
                    *                                                       R7013530
03E9  31F1  WRONG   B     L,EXPOF         EXPONENT OVERFLOW                 R7013540
                    *                                                       R7013550
                    * EXPONENT UNDERFLOW                                    R7013560
03EA  5808  EXPUF   L     AR,'8'                                            R7013570
03EB  6997          O     IR,IR           SET V FLAG QUEUE                  R7013580
                    *                                                       R7013590
                    *                                                       R7013600
03EC  58EE  ZRORST  L     AR,'EE'                                           R7013610
03ED  8997  CCLR    N     IR,IR           RESET EXPONENT & SIGN             R7013620
03EE  4683          L     SRH,NULL        CLEAR HI                          R7013630
03EF  4783          L     SRL,NULL        AND LO RESULT                     R7013640
03F0  30D6          B     CTR,FEND                                          R7013650
                    *                                                       R7013660
                    * EXPONENT OVERFLOW                                     R7013670
                    *                                                       R7013680
03F1  56FF  EXPOF   L     SRH,'FF'        HIGH RESULT = 'FF'                R7013690
03F2  486F          L     AR,SRH,CS                                         R7013700
03F3  6767          O     SRL,SRH         LO RESULT = 'FFFF'                R7013710
03F4  7808          O     AR,'8'          EXPONENT = 'FF'                   R7013720
03F5  6997          O     IR,IR           SET V FLAG QUEUE                  R7013730
03F6  3FD6          B     CVGL,FEND                                         R7013740
                    *                                                       R7013750
                    *                                                       R7013760
03F7  0042  FFAULT  D     CLR                                               R7013770
03F8  5000          L     RAH,H(FLPEN8)   FLOATING-POINT                    R7013780
03F9  5153          L     RAL,L(FLPEN8)   ARITHMETIC FAULT                  R7013790
                    *                                                       R7013800
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03FA  58E0  MDCLR   L     AR,'E0'          CLEAR V FLAG QUEUE          07J13801
03FB  30FD          B     CIR,CCLR                                     J13802
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                    ORG   '0400'                                          R7013810
                    *                                                     R7013820
                    * HALFWORD I/O                                       R7013830
                    *                                                     R7013840
                    * WRITE HALFWORD                                     R7013850
0400  4AD3  WHR     L     MDR,YS          DATA                            R7013860
0401  4533  WH      L     MAR,LOC         ADRS NEXT INSTR                 R7013870
0402  4BE1          L     IO,YD,ADRS      ADDRESS DEVICE                  R7013880
0403  4BAE          L     IO,MDR,DA+CS    OUTPUT HI                       R7013890
0404  4BA2          L     IO,MDR,DA       OUTPUT LO                       R7013900
0405  08C2          D     P2J             GO                              R7013910
0406  08C2          D     P2J             GO                              R7013920
                    * READ HALFWORD                                       R7013930
0407  4BE1  RHR     L     IO,YD,ADRS      DEVICE ADDRESS                  R7013940
0408  4D8E          L     YS,IO,DR+CS     INPUT HI                        R7013950
0409  4882          L     AR,IO,DR        INPUT LO                        R7013960
040A  6DD3          O     YS,YS,NF        COMBINE                         R7013970
040B  08C2          D     P2J             GO                              R7013980
040C  0000          DC    '0000'          FILLER                          R7013990
040D  0000          DC    '0000'          FILLER                          R7014000
040E  4BE1  RH      L     IO,YD,ADRS      DEVICE ADDRESS                  R7014010
040F  5A00          L     MDR,'0'                                         R7014020
0410  4ABE          L     MDR,IO,DR+CS    INPUT HI                        R7014030
0411  4882          L     AR,IO,DR        INPUT LO                        R7014040
0412  6AA3          O     MDR,MDR,NF      COMBINE                         R7014050
0413  1400          C     MW              STORE                           R7014060
0414  4533          L     MAR,LOC         ADRS NEXT INSTR                 R7014070
0415  08C2          D     P2J             GO                              R7014080
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                    *                                                                   R7014100
                    * SHIFT RIGHT LOGICAL FULLWORD                                      R7014110
0416  46E3  SRL       L     SRH,YD            FETCH HI                                  R7014120
0417  47F3            L     SRL,YDP1          FETCH LO                                  R7014130
0418  4CA3            L     CTR,MDR           LOAD COUNTER                              R7014140
0419  1240            C     RPT                                                         R7014150
041A  1101            C     SR1+CO            DO SHIFT                                  R7014160
041B  6F7C            0     YDP1,SRL,NA+NC    LOAD LO                                   R7014170
041C  6E6C            0     YD,SRH,NA+NC      LOAD HI                                   R7014180
041D  8BC2            D     P2J               GO                                        R7014190
                    *                                                                   R7014200
                    * SHIFT LEFT LOGICAL FULLWORD                                       R7014210
041E  46E3  SLL       L     SRH,YD            FETCH HI                                  R7014220
041F  47F3            L     SRL,YDP1          FETCH LO                                  R7014230
0420  4CA3            L     CTR,MDR           LOAD COUNTER                              R7014240
0421  1240            C     RPT                                                         R7014250
0422  1081            C     SL1+CO            DO SHIFT                                  R7014260
0423  6F7C            0     YDP1,SRL,NA+NC    LOAD LO                                   R7014270
0424  6E6C            0     YD,SRH,NA+NC      LOAD HI                                   R7014280
0425  8BC2            D     P2J               GO                                        R7014290
                    *                                                                   R7014300
                    * SHIFT RIGHT FULLWORD ARITHMETIC                                   R7014310
0426  47F9  SRA       L     SRL,YDP1,SL+CO                                              R7014320
0427  46E8            L     SRH,YD,SL         LOAD HI                                   R7014330
0428  4CA0            L     CTR,MDR,NC                                                  R7014340
0429  1240            C     RPT                                                         R7014350
042A  1102            C     SR1+CI            DO SHIFT                                  R7014360
042B  1103            C     SR1+CI+CO         COMPENSATE PRESHIFT                       R7014370
042C  6F7C            0     YDP1,SRL,NA+NC    LOAD LO                                   R7014380
042D  6E6C            0     YD,SRH,NA+NC      LOAD HI                                   R7014390
042E  8BC2            D     P2J               GO                                        R7014400
                    *                                                                   R7014410
                    * SHIFT LEFT FULLWORD ARITHMETIC                                    R7014420
042F  47F9  SLA       L     SRL,YDP1,SL+CO    FETCH LO                                  R7014430
0430  46E8            L     SRH,YD,SL         FETCH HI: SIGN TO CARRY                   R7014440
0431  4CA0            L     CTR,MDR,NC        LOAD CTR                                  R7014450
0432  4887            L     AR,NULL,SR        SAVE SIGN                                 R7014460
0433  1240            C     RPT                                                         R7014470
0434  1081            C     SL1+CO            DO SHIFT                                  R7014480
0435  1100            C     SR1               COMPENSATE PRESHIFT                       R7014490
0436  6F7C            0     YDP1,SRL,NA+NC    LOAD LO                                   R7014500
0437  6E64            0     YD,SRH,NC         LOAD HI,INSRRT SIGN                       R7014510
0438  8BC2            D     P2J               GO                                        R7014520
                    *                                                                   R7014530
                    * ROTATE RIGHT LOGICAL FULLWORD                                     R7014540
0439  46E3  RRL       L     SRH,YD            FETCH HI                                  R7014550
043A  47F3            L     SRL,YDP1          FETCH LO                                  R7014560
043B  581F            L     AR,='1F'                                                    R7014570
043C  8CA7            N     CTR,MDR           LOAD & TEST CTR                           R7014580
043D  323F            B     G,RRL1                                                      R7014590
043E  5143            L     RAL,L(RRX)        CTR = 0                                   R7014600
043F  5400  RRL1      L     FLR,='0'                                                    R7014610
0440  4875  RRLL      L     AR,SRL,SR+CO      LSB TO CARRY                              R7014620
0441  1103            C     SR1+CI+CO         DO ROTATE                                 R7014630
0442  3040            B     CTR,RRLL                                                    R7014640
0443  6F7F  RRX       0     YDP1,SRL,NA       LOAD LO                                   R7014650
0444  6E6C            0     YD,SRH,NA+NC      LOAD HI                                   R7014660
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0445  ABC2          D     P2J          GO                              R7014670
                    *                                                  R7014680
                    * ROTATE LEFT LOGICAL FULLWORD                     R7014690
0446  46E3  RLL     L     SRH,YD       FETCH HI                        R7014700
0447  47F3          L     SRL,YDP1     FETCH LO                        R7014710
0448  581F          L     AR,='1F'                                     R7014720
0449  8CA7          N     CTR,MDR      LOAD & TEST CTR                 R7014730
044A  324C          B     G,RLL1                                       R7014740
044B  5150          L     RAL,L(RLX)   CTR = 0                         R7014750
044C  5400  RLL1    L     FLR,='0'                                     R7014760
044D  4869  RLLL    L     AR,SRH,SL,CO MSB TO CARRY                    R7014770
044E  1083          C     SL1,CI,CO    DO ROTATE                       R7014780
044F  304D          B     CTR,RLLL                                     R7014790
0450  6F7F  RLX     O     YDP1,SRL,NA  LOAD LO                         R7014800
0451  6E6C          O     YD,SRH,NA,NC LOAD HI                         R7014810
0452  ABC2          D     P2J          GO                              R7014820
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                    *                                                          R7014840
                    * REMOVE FROM TOP/BOTTOM OF LIST                           R7014850
                    *                                                          R7014860
0453  5701  RTBL    L     SRL,'1'                                              R7014870
0454  487F          L     AR,SRL,CS       '0100'                               R7014880
0455  46AF          L     SRH,MDR,CS      NO.USED/MAX.SLOT                     R7014890
0456  E667          S     SRH,SRH         DECREMENT NO.USED TALLY              R7014900
0457  3883          B     C,VFLAG         LIST EMPTY (UNDERFLOW)               R7014910
                    * LIST NOT EMPTY                                           R7014920
0458  466F          L     SRH,SRH,CS                                           R7014930
0459  4A63          L     MDR,SRH                                              R7014940
045A  1408          C     MW,SB           RESTORE                              R7014950
045B  487F          L     AR,SRL,CS                                            R7014960
045C  E667          S     SRH,SRH         DECREMENT MAX.SLOT                   R7014970
045D  5802          L     AR,'2'                                               R7014980
045E  C554          A     MAR,MAR,NC                                           R7014990
045F  C054          A     MR0,MAR,NC      ADRS OF SLOT 0                       R7015000
0460  1800          C     MR              CUR.TOP/NEXT BOTTOM                  R7015010
0461  489F          L     AR,IR,CS        OP-CODE DOWN                         R7015020
0462  9801          N     AR,'1'                                               R7015030
0463  6557          O     MAR,MAR         FORCE ODD IF RBL                     R7015040
0464  48AF          L     AR,MDR,CS       GET POINTER                          R7015050
0465  91FF          N     MR1,'FF'        CUR.TOP IF RTL                       R7015060
0466  4855          L     AR,MAR,SR+CO    NEXT BOTTOM IF RBL                   R7015070
0467  5801          L     AR,'1'                                               R7015080
0468  3873          B     C,RBL           REMOVE FROM BOTTOM                   R7015090
                    * REMOVE FROM TOP                                          R7015100
0469  C217          A     MR2,MR1         INCREMENT CURRENT TOP                R7015110
046A  486F          L     AR,SRH,CS                                            R7015120
046B  98FF          N     AR,'FF'                                              R7015130
046C  5400          L     FLR,'0'                                              R7015140
046D  A817          X     AR,MR1          COMPARE TO MAX                       R7015150
046E  3270          B     G,RTL                                                R7015160
                    * TABLE WRAP; SET CURRENT TOP TO ZERO                      R7015170
046F  5200          L     MR2,'0'                                              R7015180
0470  4818  RTL     L     AR,MR1,SL+NC    USE OLD VALUE                        R7015190
0471  1004          C     CB                                                   R7015200
0472  5179          L     RAL,L(REMOV)                                         R7015210
                    *                                                          R7015220
                    * REMOVE FROM BOTTOM                                       R7015230
0473  E215  RBL     S     MR2,MR1,CO      DECREMENT NEXT BOTTOM                R7015240
0474  3876          B     C,UNDER         WRAP                                 R7015250
0475  3F78          B     CVGL,RBL1       NO WRAP                              R7015260
                    *                                                          R7015270
0476  486F  UNDER   L     AR,SRH,CS                                            R7015280
0477  92FF          N     MR2,'FF'        SET TO MAX                           R7015290
0478  4828  RBL1    L     AR,MR2,SL+NC    USE NEW VALUE                        R7015300
                    *                                                          R7015310
0479  4A2F  REMOV   L     MDR,MR2,CS      RESTORE UPDATED                      R7015320
047A  1404          C     MW,CB           POINTER                              R7015330
047B  5400          L     FLR,'0'                                              R7015340
047C  C500          A     MAR,MR0,NF+NC   SLOT ADRS                            R7015350
047D  1800          C     MR              FETCH ELEMENT                        R7015360
047E  58FF          L     AR,'FF'                                              R7015370
047F  8867          N     AR,SRH          TEST NO.USED TALLY                   R7015380
0480  4EA3          L     YD,MDR          LOAD ELEMENT                         R7015390
0481  4533          L     MAR,LOC         ADRS NEXT INSTR                      R7015400
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0482  0BC2          D     P2J          GO                                  R7015410
                    *                                                      R7015420
0483  5404  VFLAG   L     FLR,'4'      SET OVERFLOW                        R7015430
0484  4533          L     MAR,LOC      ADRS NEXT INSTR                     R7015440
0485  0BC2          D     P2J          GO                                  R7015450
                    *                                                      R7015460
                    *                                                      R7015470
                    * SUPERVISOR CALL                                      R7015480
                    *                                                      R7015490
0486  5594  SVC     L     MAR,'94'                                         R7015500
0487  1C00          C     PW           STORE PARAMETER A+(X2)              R7015510
0488  5596          L     MAR,'96'                                         R7015520
0489  4A43          L     MDR,PSW                                          R7015530
048A  1C00          C     PW           STORE STATUS                        R7015540
048B  48C8          L     AR,IR4,SL+NC                                     R7015550
048C  5598          L     MAR,'98'                                         R7015560
048D  4A33          L     MDR,LOC                                          R7015570
048E  1C00          C     PW           STORE LOCCNT                        R7015580
048F  981E          N     AR,=1E=      2X R1 FIELD                         R7015590
0490  559A          L     MAR,'9A'                                         R7015600
0491  1800          C     MR                                               R7015610
0492  42A0          L     PSW,MDR,NC   NEW STATUS                          R7015620
0493  D59C          A     MAR,'9C'     2X R1 FIELD + '9C'                  R7015630
0494  0902          D     MR+JAM       FETCH NEW LOC,LOAD CC               R7015640
0495  43A3          L     LOC,MDR                                          R7015650
0496  0AC2          D     P2N          GO                                  R7015660
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                        ORG    '0500'                                          R7015695
                *                                                              R7015696
                * INTERRUPT SERVICE BLOCK PROCESSING                           R7017500
0500  1808  ISBSVC  C      MR*SB           FETCH FUNCTION WORD                 R7015710
0501  4054          L      MR0,MAR,SR*NC   ISB ADRS                            R7015720
0502  4008          L      MR0,MR0,SL*NC   FORCED EVEN                         R7015730
0503  466F          L      SRH,SRH,CS      DEVICE NUMBER                       R7015735
0504  49A3          L      IR,MDR                                              R7015740
0505  499F          L      IR,IR,CS                                            R7015750
0506  C504          A      MAR,MR0,NC                                          R7015760
0507  44C0          L      FLR,IR4,NC                                          R7015770
0508  3E39          B      CVG,NIO1        INIT*NOP*NULL*DMT                   R7015780
                *                                                              R7015790
                * READ OR WRITE                                               R7015800
0509  1808  SVC1    C      MR*SB           FETCH START ADRS                    R7015810
050A  C554          A      MAR,MAR,NC                                          R7015820
050B  486D          L      IO,SRH,ADRS*CS  ADDRESS THE DEVICE                  R7015830
050C  42A3          L      MR2,MDR         SAVE START ADRS                     R7015840
050D  48B3          L      AR,IO*STAT                                          R7015860
050E  6667          O      SRH,SRH         DEVNO/STATUS                        R7015870
050F  1800          C      MR              FETCH FINAL ADRS                    R7015880
0510  489F          L      AR,IR,CS        NO.BYTES/INTERRUPT                  R7015890
0511  9C0F          N      CTR,'0F'                                            R7015900
0512  449F          L      FLR,IR,CS                                           R7015910
0513  3F15          B      CVGL,SVC2                                           R7015920
0514  5C10          L      CTR,'10'        16 LIMIT                            R7015930
0515  4460  SVC2    L      FLR,SRH,NC      TEST STATUS                         R7015940
0516  3F52          B      CVGL,BSTAT      BAD STATUS                          R7015950
                * STATUS CLEAR                                                 R7015960
0517  41A3          L      MR1,MDR         FINAL ADDRESS                       R7015970
0518  4523          L      MAR,MR2         START ADDRESS                       R7015980
0519  5801          L      AR,'1'                                              R7015990
051A  44C3          L      FLR,IR4         TEST FUNCTION                       R7016000
051B  3133          B      L,WRITE                                             R7016010
                *                                                              R7016020
                *                                                              R7016030
051C  1800  READ    C      MR                                                  R7016040
051D  42B2          L      MR2,IO,DR       READ DATA                           R7016050
051E  4A2F          L      MDR,MR2,CS      INSERT BYTE                         R7016060
051F  1C00          C      PW              STORE IT                            R7016070
0520  C554          A      MAR,MAR,NC      INCREMENT ADRS                      R7016080
0521  301C          B      CTR,READ                                            R7016090
                *                                                              R7016100
                *                                                              R7016110
0522  4A53  END1    L      MDR,MAR         INCREMENTED START ADRS              R7016120
0523  5802          L      AR,'2'                                              R7016130
0524  C507          A      MAR,MR0                                             R7016140
0525  1C04          C      PW*CB           RESTORE                             R7016150
0526  48A3          L      AR,MDR                                              R7016160
0527  E817          S      AR,MR1          COMPARE START:FINAL                  R7016170
0528  386F          B      C,TERM1         DONE                                R7016180
                *                                                              R7016190
0529  4493          L      FLR,IR                                              R7016200
052A  3466          B      V,TCHAR                                             R7016210
                *                                                              R7016220
052B  2040  END3    T      UT              TEST QUEUE FLAG                     R7016230
052C  325F          B      G,FLAGS                                             R7016240
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                * NO USER INTERRUPT QUEUED                          R7016250
0520  042           D     CLR                                       R7016260
052E  5000          L     RAH,H(TEST4)                              R7016270
052F  5144          L     RAL,L(TEST4)                              R7016280
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                        ORG   '533'                                        R7016290
                    *                                                      R7016300
                    *                                                      R7016310
0533  1800  WRITE     C     MR                                             R7016320
0534  48AE            L     IO,MDR,DA+CS      OUTPUT BYTE                  R7016330
0535  42AF            L     MR2,MDR,CS                                     R7016340
0536  C554            A     MAR,MAR,NC        INCREMENT ADRS               R7016350
0537  3033            B     CTR,WRITE                                      R7016360
0538  3F22            B     CVGL,END1                                      R7016370
                    *                                                      R7016380
                    *                                                      R7016390
0539  1004  NIO1      C     CB                                             R7016400
053A  3428            B     V,END3            NOP                          R7016410
053B  3845            B     C,NIO2            INIT                         R7016420
                    *                                                      R7016430
053C  499F  NIO3      L     IR,IR,CS                                       R7016440
053D  3175            B     L,TERM2           NULL                         R7016450
                    *                                                      R7016460
                    * DECREMENT MEMORY & TEST                              R7016470
053E  1808            C     MR+SB             FETCH COUNT                  R7016480
053F  5400            L     FLR,'0'                                        R7016490
0540  5801            L     AR,'1'                                         R7016500
0541  EAA7            S     MDR,MDR           DECREMENT                    R7016510
0542  1C04            C     PW+CB             RESTORE                      R7016520
0543  332B            B     GL,END3           NOT ZERO                     R7016530
                    * COUNT IS ZERO                                        R7016540
0544  5175            L     RAL,L(TERM2)                                   R7016550
                    *                                                      R7016560
                    *                                                      R7016570
0545  499F  NIO2      L     IR,IR,CS                                       R7016580
0546  4998            L     IR,IR,SL+NC       RESET INIT                   R7016590
0547  4994            L     IR,IR,SR+NC                                    R7016600
0548  4503            L     MAR,MR0                                        R7016610
0549  4A93            L     MDR,IR                                         R7016620
054A  1C00            C     PW                RESTORE                      R7016630
054B  44C0            L     FLR,IR4,NC        TEST FUNCTION BIT 0          R7016640
054C  3859            B     C,OC1             OUTPUT COMMAND               R7016650
054D  499F            L     IR,IR,CS                                       R7016660
054E  C554            A     MAR,MAR,NC                                     R7016670
054F  44C3            L     FLR,IR4           TEST FUNCTION BIT 2          R7016680
0550  323C            B     G,NIO3            DMT OR NULL                  R7016690
0551  3009            B     CTR,SVC1                                       R7016700
                    *                                                      R7016710
                    *                                                      R7016720
0552  58C3  BSTAT     L     AR,'C3'           SET INIT,NOP,QUEUE           R7016730
0553  6897            O     AR,IR                                          R7016740
0554  B901            X     IR,'1'            CLEAR HI/LO                  R7016750
0555  489F            L     AR,IR,CS                                       R7016760
0556  7830            O     AR,'30'                                        R7016770
0557  B930            X     IR,'30'           RESET CHAIN & DOIT           R7016780
0558  3F72            B     CVGL,TERM4                                     R7016790
                    *                                                      R7016800
                    *                                                      R7016810
0559  5806  OC1       L     AR,'6'                                         R7016820
055A  C504            A     MAR,MR0,NC                                     R7016830
055B  1804            C     MR+CB             FETCH COMMAND BYTE           R7016840
055C  486D            L     IO,SRH,ADRS+CS    ADDRESS THE DEVICE           R7016850
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055D  48AF          L     IO,MDR,CMD+CS   OUTPUT COMMAND                  R7016860
055E  512B          L     RAL,L(END3)                                     R7016870
                    *                                                     R7016880
                    *                                                     R7016890
055F  444F  FLAGS   L     FLR,PSW,CS      TEST PSW08                      R7016900
0560  5000          L     RAH,H(GENSWP)                                   R7016910
0561  5582          L     MAR,'82'                                        R7016920
0562  3217          B     G,GENSWP                                        R7016930
0563  2408          T     ATN+DC                                          R7016940
0564  3210          B     G,P3HELP                                        R7016950
0565  5124          L     RAL,L(TEST2)                                    R7016960
                    *                                                     R7016970
                    *                                                     R7016980
0566  5806  TCHAR   L     AR,'6'                                          R7016990
0567  C504          A     MAR,MR0,NC                                      R7017000
0568  1804          C     MR+CB                                           R7017010
0569  58FF          L     AR,'FF'                                         R7017020
056A  8727          N     SRL,MR2         LAST CHAR TRANSFERED            R7017030
056B  88A7          N     AR,MDR          TERMINAL CHARACTER              R7017040
056C  5400          L     FLR,'0'                                         R7017050
056D  A877          X     AR,SRL          COMPARE                         R7017060
056E  322B          B     G,END3          NO MATCH                        R7017070
                    *                                                     R7017080
056F  4893  TERM1   L     AR,IR                                           R7017090
0570  7940          O     IR,'40'         SET NOP                         R7017100
0571  499F          L     IR,IR,CS                                        R7017110
                    *                                                     R7017120
0572  4A93  TERM4   L     MDR,IR          MODIFIED FUNCTION               R7017130
0573  4503          L     MAR,MR0                                         R7017140
0574  1C00          C     PW              RESTORE                         R7017150
0575  5802  TERM2   L     AR,'2'                                          R7017160
0576  E507          S     MAR,MR0                                         R7017170
0577  4A63          L     MDR,SRH                                         R7017180
0578  1C04          C     PW+CB           STORE DEVNO/STATUS              R7017190
                    *                                                     R7017200
0579  449F          L     FLR,IR,CS       TEST FUNCTION BIT 6             R7017210
057A  328C          B     G,QUEUE                                         R7017220
                    *                                                     R7017230
057B  44C3  TERM3   L     FLR,IR4         TEST FUNCTION BIT 10            R7017240
057C  327E          B     G,CHAIN                                         R7017250
057D  512B          L     RAL,L(END3)                                     R7017260
                    *                                                     R7017270
                    *                                                     R7017280
057F  5804  CHAIN   L     AR,'4'                                          R7017290
057F  E500          S     MAR,MR0,NF+NC                                   R7017300
0580  1804          C     MR+CB           FETCH CHAIN VALUE               R7017310
0581  5000          L     RAH,H(DOIT)                                     R7017320
0582  486F          L     AR,SRH,CS                                       R7017330
0583  96FF          N     SRH,'FF'        DEVICE NR                       R7017360
0584  4868          L     AR,SRH,SL+NC                                    R7017370
0585  D5D0          A     MAR,L(SPTABL)   ADRS SERVICE POINTER            R7017380
0586  1C00          C     PW              STORE NEW POINTER               R7017390
0587  312C          B     L,DOIT          GO ON IF FUNCTION 11 SET        R7017400
0588  5005          L     RAH,H(END3)                                     R7017410
0589  512B          L     RAL,L(END3)                                     R7017420
058A  0000          DC    '0000'          FILLER                          R7017424
058B  0000          DC    '0000'          FILLER                          R7017429
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                *                                                                R7017430
                *                                                                R7017440
058C  5580  QUEUE   L     MAR,'80'                                                R7017450
058D  1804          C     MR*CB           ADRS OF QUEUE                           R7017460
058E  4743          L     SRL,PSW         SAVE PSW                                R7017470
058F  5200          L     PSW,'0'         FORCE SUPERVISOR MODE                   R7017480
0590  45A3          L     MAR,MDR                                                 R7017490
0591  1820          C     MR*SUT          SET QUEUE FLAG                          R7017500
                                                                                  R7017515
                *                                                                R7017520
                *                                                                R7017530
                * ADD TO TOP/BOTTOM OF LIST                                       R7017540
                *                                                                R7017550
0592  48A3  ATBL    L     AR,MDR          MAX.SLOT/NO.USED                        R7017560
0593  46AF          L     SRH,MDR,CS      NO.USED/MAX.SLOT                        R7017570
0594  E867          S     AR,SRH          COMPARE                                 R7017580
0595  389A          B     C,ADDTO                                                 R7017590
                * OVERFLOW IF NO.USED EQUAL OR GREATER                           R7017600
0596  2040          T     UT              UT SET IF CHANNEL IO                    R7017610
0597  32C8          B     G,LISTOV        QUEUE OVERFLOW INTERRUPT                R7017620
                *                                                                R7017630
0598  5404          L     FLR,'4'         SET OVERFLOW                            R7017640
0599  51BD          L     RAL,L(COMEX)                                            R7017650
                *                                                                R7017660
                *                                                                R7017670
059A  CAAE  ADDTO   A     MDR,MDR,NA*CI   INCREMENT NO.USED TALLY                 R7017680
0598  1408          C     MW*SB           RESTORE                                 R7017690
                *                                                                R7017700
059C  5802          L     AR,'2'                                                  R7017710
059D  C554          A     MAR,MAR,NC                                              R7017720
059E  1800          C     MR              CUR,TOP/NEXT BOTTOM                     R7017730
059F  489F          L     AR,IR,CS        OP-CODE DOWN                            R7017740
05A0  9801          N     AR,'1'                                                  R7017750
05A1  6557          O     MAR,MAR         FORCE ODD IF ABL                        R7017760
05A2  48AF          L     AR,MDR,CS       GET POINTER                             R7017770
05A3  91FF          N     MR1,'FF'        CUR.TOP IF ATL                          R7017780
05A4  4855          L     AR,MAR,SR*CO    NEXT BOTTOM IF ABL                      R7017790
05A5  5801          L     AR,'1'                                                  R7017800
05A6  38BF          B     C,BOTTOM        ADD TO BOTTOM                           R7017810
                * ADD TO TOP                                                     R7017820
05A7  E215          S     MR2,MR1,CO      DECREMENT CUR.TOP                       R7017830
05A8  38AA          B     C,ATL1          WRAP                                    R7017840
05A9  3FAC          B     CVGL,ATL                                                R7017850
                * LIST WRAP; SET CURRENT TOP TO MAX                              R7017860
05AA  E86E  ATL1    S     AR,SRH,NA*CI    MAX SLOT NUMBER                         R7017870
05AB  92FF          N     MR2,'FF'                                                R7017880
05AC  4828  ATL     L     AR,MR2,SL*NC    USE NEW VALUE                           R7017890
                *                                                                R7017900
05AD  4A2F  ADDIT   L     MDR,MR2,CS      INSERT UPDATED                          R7017910
05AE  1404          C     MW*CB           POINTER & RESTORE                       R7017920
05AF  C854          A     AR,MAR,NC                                               R7017930
05B0  D502          A     MAR,'2'         SLOT ADRS                               R7017940
05B1  2040          T     UT              UT SET IF CHANNEL IO                    R7017950
05B2  31B8          B     L,ALIST         NOT SET IF ATL OR ABL                   R7017960
05B3  4A03          L     MDR,MR0         GET ELEMENT                             R7017970
05B4  1C00          C     PW              STORE IT                                R7017975
05B5  5802          L     AR,'2'                                                  R7017974
05B6  E507          S     MAR,MR0                                                 R7017975
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05B7  1800          C     MR              FETCH DEVNO/STATUS                R7017970
05B8  4273          L     PSW,SRL         RESTORE PSW                       R7017980
05B9  46A3          L     SRH,MDR                                           R7017981
05BA  517B          L     RAL,L(TERM3)    RETURN                            R7017990
                    *                                                       R7018000
                    *                                                       R7018010
05BB  4AE3  ALIST   L     MDR,YD          GET ELEMENT                       R7018020
05BC  C442          D     MW,CLR          STORE IT                          R7018030
                    *                                                       R7018040
05BD  4533  COMEX   L     MAR,LOC         ADRS NEXT INSTR                   R7018050
05BE  98C2          D     P2J             GO                                R7018060
                    *                                                       R7018070
                    * ADD TO BOTTOM                                         R7018080
05BF  C214  BOTTOM  A     MR2,MR1,NC      INCREMENT NEXT BOTTOM             R7018090
05C0  E864          S     AR,SRH,NC       MAX SLOT NUMBER                   R7018100
05C1  98FF          N     AR,=FF          .                                 R7018110
05C2  5400          L     FLR,'0'                                           R7018120
05C3  A817          X     AR,MR1          COMPARE TO MAX.                   R7018130
05C4  32C6          B     G,ABL                                             R7018140
                    * LIST WRAP; SET NEXT BOTTOM TO ZERO                    R7018150
05C5  >200          L     MR2,'0'                                           R7018160
05C6  4818  ABL     L     AR,MR1,SL,NC    USE OLD VALUE                     R7018170
05C7  30AD          B     CTR,ADDIT                                         R7018180
                    *                                                       R7018190
                    *                                                       R7018200
05C8  >58A  LISTOV  L     MAR,'8A'                                          R7018210
05C9  4A03          L     MDR,MR0                                           R7018220
05CA  C42           D     PW,CLR          SAVE ABORTED ELEMENT              R7018230
05CB  4273          L     PSW,SRL         RESTORE PSW                       R7018240
05CC  558C          L     MAR,'8C'                                          R7018250
05CD  5000          L     RAH,H(GENSWP)                                     R7018260
05CE  5117          L     RAL,L(GENSWP)                                     R7018270
                    *                                                       R7018
05CF                END                                                   R7018
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```
ABL     05C6
* ABORT  000A
* ACH    015D
* ACHR   015A
  ADDIT  05AD
  ADDTO  059A
  ADJLP  03BA
  ADJST  0385
  AESE   0306
* AH     015E
* AHM    016A
* AHR    015B
* AI     018C
* AIR    0187
* AIS    01EF
* AL     01CA
  ALIKE  02D7
  ALIST  05BB
* AMODRS 0002
* AMODRX 0006
* ATBL   0592
  ATL    05AC
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	ATL1	05AA
•	BAL	0109
•	BALR	0108
	BCKDV	027D
•	BFC	0118
•	BFCR	0114
•	BFFR	0285
	BGTRA	030E
	BOTTOM	058F
	BRANCH	012C
	BREAK	0300
	BSTAT	0552
•	BTC	0110
•	BTCR	010C
•	BTFR	0291
•	BXLH	011C
	CCLR	03ED
	CEXIT	02E7
	CFDIV	03A2
	CFOP	035B
•	CH	014F
	CHAIN	057E
•	CHR	0150
•	CLB	019F
•	CLH	013A
•	CLHR	0138
	CLRWIT	0078
	COMBK	020B
	COMEX	058D
•	COMFRR	02B7
•	COMFRX	02BB
	COMP	02D2
	COMPEM	02D9
	COMPR	02E2
	COMSOR	025E
	CONSER	006B
	CONT	0317
	CRYTST	039F
	CTEST	036C
	DCR	00E1
	DCREAD	00E8
•	DCWRIT	00E4
	DFAULT	03E5
•	DH	0252
•	DHR	0253
	DIFFER	0156
	DISMEM	0084
	DISPLY	005F
	DIVQM	0267
	DIVQP	0277
	DOFRB	0287
	DOIT	002C
	END	01E6
	END1	0522
	END3	052B
	ENTHLP	003A
•	EPSR	00DD

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	EOENT	032F
	EQULIZ	0336
	EXADD	033E
*	EXBR	01A6
	EXDIV	0281
*	EXFUNC	0326
	EXIT	01E5
	EXPOF	03F1
	EXPON	035F
	EXPUF	03EA
	EXSUB	0329
	FDVLP	03C0
	FEND	03D6
	FFAULT	03F7
	FIN	0229
	FINAL	039B
	FINIS	0228
	FIX	02E9
	FLAGS	055F
	FLPENB	0053
	FRWD	028F
	FSTRT	038D
	GENSWP	0017
	HELP	003B
	HSSVC	0028
	IDLE	0063
	IDLE1	0064
	ILEG1	0104
*	ILLEG	0100
	INAL	01D1
	INFST	01DB
*	INITAL	0000
	INSDIS	0096
	INTENT	0086
	IOSVC	0029
	ISBSVC	0500
*	LB	019B
*	LBR	0199
*	LCS	01EB
*	LE	02A5
*	LER	02A2
*	LH	014C
*	LHR	014A
*	LIS	01E8
	LISTOV	05C8
*	LM	00C0
	LMLOOP	00C5
	LOC	0026
	LOOPIN	01E0
	LOOPR	021D
	LOOPW	0213
	LPST	001F
*	LPSW	00DA
	MDCLR	03FA
	MEDE	0354
	MEND	038F
*	MH	022B

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	MH1	023C
	MH2	0240
	MH3	0235
•	MHR	022C
•	MHU	024A
•	MHUR	0248
	MMFSWP	00F0
	MPYLP	0385
	MREAD	007C
	MWSL	007F
•	NH	0134
•	NHR	0132
	NIO1	0539
	NIO2	0545
	NIO3	053C
•	NMODRX	0004
	NOBRAN	0129
	NRLOOP	0345
	NRMAL	0344
	NRMFIN	0350
	NRRB	010F
	NRSB	0293
	NRUN	00D7
	NRXB	0130
•	OC	01C6
	OC1	0559
•	OCR	01C3
	ODPSW	0048
	OFPSW	0028
•	OH	0140
•	OHR	013E
	OIPSW	0040
	OKDIV	0270
	OMPSW	0038
	ONE	038A
	OTPSW	0030
	OUTDIS	008B
	OVDIV	0257
	P3EXIT	0026
	P3HELP	0010
	PNTR	0022
	PSW	0024
	PSWDIS	0089
	PWRDWN	009E
	QUEUE	058C
	QUOT	03C6
•	RB	0207
	RBL	0473
	RBL1	0478
•	RBR	0201
•	RD	01B2
•	RDR	01AF
	READ	051C
	REGDIS	0090
	REMOV	0479
•	RH	040E
•	RHR	0407

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*	RLL	0446
	RLL1	044C
	RLLL	044D
	RLX	0450
	ROUND	039D
*	RRL	0439
	RRL1	043F
	RRLL	0440
	RRX	0443
*	RTBL	0453
	RTL	0470
	RTSHFT	03CF
*	SCH	0165
*	SCHR	0162
*	SE	028A
*	SER	0286
*	SH	0166
	SHFT	03C8
*	SHR	0163
*	SINT	0057
*	SIS	01F3
	SL	0087
*	SLA	042F
*	SLHA	0186
*	SLHL	0178
*	SLL	041E
	SPTABL	00D0
*	SRA	0426
*	SRHA	017E
*	SRHL	0172
*	SRL	0416
*	SS	01BD
*	SSR	01B8
	STATR1	0221
	STATR8	0220
	STATW8	0214
*	STR	0195
*	STBR	018F
*	STE	0294
*	STH	012E
*	STM	00A9
	STMLP	00AE
*	SVC	0486
	SVC1	0509
	SVC2	0515
	TCHAR	0566
	TERM1	056F
	TERM2	0575
	TERM3	0578
	TERM4	0572
	TEST	0014
	TEST1	0022
	TEST2	0024
	TEST3	0042
	TEST4	0044
	TESTR	0226
	TESTW	021B

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*	THI	016F
	UNDFR	0476
	USRFHI	0049
	VFLAG	0483
	WAIT	005A
	WAIT1	0058
*	WB	0206
*	WBR	0200
*	WD	01AB
*	WDR	01A8
*	WH	0401
*	WHR	0400
	WRITE	0533
	WRONG	03E9
*	XH	0146
*	XHR	0144
	XLE	012A
	ZRORST	03EC

MEMORY

8KB (SERIES 5) MEMORY MAINTENANCE SPECIFICATION

1. INTRODUCTION

This specification applies to the INTERDATA 8KB (Series 5) Memories listed in Table 1.

TABLE 1. SERIES 5 MEMORIES

INTERDATA PART NUMBER	PRODUCT NUMBERS	SPEED	SIZE	CONFIGURATION
02-211F01M01	M70/71-301	1.0 us	4KB	4K X 17*
02-211F02M01	M70/71-300	1.0 us	4KB	4K X 16

*The seventeenth bit is a parity bit.

2. SCOPE

This specification describes the operation of the 8KB Memory. It does not include Processor to Memory Interface information, except the inputs necessary to operate the Memory and the resultant outputs provided by the Memory. A brief review of core memory theory precedes the detailed circuit description. This specification also provides a block diagram analysis, timing information, troubleshooting and maintenance information, and a mnemonics list.

3. PHYSICAL DESCRIPTION

The 8KB Memory consists of a one mother-board (approximately 15" x 15") that can be installed in a card file on 0.75 inch centers. Figure 1 shows the physical location on the mother-board of the major circuit blocks comprising the Series 5 Memory. A back panel Map is shown in Functional Schematic 02-211D08, Sheet 6.

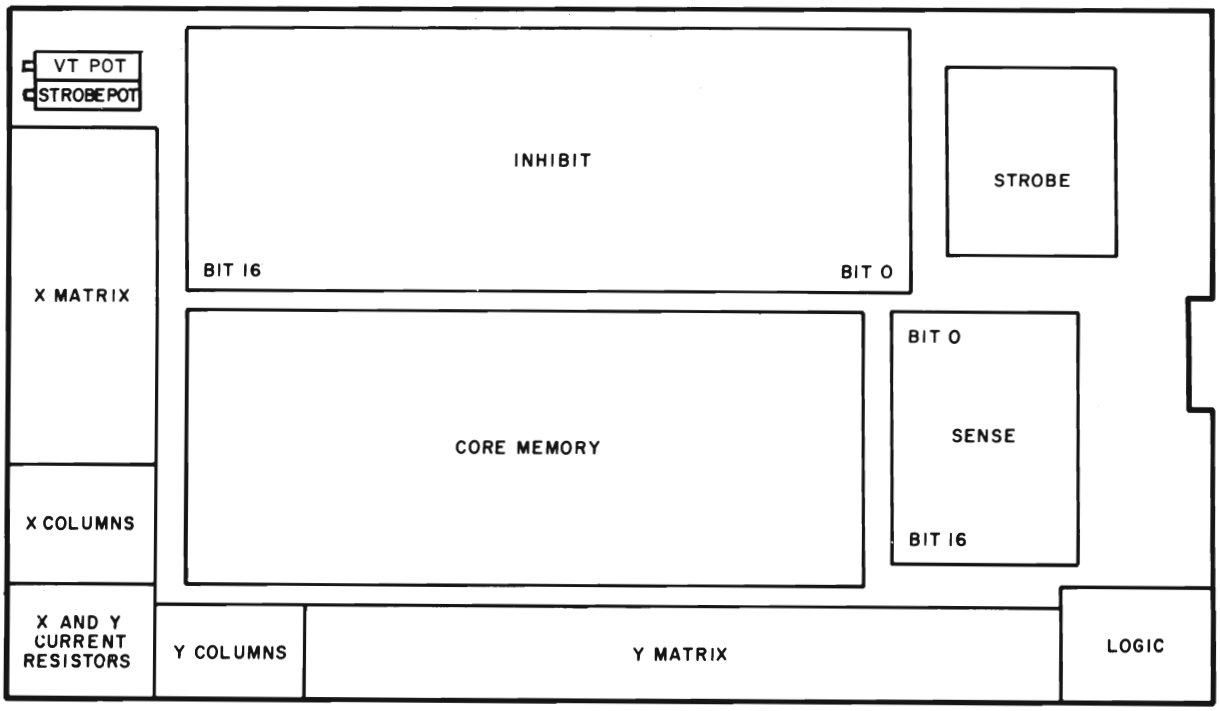


Figure 1. 8KB (Series 5) Memory Basic Layout of Major Circuit Sections

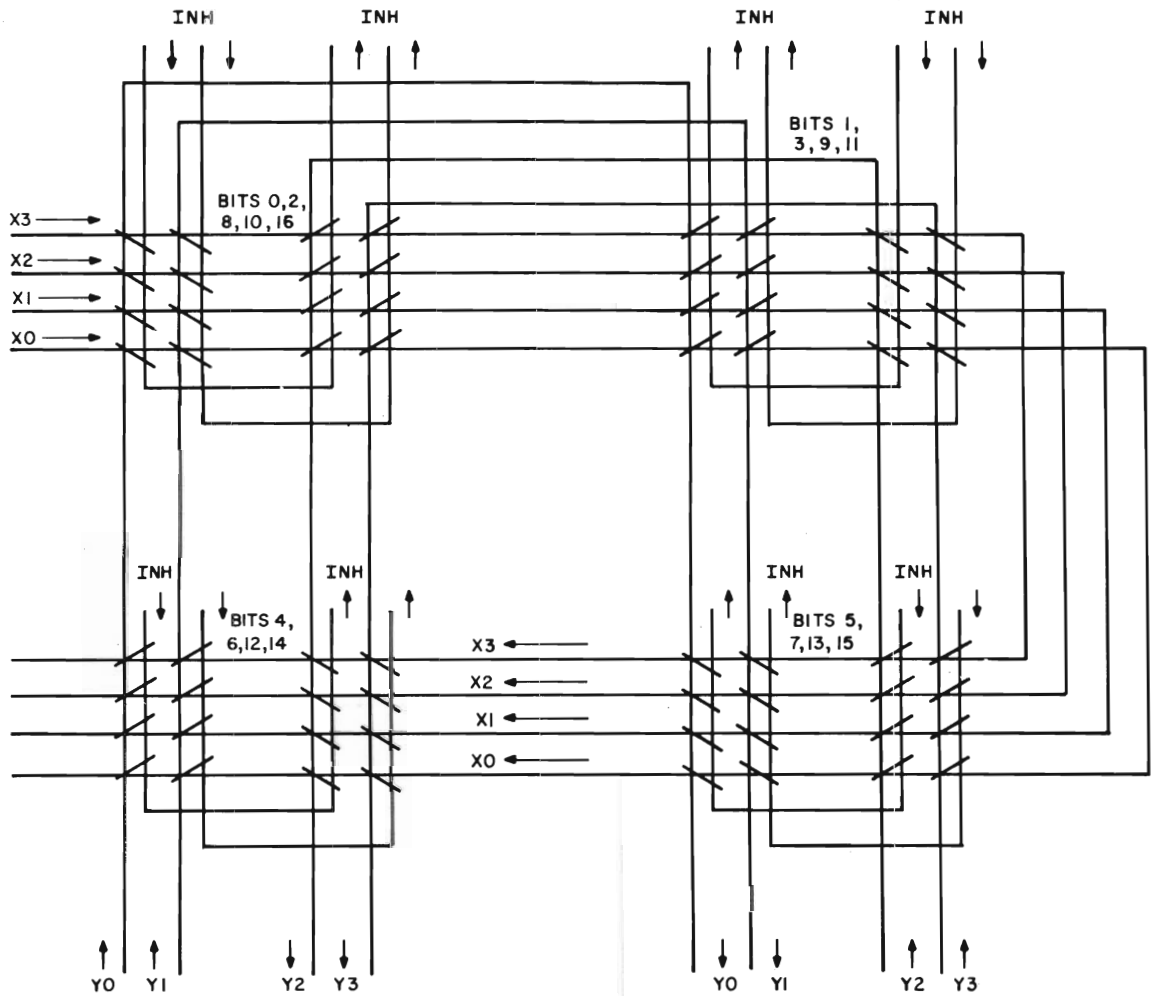
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4. BASIC CORE MEMORY THEORY

This memory is wired in a coincident current, 3D, 3 wire configuration. As an aid in describing basic core switching techniques, a portion of the core plane in the 8KB Memory is illustrated in Figure 2, where the core orientation and wiring configuration of four typical bit planes are shown. Although there are numerous core and wiring configurations existing in various types of memories, the basic core theory still holds for any version.

A core is switched by applying one-half the current, necessary to switch the core, to the appropriate X and Y drive lines. One core in each plane is thereby addressed. During a Read operation, current flow in the drive lines is such as to force the cores to the ZERO state. Nothing occurs in any core which is already in the ZERO state. However, if a core is in the ONE state, the core switches. When the core changes state, a signal is induced in the sense winding for that bit plane. The induced signal is used to generate a ONE indication for that bit position. During a Write operation, current flow is in the opposite direction in the drive lines, and tends to force the cores to the ONE state. An opposing current is applied to the inhibit winding for each bit plane which is to remain at ZERO.

The arrows corresponding to current direction in Figure 2 indicate the current direction necessary through all cores for a Write operation. A half current on X0 and Y0 will switch the cores at the intersection of X0/Y0 to the ONE state; if an X0/Y0 core in a particular bit plane is to remain in its present (ZERO) state, an inhibit current in the appropriate bit plane is also applied to cancel one of the X or Y half currents. During Read, the inhibit current is never applied and the current direction for the X and Y wires is reversed.



NOTE : CURRENT DIRECTION SHOWN FOR "WRITE" PORTION OF MEMORY CYCLE.

Figure 2. Basic Three Wire, 3 D Memory

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5. 8KB MEMORY CORE PLANE CONFIGURATION

For clarity, the core plane wiring is shown in two parts. Figure 3 depicts the X and Y wires and Figure 4 depicts the Sense-Inhibit wires.

Each bit plane contains 64 rows of cores in the horizontal direction (64Y), with each row containing 64 cores (64X), for a total of 4,096 cores (Figure 3). The X and Y wires are common to all bit planes. For a non-parity memory, the cores in Bit 17 are omitted and the X wires terminate as shown. Each bit plane has a pair of Sense-Inhibit windings (Figure 4). These serve a dual purpose: during a Read operation they are used to sense the readout of the cores; during a Write operation, they are used to carry inhibit current. The operation of the core plane is described in greater detail later in this specification.

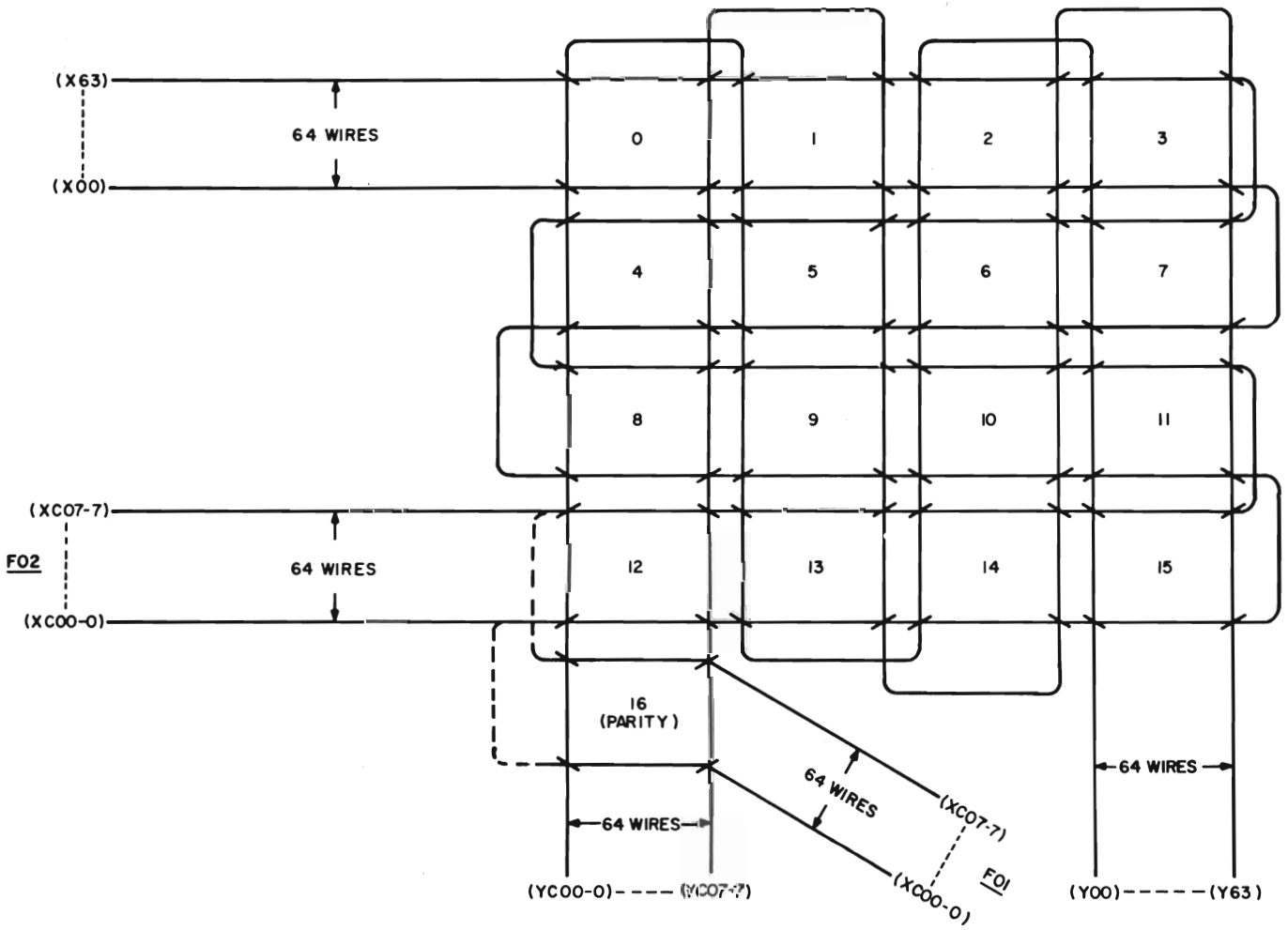


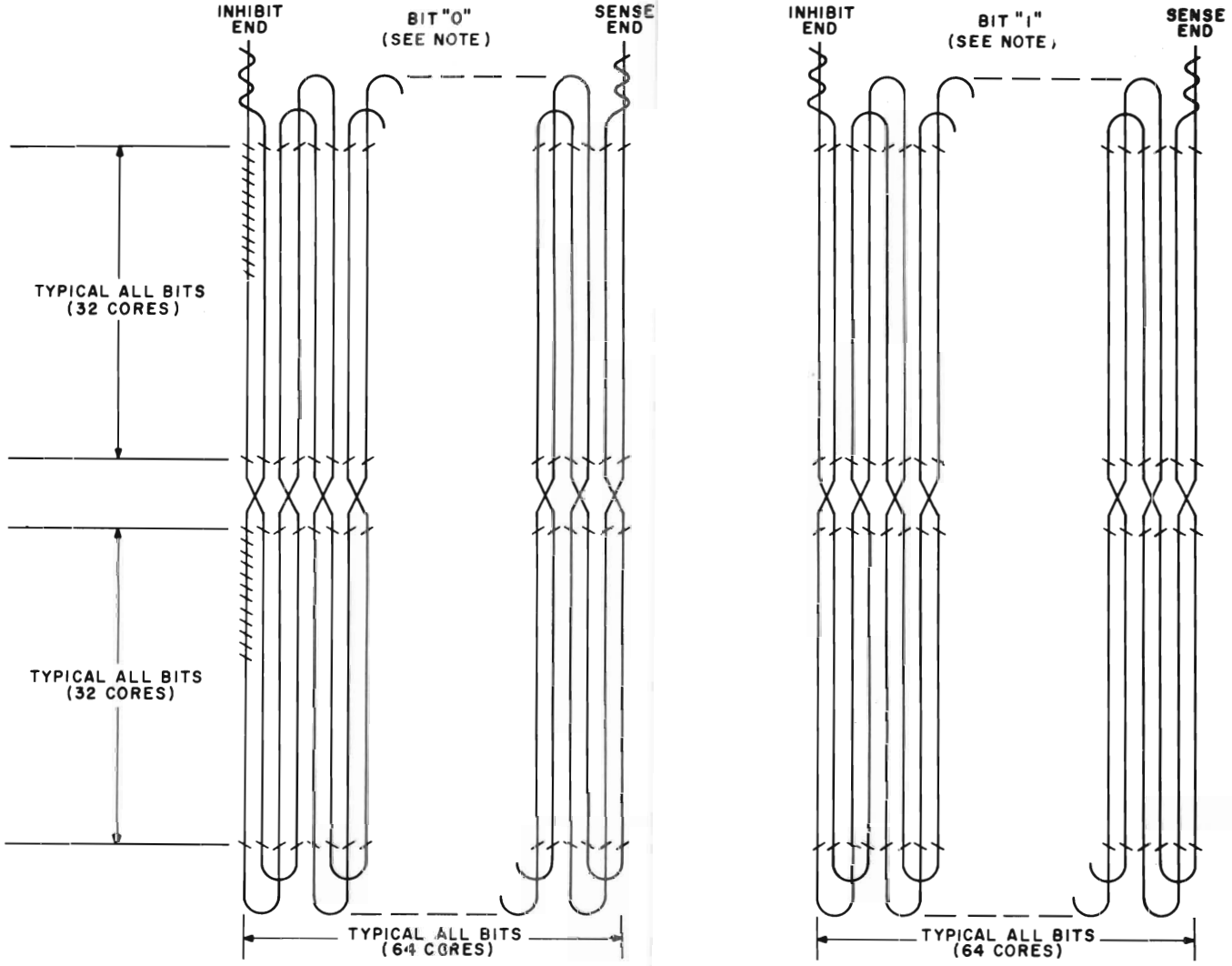
Figure 3. X and Y Core Plane Wiring

Note that the cores are oriented in opposite alignments for specific bit planes. The inhibit current direction alternates in every other bit plane. Inhibit current for bits 0, 2, 4, 6, 8, 10, 12, 14, and 16 flows from + 16.5 volts (at the inhibit end) to ground (at the sense end). Inhibit current for bits 1, 3, 5, 7, 9, 11, 13, and 15 flows from ground (at the sense end) to - 16.5 volts (at the inhibit end). As shown in Figure 4, the inhibit current direction (in any bit plane) in the first two rows of cores (and subsequent alternate pairs of rows) is in the opposite direction from the second two rows of cores (and subsequent alternate second pairs of rows).

Since the Y write current must be such as to always oppose the direction of inhibit current (see Figure 2), the Sense-Inhibit wiring pattern dictates that the Y write current of a pair of Y wires be in a direction opposite to the next adjacent pair of Y wires. This is described in greater detail later in this specification.

The Sense-Inhibit wiring pattern used in the 8KB memory minimizes noise, thereby maximizing readout ZERO-ONE separation.

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NOTE: CORE ORIENTATION SHOWN FOR BIT "0" IS TYPICAL FOR BITS 0,2,5,7,8,10,13,15, AND 16.
CORE ORIENTATION SHOWN FOR BIT "1" IS TYPICAL FOR BITS 1,3,4,6,9,11,12, AND 14.

Figure 4. Sense-Inhibit Core Plane Wiring

6. BLOCK DIAGRAM ANALYSIS

The Block Diagram for the 8KB Memory is on Sheet 6 of Functional Schematic 02-211D08. It consists of five basic blocks The Logic Block receives the four main timing pulses, LR0, W0, ER0, and INH0, and sends a parity indicating signal (PAR0) signifying whether or not the memory has a parity bit. The logic contains double inverting gates for fan-out, and a decoder that generates other timing pulses used in the Y access.

The Y and X Access Blocks receive external memory addresses and timing pulses from the input logic. Each block contains decoders, current switches and drivers, and a diode matrix. Sixty-four wires from the Y Diode Matrix and 64 wires from the X Diode Matrix are threaded through the core plane.

The Inhibit and Sense Block receives memory data and sends memory sense pulses. Each pair of the 17 pairs of dual purpose sense-inhibit wires is threaded through its corresponding bit core plane. The Inhibit and Sense Block also contains the inhibit current drivers, sense amplifiers, strobe circuit, and bus sending and receiving gates.

7. TIMING

The timing for the 8KB Memory is shown in Figure 5. The pulse widths and pulse timing must be maintained within ±9 nanoseconds.

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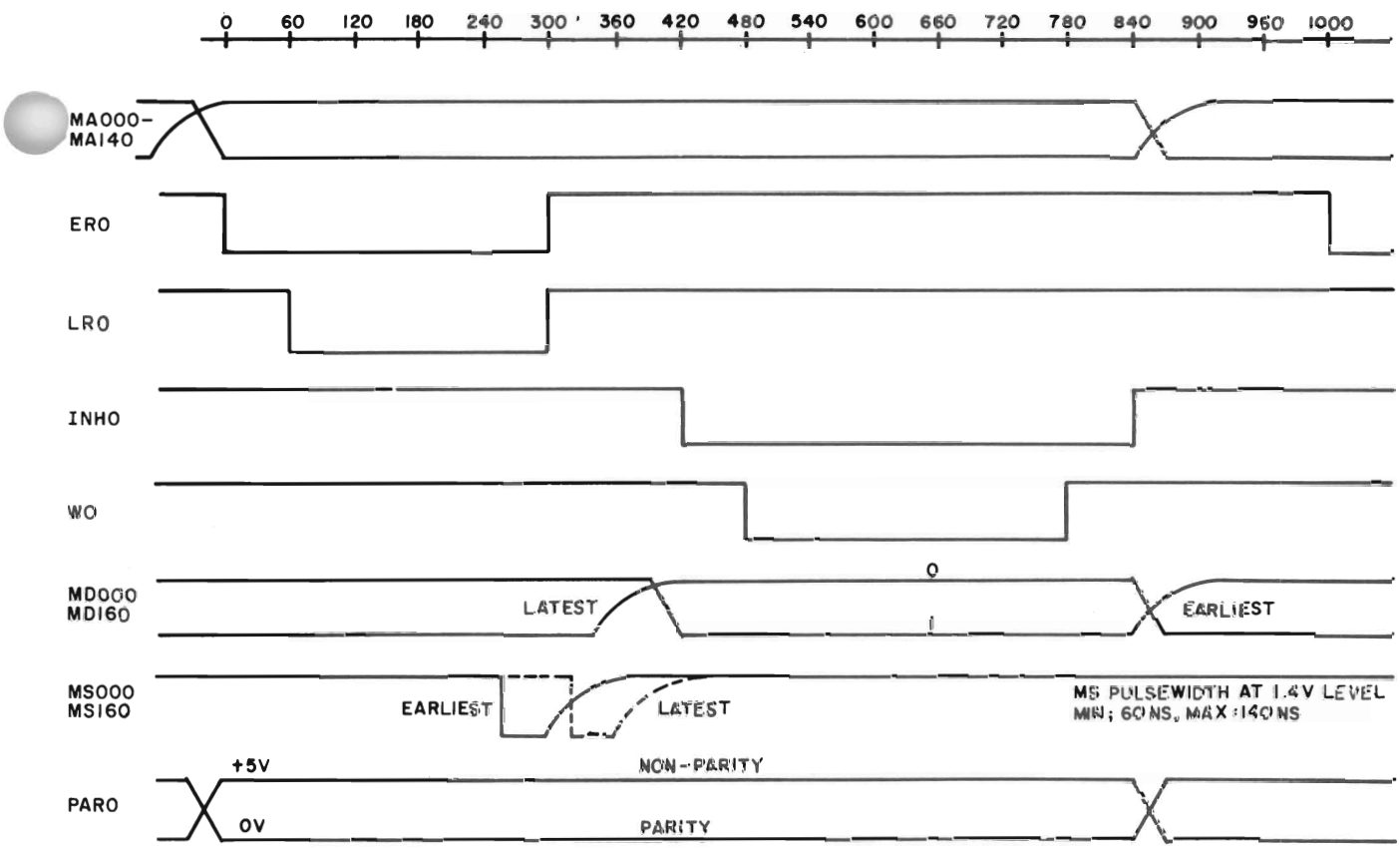


Figure 5. 8KB (Series 5) Memory Timing

For a Write (Erase and Write) operation, ER0 (Early Read) which controls Y drive current, is lowered at T_0 after the address (MA000 - MA140) has settled. LR0 (Late Read) which controls X drive current, is lowered 60 nanoseconds after ER0 is lowered. Both ER0 and LR0 are raised at the same time, at 300 nanoseconds. The addressed word is read and switched to ZERO, and gated onto the MS Bus. The Read data is not written back into the same address location. The net effect is an erase of data in the addressed location.

INH0 (Inhibit Current Control) is lowered 120 nanoseconds after ER0 and LR0 are raised, followed 60 nanoseconds later by the lowering of W0 (Write), which controls the X and Y drive current. W0 is raised 60 nanoseconds before INH0. New data is written into this addressed location depending on MD000 - MD160. Raising the MD line signifies a ZERO; lowering the MD line signifies a ONE.

The times indicated are nominal values with the Processor timing set for a 240 nanosecond period of CLK1.

The Read (Read-Restore) operation timing functions in the same manner as in the Write operation, except that data read out is written back into the same address location.

Output PAR0 is a DC level. When the 8KB Memory is addressed, PAR0 is high if the memory does not have a parity bit and low if it does have a parity bit. This allows Parity Core Memories and Non-Parity Core Memories to be intermixed in the same system.

8. ADDRESSING

Addressing in the 8KB Memory requires the selection of two core plane wires. Figure 6 tabulates the memory address assignments. MA000, MA010, and MA020 are used in selecting up to one-out-of-eight memory boards. This is accomplished on the back panel pins of memory slots in the Processor card file and expansion card file, where each memory slot is uniquely preconnected so that each memory responds to its one-out-of-eight address code. Memory boards can easily be interchanged without necessitating any wiring changes on the memory board itself. Refer to Schematic 02-211D08 Sheet 6, for the memory back panel map and the address decoding table.

The X access contains an 8 x 8 diode matrix to drive current in the 64 X wires. MA030, MA040, and MA050 are used for the X column selection, while MA060, MA070, and MA080 select the X lines. The 64 Y wires are driven by an 8 x 8 diode matrix in the Y access. MA090, MA100, and MA110 select the Y columns and MA120, MA130, and MA140 are used in the selection of the Y lines.

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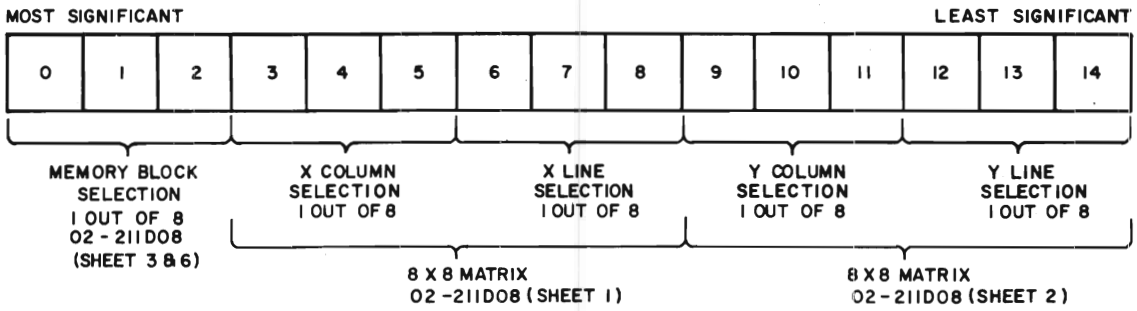


Figure 6. Memory Address Assignments

Figure 7 shows a simplified schematic of the 8KB Memory with Bits 0 and 15 used for illustrative purposes. The sense-inhibit wiring pattern for Bits 0 and 15 is shortened and simplified. The sense amp ends, exit the bit planes in the Y62 an Y63 rows (see Figure 4 for the precise wiring pattern). The direction of inhibit current is shown for each bit plane. Note that in order for the Y current to be opposition to the inhibit current at each core location, appropriate switches must be closed. The currents in YL00 and YL01 must be opposite to those in YL02 and YL03. This current direction alternates throughout successive pairs of Y lines. See Section 9 and Functional Schematic 02-211D08, Sheet 2, for more detailed information on the Y access.

Examples of core switching are tabulated in Table 2, referencing Figure 7. S1 through S16 represent switching circuits.

TABLE 2. CORE SWITCHING EXAMPLES

OPERATION	SWITCHES CLOSED		
	X	Y	Inhibit
Read Core A0 and A1*	S2, S3	S5, S14	---
Read Core C0 and C1*	S2, S3	S10, S13	---
Write One in A0 and Zero in A1	S1, S4	S6, S13	S16
Write Zero in A0 and One in A1	S1, S4	S6, S13	S15
Write One in C0 and Zero in C1	S1, S4	S9, S14	S16
Write Zero in C0 and One in C1	S1, S4	S9, S14	S15

*Cores B0/B1 operate in same fashion as the A0/A1 cores; D0/D1 operate the same as C0/C1.

9. CIRCUIT DESCRIPTION

9.1 Introduction

This section describes the 8KB Memory circuits shown on Functional Schematic 02-211D08. The decoders referenced in the logic and Y and X access sections, are one-out-of-ten decoders in which only eight, or fewer, outputs are used for one-out-of-eight decoding. A high on the D input (pin 12) of any decoder enables the last two outputs that are not used, and disables the first eight outputs. Therefore, the D inputs to the decoders are driven by timing pulses which either enable or disable a decoder. The access decoder outputs are activated, in order, by the memory addresses, with input A being the least significant and the timing pulse on input D being the most significant.

The zone location in the schematics of components referenced or which generates signals referenced during the course of the following descriptions are provided in parenthesis after the circuit designation or signal mnemonic.

9.2 Logic

Refer to Schematic 02-211D08, Sheet 3. The Logic consists of an enabling gate, input buffer gates, inverting gates, a timing decoder, and a parity indicating gate. The three back panel decoded addresses, MA00, MA01, and MA02, are the three inputs to the enabling gate, A3(3B3). The Address Connection Table on Sheet 6 of Functional Schematic 02-211D08 tabulates the eight strap configurations to obtain one-out-of-eight address decoding. Whenever the three inputs to the AND gate A3 are high, the output is high. This enables certain gates in A4, A5, and decoder A2. If any input to AND gate A3 is low, all the above-mentioned gates are disabled to prevent any timing pulses from reaching their destinations in the memory circuits.

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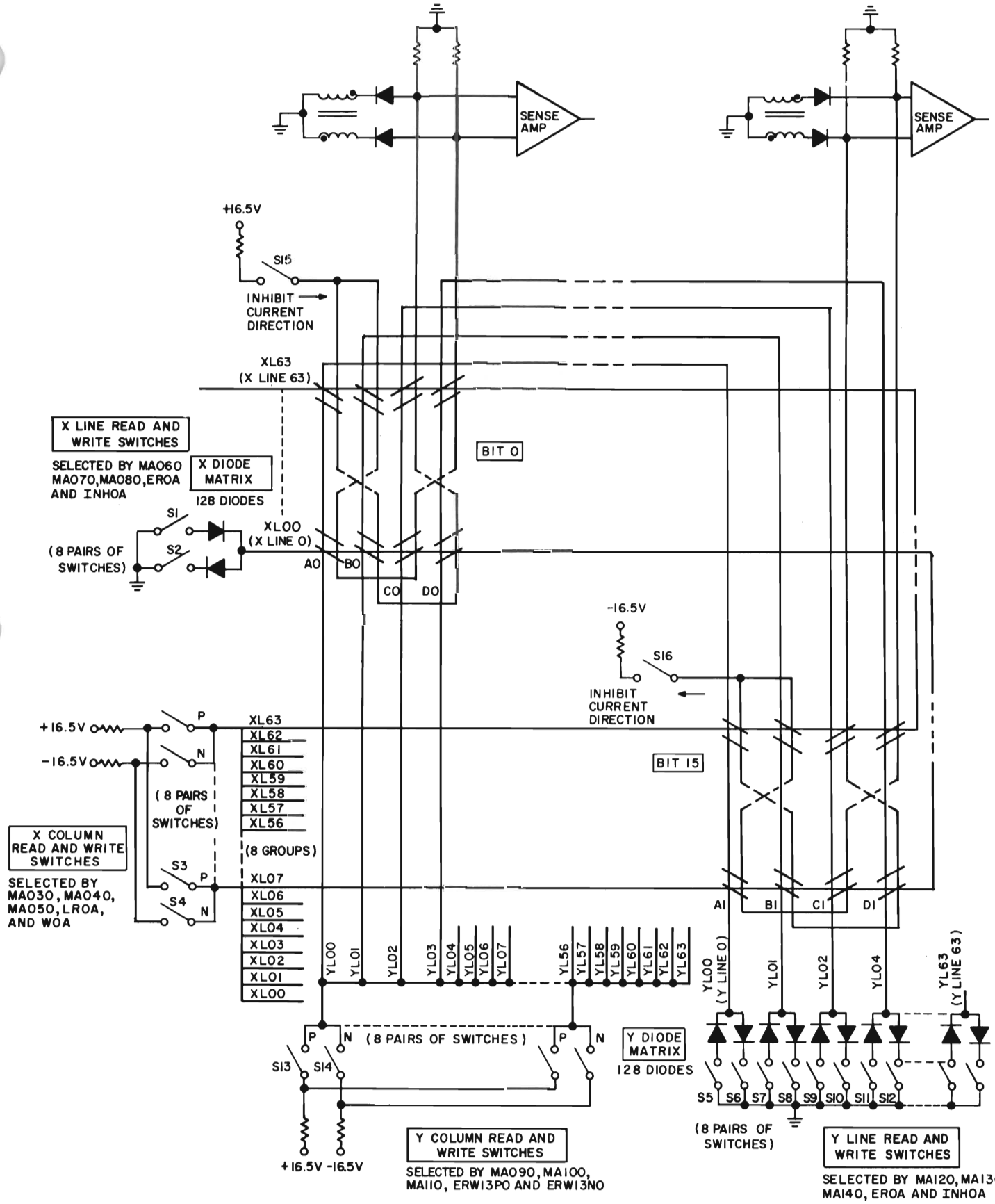


Figure 7. Memory Addressing, Simplified Schematic

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The input to gate A1A (3B4) is strapped to the enable line of A3 (B) when the board contains a parity core plane. Whenever the memory board is addressed, PAR0 goes low. By strapping the input to A1(A) to ground (C), a high PAR0 defines a non-parity memory.

Gates A5 (3E2) buffer and invert the four major timing inputs (LR0, W0, ER0, INH0), and the A4 gates (3E3) then invert these pulses to their correct negative-going levels (LR0A, W0A, ER0A, INH0A) to enable the X and Y access decoders. INH1A (3H2), however, is positive-going to enable the memory data input gates on Sheets 4 and 5. LR1A and W1A are positive-going to turn on the positive and negative current generating switches in the X Access.

Decoder A2 (3E4) decodes ER0A, W0A, and MA130. Two pairs of outputs are OR tied to obtain ERW13P0 and ERW13N0. The ERW13P0 and ERW13N0 signals are used to enable Column Decoders in the Y Access, which effectively reverses the direction of Y drive current (during Read and Write) in successive pairs of Y wires, depending on the state of MA130. ERW13P1 and ERW13N1 are positive-going to turn on the positive and negative current generating switches in the Y access.

9.3 Y Access

Refer to Schematic 02-211D08, Sheet 2. Memory addresses MA120 through MA140 (2A2) are three inputs to one-out-of-eight Read/Write line decoders, A12 and A7. MA090 through MA110 (2S2) are three inputs to the one-out-of-eight Read/Write column decoders, A18 and A13. The Y Access is an eight-by-eight matrix. One-out-of-eight decoder, A12 (2B4) turns on one of the eight line Read switches, Q9-Q16, during Read time when it is enabled by ER0A. Another one-out-of-eight decoder, A7 (2B7) turns on one of the eight Write switches, Q1-Q8, during Write time when it is enabled by INH0A. The decoder A18 (2H2) and the eight positive column switches Q25-Q32 are enabled by ERW13P0, and decoder A13 and the eight negative column switches Q17-Q24 are enabled by ERW13N0. A column is turned on after one of the Write lines has been turned on by INH0A during Write time. For Read, one line and one column are turned on simultaneously. The positive (2D1) and negative (2L1) currents are turned on when gates A20 are enabled by ERW13P1 and ERW13N1 respectively. SCLR0A connects to the second inputs of the current switching gates at 2B1 and 2J1. This input is low during power on power off sequences; the currents are thereby inhibited and memory contents are preserved.

Note that the polarity of alternate line switch transistor pairs (Q9-Q10; Q11-Q12) is reversed in order to drive current into alternate Y line pairs in an opposite direction. The Y Column Decoders correspondingly turn on appropriate positive or negative column switches. The decision of whether to turn on a positive or negative switch is controlled by ERW13P0 and ERW13N0, an OR function of ER0A, W0A, and MA130. MA130 (second least significant) is also a control input to the line decoders, where it turns on pairs of Read or Write switches (each of which is in turn selected by MA140, the least significant). When a Line switch with its collector grounded (Q9, Q10, Q13, Q14, Q3, Q4, Q7, Q8) is turned on, a negative column switch is turned on (Q17 through Q24); conversely, when a Line switch with its emitter grounded (Q11, 12, 15, 16, 1, 2, 5, 6) is turned on, a positive column switch is turned on (Q25 through Q32) to allow current to flow in the Y line which is opposite to that of the current generated by the first example. Also note that the Y Access current is turned on before the X Access current during Read time. This is to minimize the effect of noise on the sense wire which occurs when currents are turned on. Two test points (2G1, 2R1) are available to observe voltages. For a basic example of access operation, see Section 3, Addressing.

The Y Access line and column switches are selected according to the truth table in Table 3. An active decoder output turns on the transistor switch connected to it.

9.4 X Access

The X Access circuit is shown on Sheet 1 of Functional Schematic 02-211D08. Memory addresses MA060, MA070, and MA080 (1A2) are used to drive the one-out-of-eight Read/Write line decoders, A27 and A32. MA030, MA040, and MA050 are used for driving the one-out-of-eight Read/Write column decoders A20 and A21. The X Access is an eight-by-eight matrix. The one-out-of-eight decoder, A27, turns on one of the eight line Read switches (Q53-Q60) during Read time when it is enabled by ER0A. The one-out-of-eight decoder A32 turns on one of the eight line Write switches (Q61-Q68) during Write time, when it is enabled by INH0A. The eight column Read and Write switches (Q37-Q52), when activated by decoders A26 and A21, function in the same fashion. ER0A and INH0A enable the line decoders and switches first; LR0A and W0A enable the column decoders and switches after the line switches have been turned on. The positive (1D1) and negative (1L1) currents are turned on when gates A20 are enabled by LR1A and W1A respectively. SCLR0A connects to the second inputs of the current switching gates at 1B1 and 1J1. This input is low during power on/power off sequences; the currents are thereby inhibited and the memory contents are preserved. Two test points (1G1, 1R1) are available for observing voltages. For a basic example of access operation, see Section 8, Addressing. The X Access line and column switches are selected according to the truth table in Table 4. An active decoder output turns on the transistor switch connected to it.

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TABLE 3. Y SELECTION DATA

Y LINE SELECTION DATA						
ER0A	INH0A	MA120	MA130	MA140	Decoder Output	Mnemonic
0		1	1	1	A12-09	YL00P0
0		1	1	0	07	YL01P0
0		1	0	1	06	YL02N0
0		1	0	0	05	YL03N0
0		0	1	1	04	YL04P0
0		0	1	0	03	YL05P0
0		0	0	1	02	YL06N0
0		0	0	0	01	YL07N0
	0	1	1	1	A7-09	YL00N0
	0	1	1	0	07	YL01N0
	0	1	0	1	06	YL02P0
	0	1	0	0	05	YL03P0
	0	0	1	1	04	YL04N0
	0	0	1	0	03	YL05N0
	0	0	0	1	02	YL06P0
	0	0	0	0	01	YL07P0

Y COLUMN SELECTION DATA						
ERW13P0	ERW13N0	MA090	MA100	MA110	Decoder Output	Mnemonic
0		1	1	1	A18-09	YC00
0		1	1	0	07	YC01
0		1	0	1	06	YC02
0		1	0	0	05	YC03
0		0	1	1	04	YC04
0		0	1	0	03	YC05
0		0	0	1	02	YC06
0		0	0	0	01	YC07
	0	1	1	1	A13-09	YC00
	0	1	1	0	07	YC01
	0	1	0	1	06	YC02
	0	1	0	0	05	YC03
	0	0	1	1	04	YC04
	0	0	1	0	03	YC05
	0	0	0	1	02	YC06
	0	0	0	0	01	YC07

9.5 Sense-Inhibit Circuits

The Sense-Inhibit Circuits are shown in 02-211D08, Sheets 4 and 5. Since the circuits in Sheets 4 and 5 are similar, only Sheet 5 will be used in the description. Nine MD gates, A38, A40, and A45 (5A2-5R2), are used to turn on the nine Inhibit switches, Q77-Q85 (5A3-5R3). During Write time, INHIA (5A1) is high enabling the nine MD gates. The state of the MD lines determines if a ONE or a ZERO is to be written at a particular address. A high MD (Write Zero) line turns on the Inhibit switch causing current to flow in the Sense-Inhibit wires. This current cancels the X or Y current with the result that the core remains in the ZERO state (not switched). A low MD (Write One) will not turn on the Inhibit switch. The coincident X and Y current causes the core to switch to the ONE state.

Bit 0, 2, 4, 6, and 8 currents flow from +16.5 volts, through switches, to ground. Bit 1, 3, 5, and 7 currents flow from ground, at the balun network (5A5-5R5), to -16.5 volts through switches. The inhibit current is divided through a pair of Sense-Inhibit wires (5A4-5R4) unique to each bit. The balun network at the sense end equalizes the current in each pair of Sense-Inhibit wires. Note, therefore, that the Inhibit switch carries approximately 600 milliamps with 300 milliamps flowing in each leg of the Sense-Inhibit pair.

During Read time, bipolar readouts are sensed by the sense amplifiers, A44, A48, A49, A55, and A56 (5A6-5R6). The positive-going sense amplifier output is enabled by the positive-going strobe pulse STBB1. The VT (threshold voltage) of the sense amplifiers is adjusted to provide maximum ZERO/ONE margins. The voltage division at the reference input to the sense amplifier is approximately 100 to 1.

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TABLE 4. X SELECTION DATA

X LINE SELECTION DATA						
ER0A	INH0A	MA060	MA070	MA080	Decoder-Output	Mnemonic
0		1	1	1	A27-09	XL00N0
0		1	1	0	07	XL01N0
0		1	0	1	06	XL02N0
0		1	0	0	05	XL03N0
0		0	1	1	04	XL04N0
0		0	1	0	03	XL05N0
0		0	0	1	02	XL06N0
0		0	0	0	01	XL07N0
	0	1	1	1	A32-09	XL00P0
	0	1	1	0	07	XL01P0
	0	1	0	1	06	XL02P0
	0	1	0	0	05	XL03P0
	0	0	1	1	04	XL04P0
	0	0	1	0	03	XL05P0
	0	0	0	1	02	XL06P0
	0	0	0	0	01	XL07P0

X COLUMN SELECTION DATA						
LR0A	W0A	MA030	MA040	MA050	Decoder-Output	Mnemonic
0		1	1	1	A26-09	XC00
0		1	1	0	07	XC01
0		1	0	1	06	XC02
0		1	0	0	05	XC03
0		0	1	1	04	XC04
0		0	1	0	03	XC05
0		0	0	1	02	XC06
0		0	0	0	01	XC07
	0	1	1	1	A21-09	XC00
	0	1	1	0	07	XC01
	0	1	0	1	06	XC02
	0	1	0	0	05	XC03
	0	0	1	1	04	XC04
	0	0	1	0	03	XC05
	0	0	0	1	02	XC06
	0	0	0	0	01	XC07

The flip-flop circuit at location 5A8, which is typical of all the sense amp flip-flops, is used in the following description: The set input (Pin 5 of A60) goes high when a Strobe pulse (STBD1) is generated. The positive-going sense amp output (when a ONE is read out) is inverted by gate A57, whose output connects to the ONE side of the flip-flop (Pin 6 of A60). If a ONE is read out, the flip-flop is reset. The ZERO side of the flip-flop (Pin 3 of A60) is inverted by A58 and the negative-going pulse is placed on the MS Bus. When the Strobe pulse (STBD1) goes low, the flip-flop is set again. If a ZERO is read out, the flip-flop is never reset and the MS Bus stays high.

9.6 Sense Auxiliary Circuits and Decoupling

Refer to Schematic 02-211D08 Sheet 3 during the following descriptions.

9.6.1 Strobe. The Strobe pulse (STB0) is derived from a dual single shot monostable, A42 (3N2). The negative-going edge of LR0A triggers the first monostable. The negative-going output from the second monostable is connected to fan-out and inverting gates, A41. STBA1 and STBB1 enable the sense amplifiers; STBC1 and STBD1 are used to set the MS flip-flops. Potentiometer P2 (3N1) and Capacitor C85 (3N2) are timing components used to vary the Strobe pulse delay. C114 and R251 determine the width of the Strobe pulse. A test point, STB, is provided to observe the strobe.

9.6.2 VT. The VT circuit (3M5) provides a regulated threshold voltage for the sense amplifiers. This VT can be varied by P1. Terminals 129-1 and 228-1 allow connection to an external test circuit to override the VT circuit for factory test purposes. A test point is provided to measure VT.

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9.6.3 -6.2 Volts. The network at 3N7 derives -6.2 volts from the -16.5 volt source. The -6.2 volts is one of the supply voltages required by the sense amplifiers.

9.6.4 Thermistor. The thermistor connections to the back panel are shown at 3S7. The thermistor is a temperature sensitive device which connects to the ± 16.5 volt power supply. The ± 16.5V will vary as the temperature varies. At 0°C the supply voltages are approximately 18.00 volts; at 50°C the supply voltages are approximately 15.00 volts. (See Section 11.2, Voltage Adjustment, and Figure 8.) This temperature/voltage tracking is necessary since the memory drive current requirements vary with temperature; at 0°C more drive current is required, while at 50°C less drive current is required to realize optimum memory performance.

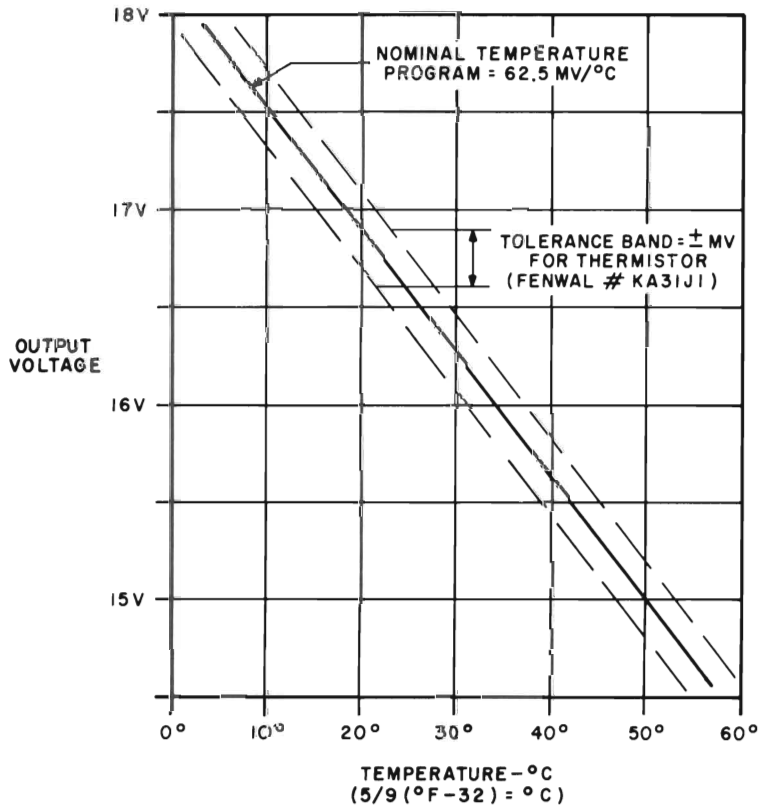


Figure 8. Thermistor Temperature Program

9.6.5 Decoupling. Various capacitors are used throughout the board for voltage decoupling. Their values and their approximate physical location in the vicinity of IC's are referenced at 3B7 through 3K7.

10. TEST POINTS

Figure 9 illustrates the approximate physical locations of test points. These are tabulated in Table 5 with their corresponding location in Functional Schematic 02-211D08.

TABLE 5. TEST POINT LOCATIONS

Test Point	Function	Schematic Location
VT	Sense Amplifier Threshold Voltage	3S5
STB	Strobe	3M3
LR0A	X Column Read Timing and Strobe Generation	1G2
GRD	Ground	
PYC	Positive Y Column Voltage	2G1
NYC	Negative Y Column Voltage	2R1
PXC	Positive X Column Voltage	1G1
NXC	Negative X Column Voltage	1R1

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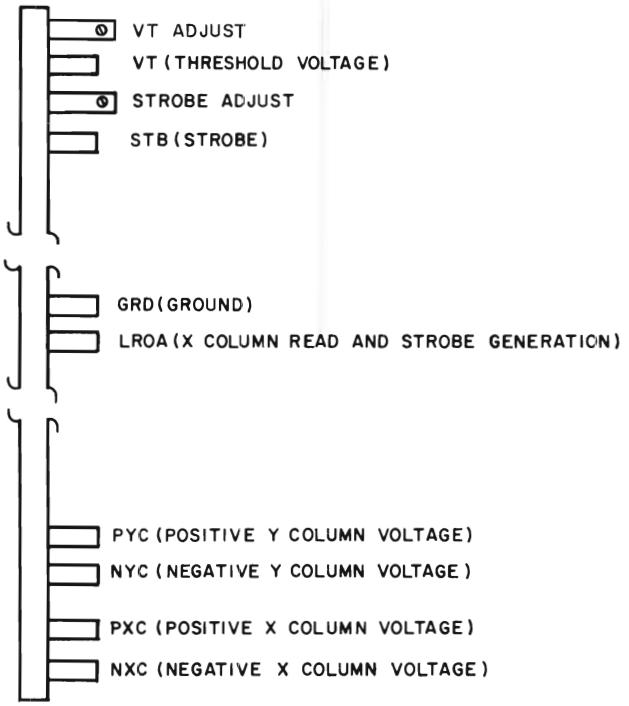


Figure 9. Memory Test Points

11. TESTS AND ADJUSTMENTS

11.1 Introduction

This section describes tests and adjustments which should be used periodically as a check of memory system operation, and as an aid in troubleshooting when a memory problem exists. Perform the checks in the order that they are listed in this section.

NOTE

The power supply adjustments listed in the appropriate Power System Manual, and the system clock adjustments listed in the appropriate digital system maintenance manual, should be performed prior to the memory adjustments.

11.2 Voltage Adjustment

The nominal ± 16.5 volt input to the memory system should be checked prior to any other memory checks. The 16.5 volt regulator on the power supply has a control input from a thermistor mounted on the memory board. It is therefore important to consider the ambient temperature when adjusting the 16.5 volt regulator. The following test equipment is required for this adjustment.

1. A laboratory thermometer accurate to ± 1%.
2. A digital voltmeter capable of reading 15 to 18 volts ± 1%.

Use the following procedure to check, and adjust if necessary, the 16.5 volt regulator.

1. Measure the ambient temperature. Refer to Figure 8 and determine the voltage setting for the temperature measured.
2. Compare the voltage of -16.5 and +16.5 at the back panel terminals to assure that the voltages are equal. If the voltages are not equal, adjust the trimpot on the power supply to obtain equal readings.
3. Measure the voltage at the +16.5 back panel terminal.
4. Adjust the trimpot on the power supply to obtain the reading calculated in Step 1.

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11.3 Strobe Timing Adjustment

There is a single timing adjustment on the 8KB Memory.

CAUTION

The adjustment described in this section is carefully set at the factory using sophisticated test equipment not normally available in the field. The adjustment is very stable and should not require field adjustment. The adjustment should be changed only after the check provided indicates that it is out of tolerance and there are no faulty components in the system.

A dual trace oscilloscope with a calibrated time base is required for this check. Use the following procedure to check strobe timing.

1. Load and run the appropriate Memory Test Program.
2. Synchronize the oscilloscope to the negative-going edge of LR0A on TP "LR0A". (See Figure 9). Observe this pulse.
3. On the second trace, observe the strobe pulse on TP "STB" (see Figure 9). The relationship should be as shown in Figure 10.
4. If the relationship is not as shown in Figure 10 and all components are found to be operating correctly, adjust the Strobe trimpot shown on Figure 9.

The above is a rough adjustment that places the strobe in the general correct area. The VT trimpot is increased to 2.0 volts (see Section 11.5, Marginal Test, for proper procedure). If there are memory errors, the Strobe trimpot is fine adjusted until there are no errors. Then verify that there are no errors with VT at 1.0 volts. When memory is operating properly, adjust the VT trimpot back to its nominal 1.5 V ± 0.1V.

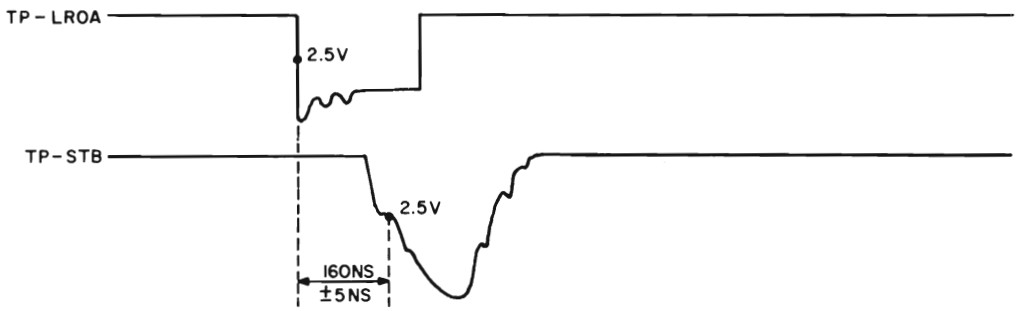


Figure 10. LR0A - STB Relationship

11.4 Memory Test

Run the appropriate Memory Test Program.

11.5 Marginal Test

The following Marginal Test may be performed periodically to locate memory areas which may cause future problems. Test equipment required for this test is:

1. A voltmeter capable of measuring 5 volts ± 2%.

Use the following procedure:

1. Connect the voltmeter to test-points VT and GRD.
2. Run the Memory Test referenced in Section 11.3.
3. Vary the VT trimpot to 1.0 volt and then to 2.0 volts. The test program should continue to run normally within these VT voltages. Return VT to its nominal 1.5 volts ± 0.1 V setting after tests are completed.

11.6 Trouble Shooting Aid

Sheets 7 and 8 of Drawing 02-211D08 are provided as an aid in trouble-shooting circuits and locating components. They are used in conjunction with Functional Schematic 02-211D08, Sheets 1 through 6.

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12. MEMORY MNEMONICS

The following list provides a brief description of each mnemonic in the 8KB Memory. The 02-211D08 source of each signal is also provided.

MNEMONIC	MEANING	LOCATION
ENABLE1	Enables logic and access circuits	3C3
ER0	Early Read; X and Y lines read timing pulse	3E1
ERW13N0 ERW13P0 ERW13N1 ERW13P1	Early Read or Write; Y column read and write current direction control timing pulses	3H5
INH0	Inhibit; X and Y lines write, and inhibit drivers timing pulse	3E1
LR0	Late Read; X column read timing pulse and strobe generation	3E1
MA00-MA02	Decoded Memory block selection address	3B1
MA030-MA140	Memory Address Bus	2A2, 2S2, 3A2, 3S2
MD000-MD160	Memory Data Bus	4A1-4N1, 5A1-5R1
MS000-MS160	Memory Sense Bus	4B9-4S9, 5B9-5S9
NXC	Negative X column voltage	1R1
NYC	Negative Y column voltage	2R1
PAR0	Parity indicating signal	3A5
PXC	Positive X column voltage	1G1
PYC	Positive Y column voltage	2G1
SCLR0A	System Clear	1A1
STB0	Strobe Pulse	3N3
STBA1 and STBB1	Enables sense amplifiers	3S3
STBC1 and STBD1	Sets MS flip-flops	3S5
TEMPA	Connection to thermistor	3S7
TEMPB	Connection to thermistor	3S7
VT	Sense amplifiers threshold voltage	3S6
W0	Write; X and Y column write timing pulse	3E1
XC00-XC07	X column wires (common)	1J6-1S6

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MNEMONIC	MEANING	LOCATION
XC00-0 through XC07-7	X wire; Column 0, Wire 0 through Column 7, Wire 7	1J5-1S5
XL00N0-XL07N0	X Line Cathodes	1F6-1F9
XL00P0-XL07P0	X Line Anodes	1F6-1F9
YC00-YC07	Y column wires (common)	2J6-2S6
YC00-0 through YC07-7	Y Wire; Column 0, Wire 0 through Column 7, Wire 7	2J5-2S5
YL00N0-YL07N0	Y Line Cathodes	2F6-2F9
YL00P0-YL07P0	Y Line Anodes	2F6-2F9

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SELECTOR CHANNEL

M70-103
NS SELECTOR CHANNEL
INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-232 Selector Channel (SELCH) (Product Number M70-103) in a Model 70, 74, 80, 7/16 or 7/16 HSALU Processor System. The NS Selector Channel is complete on one 35-391M02 printed circuit board.

2. PHYSICAL CHARACTERISTICS

2.1 Dimensions **15 3/8 x 14 7/8"**

2.2 Weight **$2\frac{1}{2}$ pounds maximum**

3. INSTALLATION

The NS SELCH may be installed in any even numbered universal expansion slot (i.e., 0, 2, 4, or 6) in the Central Processor Unit (CPU) or in the first memory-I/O expansion chassis. See Figure 1. On 7/16 HSALU the NS SELCH may only be installed in Slot 0 of the CPU back panel.

To install a NS Selector Channel on a Model 74 or a 7/16 BASIC, the Selector Channel must be a 35-391M02. To install a Selector Channel on a 7/16 HSALU the Selector Channel must be a 35-391M02, R02 or higher.

NOTE

A SELCH may be installed in slots 0, 1, or 2 of a Model 80/85 CPU chassis only. In this case cutting of the multiplexor bus is not necessary.

3.1 Back Panel Wiring

3.1.1 Multiplexor Channel Bus. **At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the SELCH and the next higher numbered slot on the One (1) connector only. The RACK0/TACK0 daisy chain wiring on the back panel is rerouted according to Figure 1. The lower numbered card slots in the chassis become part of the private SELCH Bus on the One (1) connector only.**

For the convenience of cutting the Multiplexor Bus, the connections between every other slot are made using "top" wire wraps. (This refers to wire wrap back panels only.) This allows the cutting of the bus by simply lifting the top wraps when the SELCH is installed in an even numbered slot. Refer to Figure 1 A during the following example.

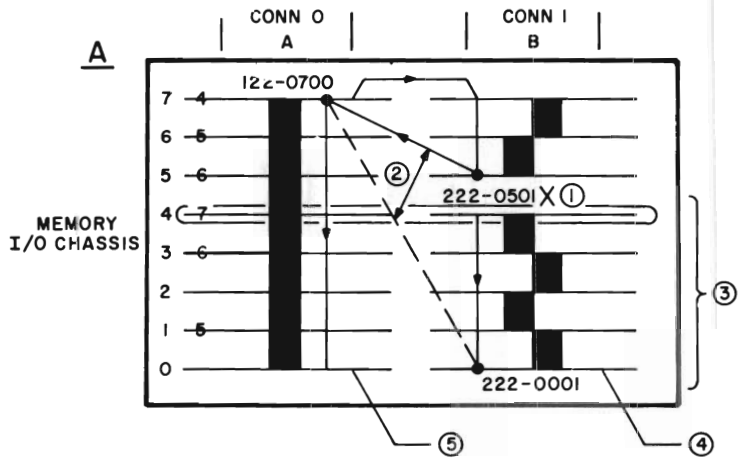
To install a SELCH in Slot 4:

1. **Remove all wires on Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2. (See backpanel map in 02-232M01D08 Sheet 7.)**
2. **Remove the wire between 222-0001 and 122-0700.**
3. **Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the Zero (0) and One (1) connectors of Slot 4.**
4. **Connect 122-0700 to 222-0501.**
5. **Install the SELCH into Slot 4 of the chassis. The private SELCH Bus now appears on the Connector One (1) side of Slots 4, 3, 2, 1, and 0. All slots on the Connector Zero (0) side and Slots 7, 6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.**

To install a SELCH in any other even numbered slot of a CPU chassis or a Memory-I/O chassis, a similar procedure is followed. Refer to Figure 1 B, C, D, and E.

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NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, AND C REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.



TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

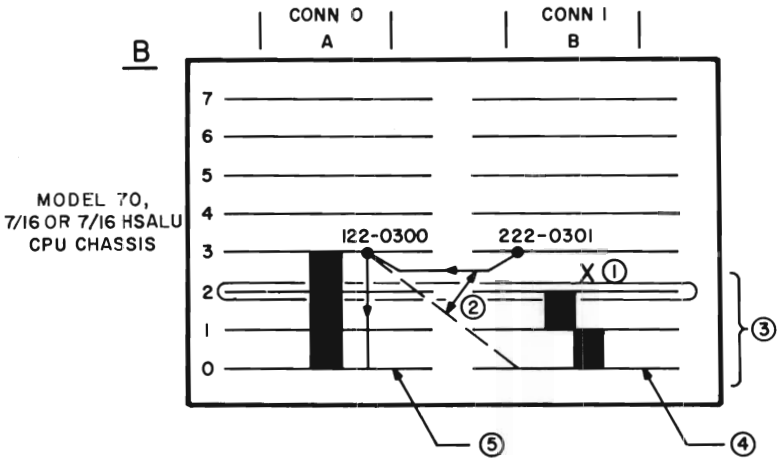
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE, AND SLOTS 7, 6 AND 5 ON CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ MEMORY MODULE 7, IF IT EXISTS, MUST BE LOCATED IN SLOT 3.



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

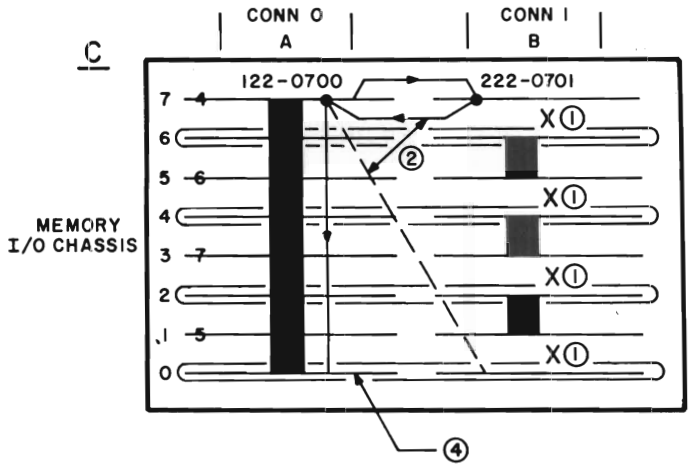
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

NOTE: 1
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, ANY SELECTOR CHANNELS MUST BE INSTALLED IN THAT CHASSIS.

NOTE: 2
A SELECTOR CHANNEL MAY NOT BE INSTALLED IN SLOT 2 OF THE 7/16 HSALU. SLOT 0 IS THE ONLY SLOT IN WHICH A SELCH MAY BE INSTALLED.



TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2 AND 0) OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

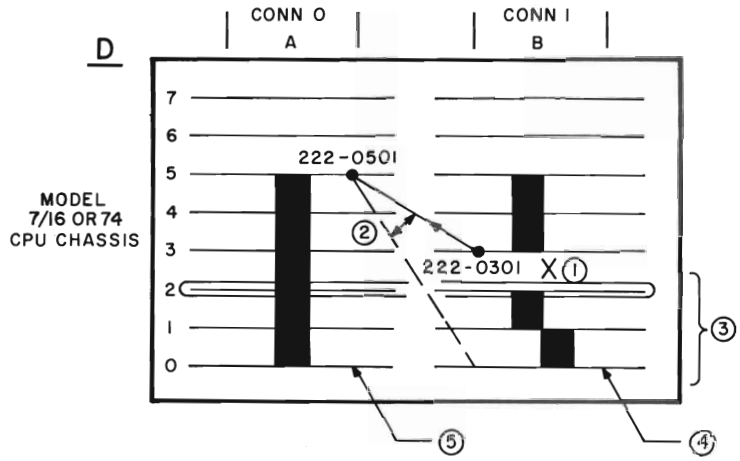
③ EACH SELCH, EXCEPT THE ONE IN SLOT 0, HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3 AND 5 ON CONNECTOR ONE (CONN.1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ MEMORY MODULES 5 AND 7, IF THEY EXIST, MUST BE LOCATED IN SLOTS 1 AND 3.

Figure 1. Backpanel Modifications

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TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

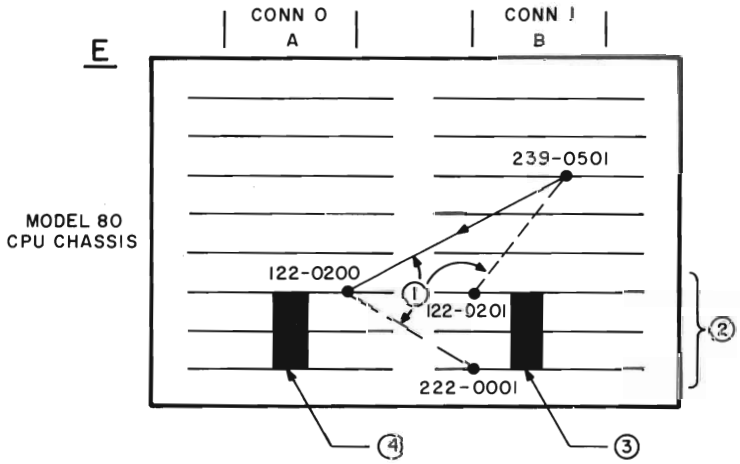
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHE CHASSIS BY INSTALLING A CABLE HERE.

NOTE:
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, THE SELECTOR CHANNEL MUST BE IN SLOT 0 OF THE CPU CHASSIS OR IN SOME SLOT OF THE EXPANSION.



TO INSTALL A SELECTOR CHANNEL IN SLOT 0, 1 OR 2 CHASSIS——

① JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPERS.

② THIS SECTION BECOMES THE PRIVATE SELCH BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR SLOTS.

③ EXTEND THE SELCH BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

④ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

NOTES:
1. IF A 17-183 CABLE IS INSTALLED BETWEEN CONNECTORS ZERO AND ONE IN THE CPU CHASSIS. THIS CABLE MUST BE REMOVED PRIOR TO INSTALLING SELCH.
2. THE INSTALLATION OF A SELCTOR CHANNEL OR OTHER I/O DEVICE CONTROLLER IN THE M80 CPU CHASSIS REDUCES THE MAXIMUM MEMORY SIZE BY 16K BYTES (ONE MSU) FOR EACH SLOT USED!
3. ONLY ONE SELECTOR CHANNEL MAY BE CONFIGURED IN THE MODEL 80 PROCESSOR CHASSIS.

Figure 1. Backpanel Modifications
(Continued)

3.1.2 ACT0/TAC0. The ACT0/TAC0 jumper between Pins 137-0 and 237-0 must be removed from the slot used by the SELCH controller. If the Selector Channel is not the first Direct Memory Access (DMA) channel on the Memory Bus, jumper "K" on the SELCH controller must be removed. Note that on a Model 74 only one DMA device is permitted.

NOTE (Not Applicable on Model 74)

On installations with Multiple SELCH's, remove the "EN0" and the "INH0" filters on all but the last SELCH (Remove the following: R70, R72, C59 and C61).

3.2 Cabling

The cabling necessary for the SELCH depends on the system's physical configuration. When the SELCH Bus does not extend outside the chassis, no cabling is required. When the SELCH Bus must be extended to another chassis, a number of cable configurations can be used. See Figure 2. Care should be taken to minimize bus lengths.

See Figure 2 for a summary of cables. Refer also to User's Manual, Publication Number 29-261, for further details on system configurations.

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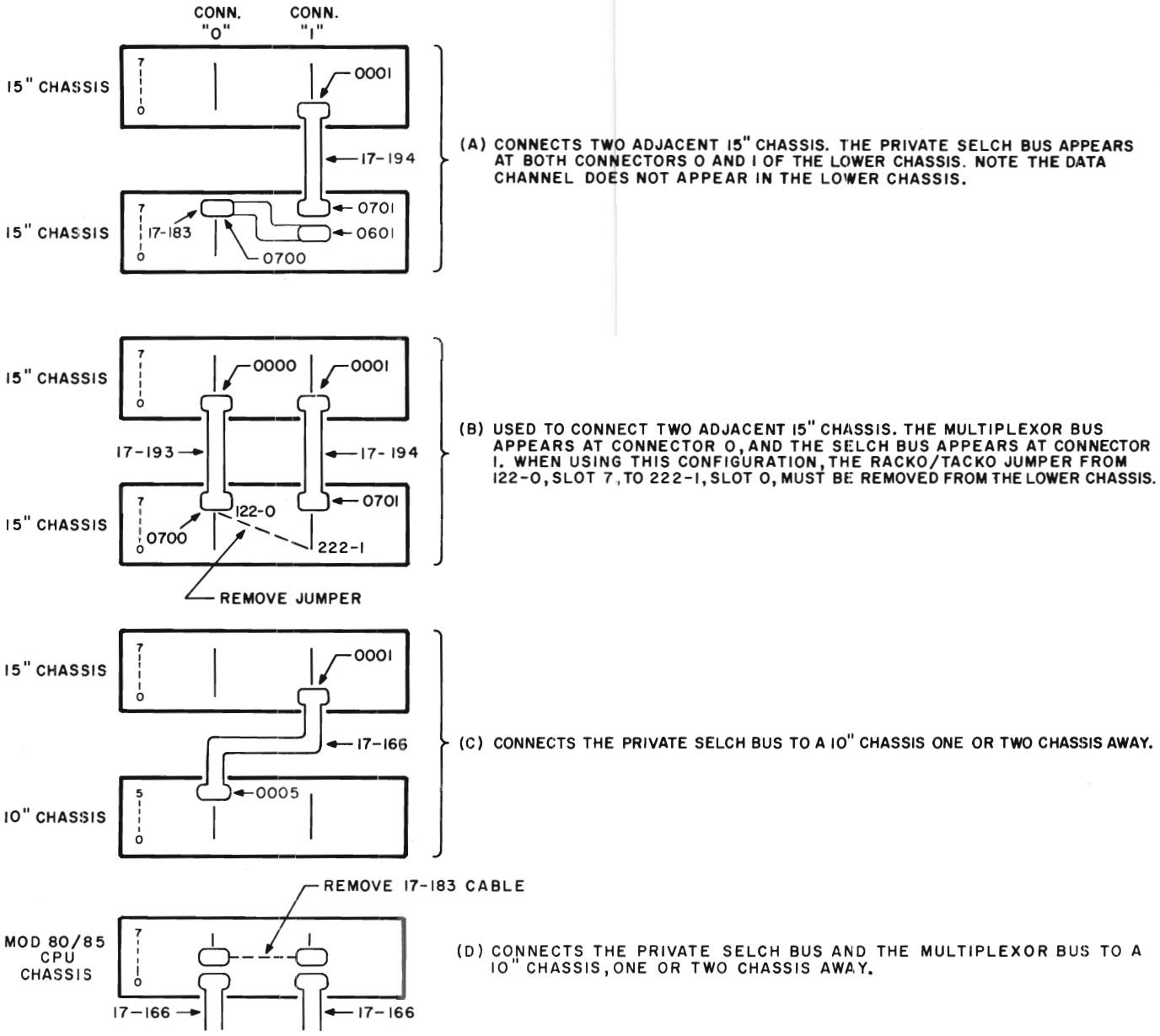


Figure 2. Cabling

4. ADDRESS STRAPPING

The preferred address of the NS Selector Channel is X'F0'. The controller is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-232M01D08. The number and letter designations shown on the schematic refer to the designations on the apparatus side of the SELCH controller board.

5. MODEL 80/85 STRAPPING

For use with the Model 80 or 85 the following options must be exercised:

1. Remove the jumper labled J located between IC 14 and 15.
2. Change the jumper, above IC 53, from (L to X) to (L to 2).

6. INSTALLATION CHECKS

The NS SELCH is factory tested using a special high speed device. Therefore, field checks are contingent upon the user having appropriate hardware and software available with which to exercise the Selector Channel. When the SELCH is used with Model 80 or 85, insure that the strap options on the SELCH have been made according to Section 5.

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M70-103
NS SELECTOR CHANNEL
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-232M01 NS Selector Channel (SELCH) (Product Number M70-103) is a Direct Memory Access port (DMA) which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the Processor. The Processor sets up the device controller, loads the SELCH with the starting and final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO Command. The SELCH then handles the transfer without further direction by the Processor.

The NS Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The SELCH provides the drivers, receivers and termination resistors for the private SELCH Bus. This bus originates at Connector One (1) of the SELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private SELCH Bus can be extended to other chassis, as required. For installation information, refer to Installation Specification 02-232M01A20.

2. SCOPE

This specification describes the operation of the SELCH in its various modes; Setup, Memory Read, Memory Write, and Termination. Where necessary, this specification references the Multiplexor Channel Bus and Memory Bus operations. These buses are described in detail in the User's Manual, Publication Number 29-261.

3. BLOCK DIAGRAM ANALYSIS

Refer to the SELCH block diagram on Sheet 7 of Functional Schematic 02-232M01D08, and the SELCH Flow Chart, Figure 1, during the following analysis. Before initiating a data transfer via the SELCH, the device controller and the SELCH must be set up. The setup procedure is implemented by the Processor via the Multiplexor Bus (MPX-Bus). When the SELCH is in the Idle mode, the MPX-Bus is tied directly to the private SELCH Bus through the SELCH. This allows the Processor to communicate directly with any device on the private SELCH Bus.

To prepare the SELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines D080:150 by four consecutive Data Availables (DAs) from the Processor. The first two Data Availables simultaneously load the AR and AAR, which are 16-bit incrementing registers. The AR is incremented, by two, after each halfword is transferred to/from memory, and the AAR is incremented, by one, with each byte transferred to/from the device. Data transfer is terminated when the AAR is equal to the FAR or when the AAR increments past its maximum value, X'FFFF'.

Data transfer is begun by the Processor issuing a GO Command to the SELCH. Transfer to/from the device is now independent of the Processor. The GO Command also prevents communication between the Processor and any device on the private SELCH Bus until the transfer is terminated and the SELCH is addressed.

Data transfer is controlled in the Move Data circuit by inspection of the four least significant bits of the Status Byte presented by the active device on the private SELCH Bus. When any one of the three least significant bits are set, (EX, EOM, or DU), the transfer is terminated. Bit-12 (Busy) regulates the rate of data transfer. In the Memory Read mode, the actual data transfer begins with a memory request, REQ0 active, as soon as a GO Command is issued. When the memory request is serviced by the Processor, the SELCH Memory Bus Control circuit activates Select (SEL), which gates the contents of the Address Register (AR) onto the Memory Address Bus, and gates a halfword of data from memory into the Data Register (DR). At the termination of the memory transfer, the data is loaded from the DR to the Data Buffer (DB) and the AR is incremented.

NOTE

Unless the SELCH has dropped REQ0 in time to remain selected during the next memory cycle, the SELCH is deselected by the rising edge of Inhibit (INH0) after the halfword has been transferred.

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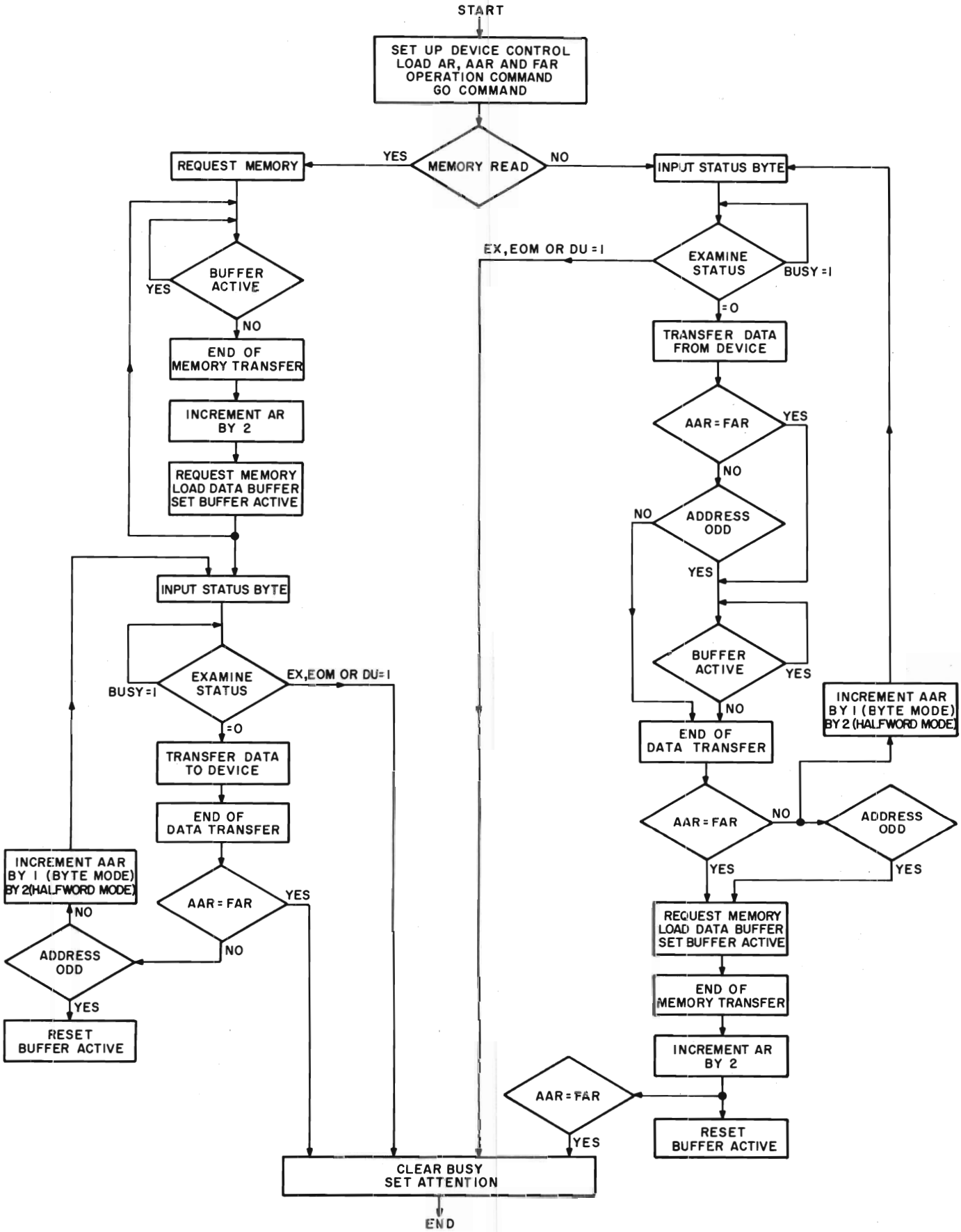


Figure 1. Flow Chart

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Once the DB is loaded, data transfer to the device over Private Data Lines PD000:150 is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and contents of the Final Address Register, or until the transfer is aborted due to an error condition.

In the Memory Write mode, the data transfer sequence described previously for Memory Read mode is reversed. That is, two bytes of data are loaded into the DR from the device prior to a memory request and the data flow is from the device to the DR, DR to the DB, and finally into memory.

The Branch Gate circuit and the Move Data circuit control the flow of data between memory and the device. The Branch Gate supervises the overall data flow, while the Move Data circuit performs the handshaking between the SELCH and the active device on the private SELCH Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the SELCH Busy flip-flop which is presented to the program as Bit-12 of the SELCH Status Byte.

Selector Channel Status and Command Byte Data is shown on Table 1.

TABLE 1. SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP			

BSY — When this bit is set, a one shot generates the EBS1 pulse to start the appropriate SELCH operation. When this bit is cleared an interrupt is generated.

READ — This command, Bit-2, sets the Memory Write (WT) flip-flop. The controller on the SELCH Bus is setup for a device Read operation.

GO — This command, Bit-3, clears the MSC flip-flop and sets the BSY flip-flop to initiate the Data Transfer mode.

STOP — This command, Bit-4, from the Processor clears the BSY flip-flop and initializes the Load/Unload Sequencer. During the Data Transfer mode, execution of the command is delayed until the end of a memory cycle, if one is in progress.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section relates to Functional Schematic 02-232M01D08, Sheets 1 through 6. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 (D08). The last character (0) inidicates that when D080 is active, the line is at a logical Zero level.

4.2 SELCH Control Circuit

In the Idle mode, the SELCH Address (2M8), Busy (3F3), and Multiplexor-SELCH (MSC) (3FA) flip-flops are reset and the private SELCH Bus is tied directly to the Multiplexor Bus. This allows the Processor to communicate, via the Multiplexor Bus, with any device on the private SELCH Bus.

To communicate with the SELCH, it must first be addressed. The SELCH Address (X'F0' preferred) is placed on Data Lines D080:150 (1A3-8) and the Address control line is activated (ADRS0)(4B8). The SELCH Address is decoded by the four input NAND gate (1F4) and the Address flip-flop is set (2M8). The set output from the Address flip-flop (AD1)(2J7), when active, prevents the control signals on the MPX-Bus from passing onto the private SELCH Bus by holding the Control Line Gate inactive (CLG1) (1B2). Capacitors C33 and C34 (4D8) delay the propagation of the Private Address control line (PADRS0) (4F9) to the SELCH Bus, so that when the SELCH is being addressed PADRS0 does not become active. This delay allows the SELCH to be addressed without resetting the Address flip-flop of the active device on the private SELCH Bus.

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The simultaneous loading of the Address Register (AR) and Auxiliary Address Register (AAR), and the loading of the Final Address Register (FAR) is accomplished by four consecutive Data Availables (DAs) from the Processor. The Load/Unload Sequencer (2L2) controls the loading of these registers (AR, AAR, and FAR) and the unloading of the AAR. The sequencer is set to its initial state by the termination of the last data transfer, a Stop Command, or a System Clear (SCLR0)(4MS) so that the first DA, through Data Available Gate (DAG0)(2L4), will activate Load Address Register High (LARH0)(2S2).

LARH0 gates Data Lines DA081:151 (1D3-8) into the eight most significant bits of the AR and AAR. The rising edge of the first and each successive Data Available Gate (DAG0)(2L4) increments the sequencer and allows the next DA to activate the next load line. The second DA loads the eight least significant bits of these registers. The third and fourth DAs will then load the Final Address Register in the same order. The contents of the AAR may be inspected, via the program, by issuing two Data Requests (DR) to the SELCH whenever the Load/Unload Sequencer is in its initial state. (e.g., Upon termination of a SELCH transfer, sequencer initialized, the FAR may be inspected to determine if the entire block of data had been transferred.)

If a Memory Write operation is desired, an Output Command with Bit-10 set must be issued to set the Write flip-flop (3F5). Since the Write flip-flop is reset by the Data Available/Request Gate (DARG1)(2L5) whenever a DA or DR is sent to the SELCH (setup procedure), no command is necessary to initiate a Memory Read operation.

Data transfer commences with a GO Command from the Processor, which is an Output Command with Bit-11 set. The GO Command sets both the Busy (3F3) and MSC (3F4) flip-flops. The setting of the Busy flip-flop causes an End of Busy Set pulse (EBS1) (3H4) to be generated. This pulse is generated from the falling edge of BSY0 (3F3), and is used by the Branch Gate circuit to initiate the transfer cycle. The Busy latch circuit remains set until the Selector Channel detects the termination of transfer and its state is presented to the program via Bit-12 of the Sense Status Byte.

The MSC flip-flop is reset by SCLR0A or by addressing the SELCH, Set Gate active (SGAD1)(2L9), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the Selector Channel.

Information is steered from the SELCH to both the Data Lines D080:150 (1B4-9) and the Private Data Lines PD080:150 (1S4-9) by the proper gating of four each, four-to-one line multiplexors (Sheet 1). For example; with the SELCH idle, Busy reset, all Data Lines are tied directly to the Private Data Lines in both directions.

4.3 Memory Bus Control Circuit

Memory Bus Control timing relationships are shown in Figure 2. A SELCH request for memory is started by activating Set Request (SREQ0)(3S4). SREQ0 is activated by the Branch Gate circuit (3M8) when either the SELCH has received a halfword of data from the device or, in the Memory Read mode, whenever the Memory Data Register is available to accept the next halfword.

SREQ0 is applied to the direct set input of the Request flip-flop (REQ)(4L5) which sets the flip-flop and sends REQ0 to the Processor. When REQ0 is received, the Processor generates Enable (EN0). EN0, on the first DMA device, is jumpered to Accept (ACT0) which generates the daisy chain priority loop through all DMAs in the system. The daisy chain begins at the highest priority DMA as EN0, and propagates to the lower priority DMAs as Transmit Accept (TAC0) until it is captured by the first DMA requesting a memory cycle. When the REQ flip-flop is set and ACT0 (EN0) is active, the ACT0/TAC0 contention circuit (4H2) blocks the propagation of TAC0, and provide highs on the J input to the SEL flip-flop and the K input to the REQ flip-flop. Thus, on the rising edge of EN0, the Select flip-flop becomes set and the Request flip-flop is reset. When the SELCH REQ flip-flop is reset and ACT0 (EN0) is active, the ACT0 signal is propagated as TAC0 to the DMA with a lower priority.

The trailing edge of Inhibit (INH0) (4H5), from the Processor, indicates the end of the memory cycle. This edge, unless the SELCH has dropped REQ0 in time to remain selected during the next cycle, causes the SEL flip-flop to reset. Two pulses, End of Memory Transfer (EMX0) (4M7) and Inhibit (INH0P) (4M2), are generated by the leading and trailing edges of INH0 respectively. EMX0 is used by the Branch Gate circuit to indicate the end of the memory transfer. The Address Register is toggled by the AND function of SEU and INH1.

In the Memory Read mode, the Memory Data Register (MDR) is cleared by Clear Data Register (CDR0) (4R2) which is generated by the trailing edge of REQ1. Write Not (WT0A) (3F5) is ANDed with SEL1 to form Enable Memory Data Read (ENMDR1) (4R6), which gates the contents of the MDR onto the Memory Data Lines MD000:150 (Sheet 6) for the restore portion of the memory cycle. (This function is disabled when using solid state memory.) The contents of the memory location accessed is gated to the direct set inputs of the MDR by Enable Memory Strobe (ENMS1) (4R4). This function is WT•SEL•CDR0 for use with core memory and WT•SEL•INH when using solid state memory (4R4).

When writing to memory, the contents of the Data Buffer is gated onto Memory Data Lines MD000:150 (Sheet 6) by Enable Memory Data Write (ENMDW1)(4R3), when selected. A Memory Write operation is indicated to the Processor by activating WRT0A (4S3).

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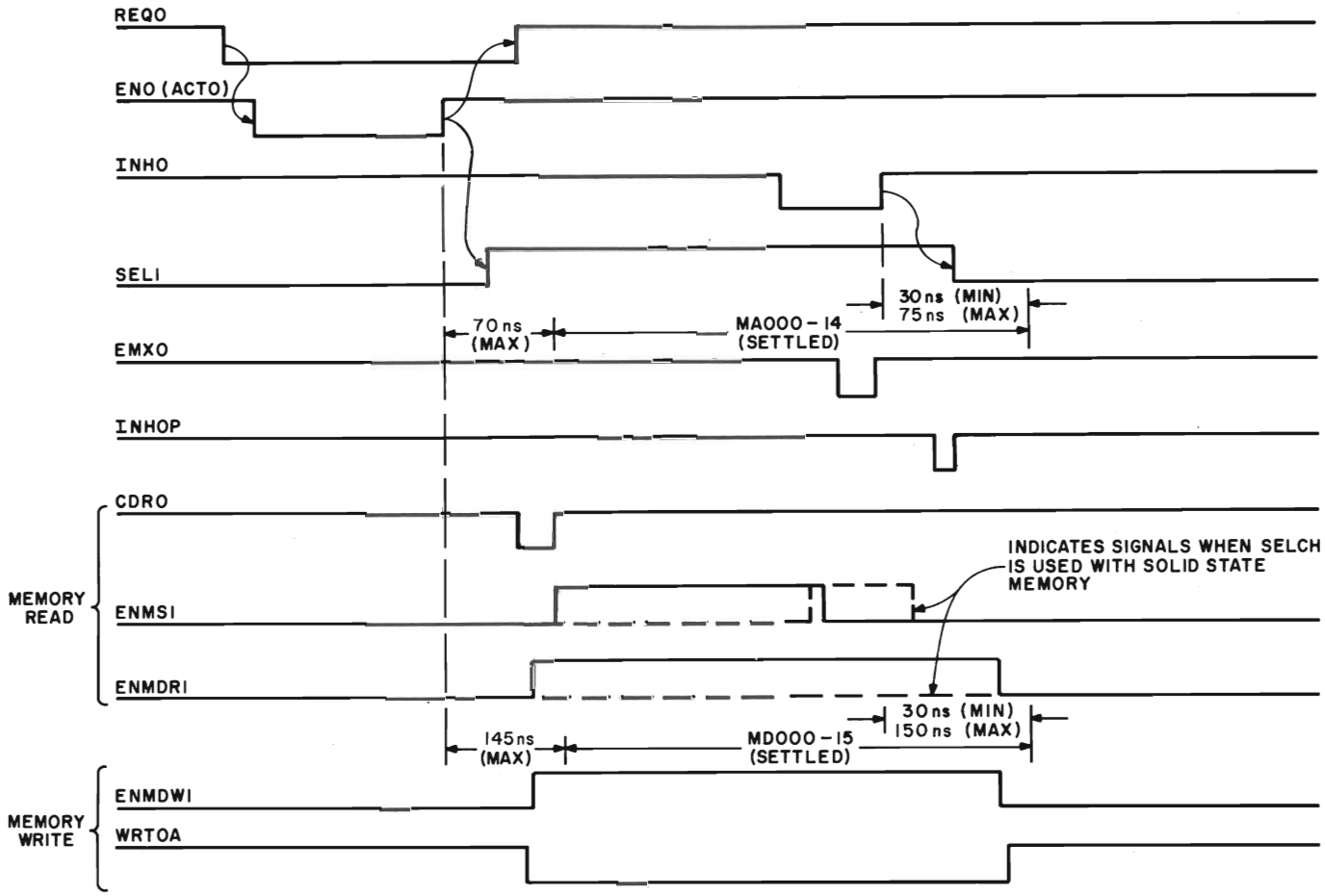


Figure 2. Memory Bus Control Timing Diagram

4.4 Address Register and Auxiliary Address Register.

The Address Register (AR) and Auxiliary Address Register (AAR) (Sheet 5) each consist of four, four-bit counters. These registers are loaded simultaneously by the Processor from Data Lines D080:150 (1A3-8), under control of the Load/Unload Sequencer (as discussed in Section 4.2), with the starting address from which the block transfer is to begin. The contents of the AR (Sheet 5) is gated onto Memory Address Lines MA000:140 (5R1-8) whenever the SELCH is selected, SEL flip-flop set. The AR is incremented with each memory transfer by Select·Inhibit (SINH0) (4K8). The AAR (Sheet 5) keeps track of the transfer between the SELCH and the device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0) (3M1). When the transfer is in the Halfword mode, TAAR0 is generated twice for each transfer. The outputs of the AAR are used by the Match circuit to determine the end of the data block. Its contents may be examined, via the program, by issuing two consecutive DRs to the SELCH when the sequencer is initialized. In addition, AAR151 is used in the Byte Transfer mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the AAR (CO0) (541) terminates the transfer, clear Busy, when a transfer is attempted past the maximum memory address. This feature prevents 'wrap-around' in memory.

4.5 Final Address Register

The Final Address Register (FAR) is implemented by four quad latches (Sheet 5). This register, like AR and AAR, is loaded by the Processor under control of the Load/Unload Sequencer. The outputs of this register are used exclusively by the Match circuit to determine when the final address of the transfer is reached.

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4.6 Memory Data Register and Data Buffer

The Memory Data Register (MDR)(Sheet 6) is a 16-bit register composed of 16 edge triggered JK flip-flops. In the Memory Read mode, the MDR is first cleared by Clear Data Register (CDR0) (4R2) and then direct set by each active bit on Memory Strobed Data Lines MS000:150 (Sheet 6). During a Memory Write, the data, in double rail format, present at the J and K inputs to the MDR, is toggled into the flip-flops on the trailing edge of either Load Data Register High (LDRH0)(649) or Load Data Register Low (LDRL0)(6J9).

As soon as the MDR is loaded, if the Data Buffer (DB) is empty (as determined by the inactive state of the Buffer Active flip-flop)(3H1), the MDR contents are loaded into the DB (Sheet 6) by Load Data Buffer (LDB1)(357). Information present in the DB is, in turn, either written into memory via Memory Data Lines MD000:150 or sent to the device on Private Data Lines PD000:150.

4.7 Data Transfer Circuit

Refer to Figure 3 for Memory Read timing diagrams and Figure 4 for Memory Write timing diagrams. The Memory Read timing diagram shows the timing of a three byte transfer, in the Byte mode, of 2,000,000 bytes/second. Figure 4 shows a transfer of two halfwords, in the Halfword mode, to a slower device.

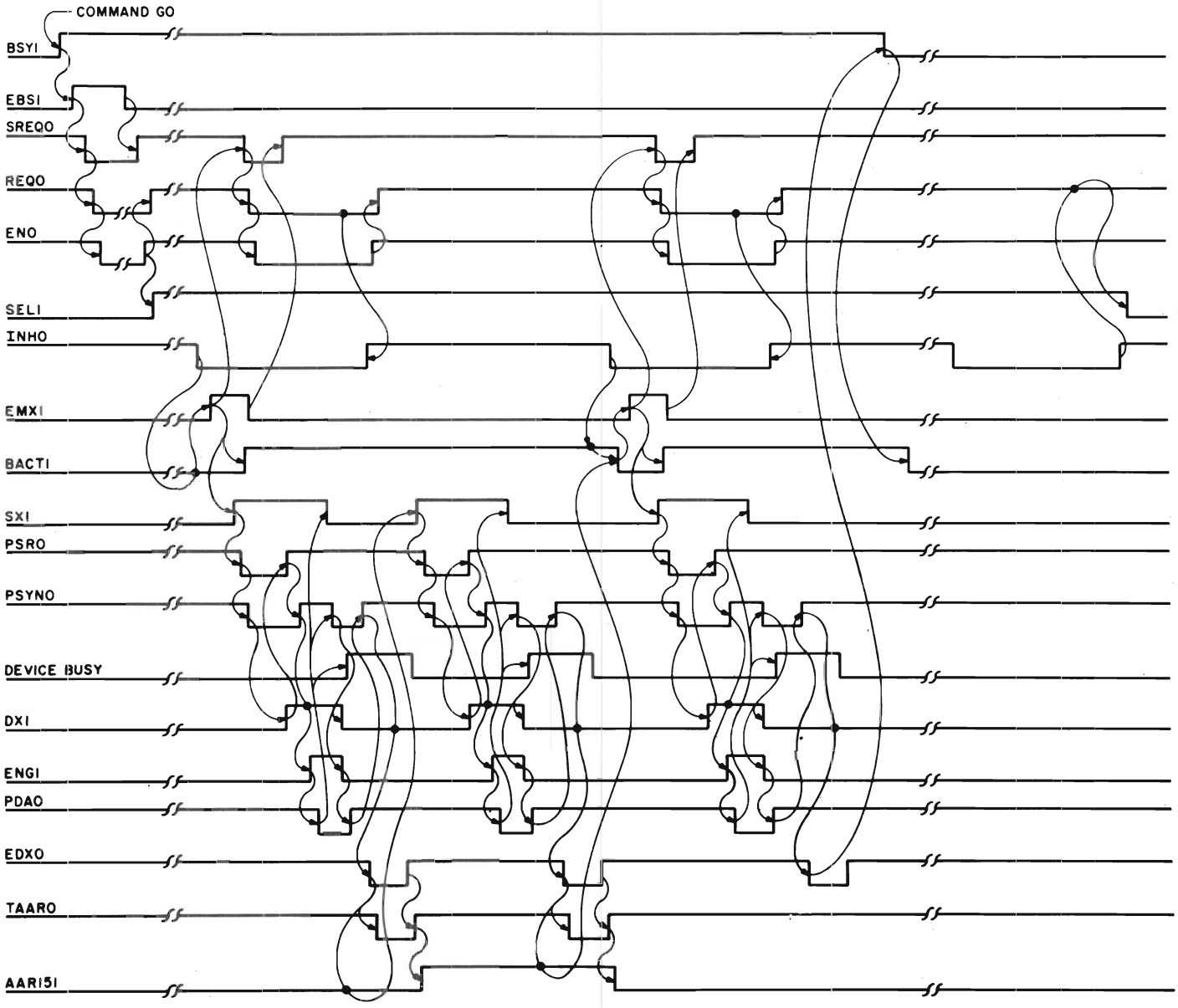


Figure 3. Memory Read (Byte Mode)

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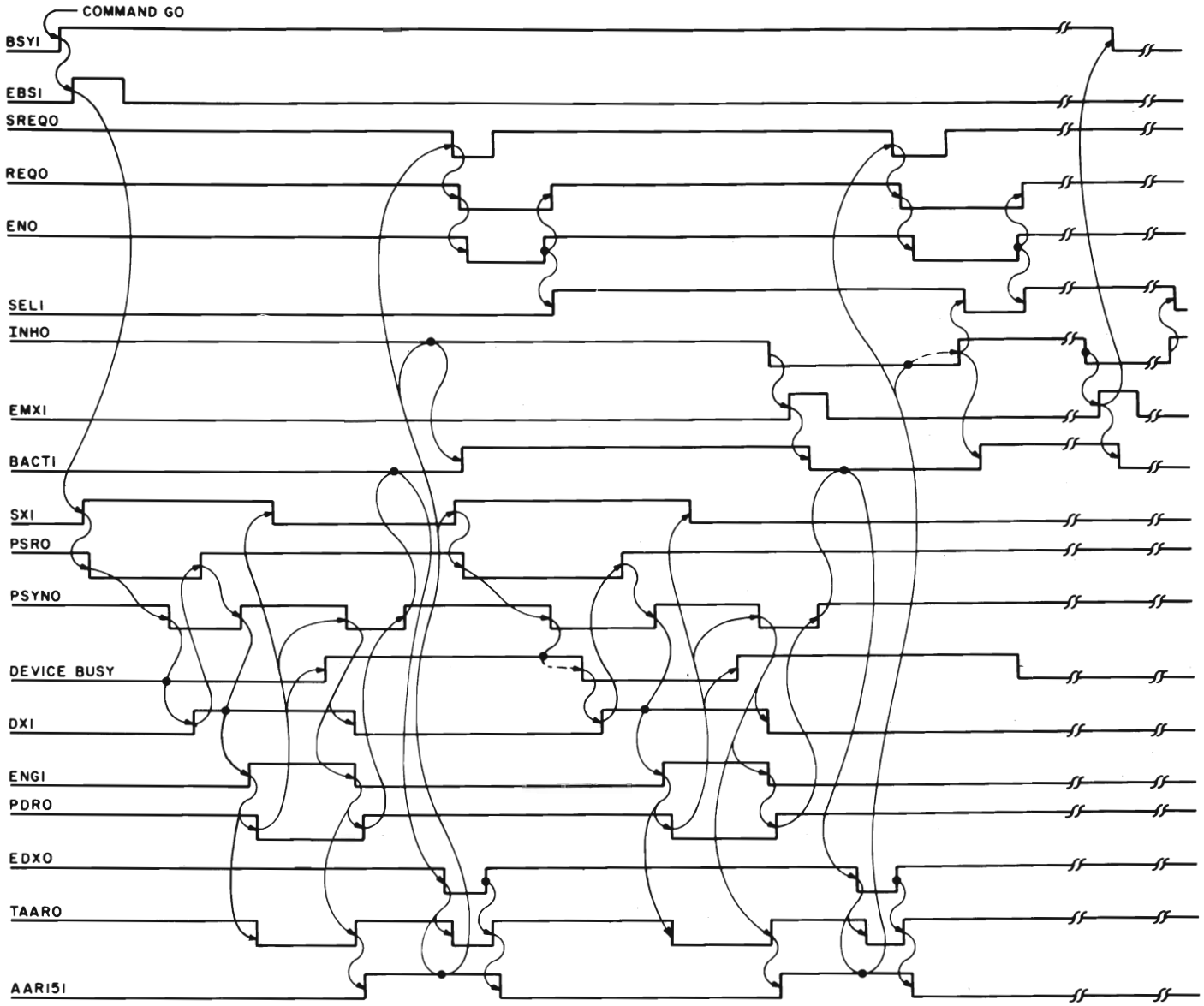


Figure 4. Memory Write (Halfword I/O Mode)

A GO Command to the Selector Channel sets the Busy flip-flop which generates the End of Busy Set pulse (EBS1)(3K8).

In the Memory Read mode, EBS1 is decoded by the Branch Gate circuit and SREQ0 is generated. Thus, a request for memory is initiated. When the halfword of data is present in the MDR, the End of Memory Transfer pulse (EMX1)(4R6) becomes active and the Branch Gate circuit once again requests memory and generates Set Status Transfer (SSX0)(3S5) and Load Data Buffer (LDB1) (3S7). These signals initiate the transfer to the device and load the Data Buffer (DB) respectively.

SSX0 sets the Status Request flip-flop (3F6) which activates the Private Status Request control line (PSR0)(3G6) to the active device on the private SELCH Bus. This Status Request examines the four least significant bits of the Status Byte. If any of the three least significant bits (EX, EOM, or DU) are set, the transfer is terminated by resetting the Busy flip-flop (3F3). The assumption is made that each of these status bits remain reset for the remainder of this discussion. With Bit-12 (Busy) of the Status Byte reset, the Data Transfer flip-flop becomes set (3F7). Data Transfer (DX0)(3E1) inhibits the generation of PSR0, which causes Private Sync (PSYN1)(4B4) from the device to become inactive. This enables Engage to go high (ENG1)(3D8), which allows the Private Data Available control line (PDA0)(3H5) to become active. The Private Data Available/Request signal (PDAR1)(3H5), generated whenever a Private Data Available (PAD0) or Private Data Request (PDR0) signal is active, will then clear the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset and ENG1 goes low, disabling PAD0. When the Sync is removed by the device, an 80 nanosecond End of Data Transfer pulse is generated (EDX0) (3J8) which increments the Auxiliary Address Register and is used by the Branch Gate circuit to generate a function in accordance with the truth table for EDX on Sheet 3. This cycle continues until termination of the transfer is detected.

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In the Memory Write mode, WT1 active (3F5), EBS1 is used to generate SSX0, and the Branch Gate circuit directs the loading of a halfword of data into the DB before a memory request is made. The transfer of data from the device is the same as described in the Memory Read mode, except that ENG1 is used to generate the Private Data Request control line (PDR0)(3H5) rather than PDA0. Data from the device is loaded into the MDR on the trailing edge of either Load Data Register High (LDRH0)(2R2) or Load Data Register Low (LDRL0)(2R2), depending on which eight bits are being loaded. In the Halfword Transfer mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (3H8) when the Buffer Active flip-flop is set (BACT1)(3H1), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0)(5J2). This prevents the reloading of the Data Buffer (DB) before the last halfword has been written into memory.

4.8 RACK0/TACK0 Contention Circuit

The Selector Channel directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus as well as devices on the private SELCH Bus. If the Selector Channel Attention flip-flop (4B4) is set, the SELCH captures the Receive Acknowledge signal (RACK0) (4B3), place its device address on the Data Lines and return Sync to the Processor, Attention Sync (ATSYN0)(4F4) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0)(4F2) or Transmit Acknowledge (TACK0)(4F3). Since devices on the private SELCH Bus have a higher interrupt priority than devices below the SELCH on the MPX Bus; if the Private Attention Test line is active (PATN0) (4B1), PTACK0 is generated rather than TACK0. Note that when MSC0 is high (3F4), PATN0 is disabled so that a device on the private SELCH Bus may not interrupt the Processor while the SELCH is active.

5. MAINTENANCE, TROUBLE SHOOTING, AND TEST

Before attempting any maintenance or testing, insure that the necessary back panel modifications and SELCH board option strapping have been made in accordance with the NS Selector Channel Installation Specification 02-232M01A20.

To insure a 2,000,000 Byte/second transfer rate in the Byte Transfer Mode, it is necessary to limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0), to 30 nanoseconds. In addition, the device must be ready for the next byte of data, Busy Status Bit reset, whenever a Status Request is made. Field testing of this device is contingent upon the user having appropriate software and hardware available with which to exercise the Selector Channel. There are no adjustments associated with this device. Do not install Terminator Boards 35-433 or 35-434 on the SELCH bus if a transfer rate of 2,000,000 Bytes/second is to be maintained in the Byte (8 Bit) Mode. The SELCH Bus should be contained on a single 15 inch chassis if no terminators are used.

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the SELCH. The source of each signal on Functional Schematic 02-232M01D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:151	Outputs of the Auxiliary Address Register	5F1-5F9
ACT0	Accept - Request for memory accepted by Processor	4H1
AD1	Address - Active when SELCH is addressed	2K7
ADRS0	Address control line from MPX-Bus	4B8
AG081:151	Address Gated Lines - Output of Address Strap	1E3 - 1E8
ATN0	Attention - Attention to Processor	4F1
ATSYN	Attention Sync - Generated by an Acknowledge Attention from Processor	4F4
BACT1	Buffer Active - Indicates that valid data is present in the DB	3H1
BSY	Busy - Indicates a data transfer is in progress	3F3
CDR0	Clear Data Register - Clears MDR prior to loading from MS000:150	4R2
CBSY0	Clear Busy - Terminates transfer when a match is detected	3M3
CL070	Control Line 7 - Control Line from MPX-Bus	4B6
CLG1	Control Line Gate - Gates Private Control Lines	1C2

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MNEMONIC	MEANING	SCHEMATIC LOCATION
CLUS0	Clear Load/Unload Sequencer - Clears Sequencer	3S2
CMD0	Command Control Line from MPX-Bus	4B8
CMG	Command Gated by AD1	2S7
CO0	Carry Out of the AAR - Prevents Memory 'Wrap-around'	5A1
D000:150	Data Lines from MPX-Bus	1A3 - 1A8 2A1 - 2A8
DA0	Data Available Control Line from MPX-Bus	4B7
DLG0	Data Line Gate - Gates Data Lines and Private Data Lines	1R2 - 1D3
DB001:151	Outputs of Data Buffer	6G2 - 6G9 6R2 - 6R9
DR0	Data Request Control Line from MPX-Bus	4B7
DRG0	Data Request Gated by AD1	2L5
DX	Data Transfer flip-flop	3F8
EBS1	End of Busy Set - Signals the start of a SELCH transfer	3J4
EDX1	End of Data Transfer - Signals the end of a device transfer	3J8
EMX1	End of Memory Transfer - Signals the end of a memory transfer	4R7
EN0	Enable from Memory Bus	4H2
ENG1	Engage - Gates either PDS0 or PDR0	3D8
ENMDR1	Enable Memory Data Register Read - Gates contents of MDR to MD000:150	4R6
ENMDW1	Enable Memory Data Register Write - Gates contents of DB to MD000:150	4R3
ENMS1	Enable Memory Strobe - Gates contents of MS000:150 to MDR	4R4
HW0	Halfword Control Line from MPX-Bus	1D2
INH0	Inhibit from Memory Bus	4H5
LARH0	Load Address Register High - Loads AAR and AR, Bits 00:07	2R2
LARL0	Load Address Register Low - Lards AAR and AR, Bits 08:15	2R2
LDB1	Load Data Buffer - Load contents of MDR to DB	3S2
LDRH0	Load Data Register High - Loads MDR Bits 00:07	3F8
LDRL0	Load Data Register Low - Loads MDR Bits 08:15	3H9
LFRH0	Load Final Address Register High - Loads FAR Bits 00:07	2S3
LFRL0	Load Final Address Register Low - Loads FAR Bits 08:15	2S3
MA000:140	Memory Address Lines to Memory Bus	5R1 - 5R8
MCH1	Match - Indicates a match between AAR and FAR	5J6

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MNEMONIC	MEANING	SCHEMATIC LOCATION
MD000:150	Memory Data Lines to Memory Bus	6G1 - 6G8 6R1 - 6R8
MS000:150	Memory Strobed Data Lines from Memory Bus	6A1 - 6A8 6H1 - 6H8
MSC0	Multiplexor SELCH Control flip-flop	3F4
PADRS0	Private Address Control Line to SELCH Bus	4F8
PATN0	Private Attention from SELCH Bus	4B1
PCL070	Private Control Line 7 to SELCH Bus	4R6
PCMD0	Private Command Control Line to SELCH Bus	4F8
PD000:150	Private Data Lines - SELCH Bus	2F1 - 2F8 1S3 - 1S9
PDA0	Private Data Available Control Line to SELCH Bus	3H5
PHW0	Private Halfword Control Line from SELCH Bus	1A1
PSR0	Private Status Request Control Line to SELCH Bus	3H6
PSYN0	Private Sync from SELCH Bus	4B5
PTACK0	Private Transmit Acknowledge to SELCH Bus	4F2
RACK0	Receive Acknowledge from MPX-Bus	4B5
RBA0	Reset Buffer Active - Resets Buffer Active flip-flop	3M2
REQ0	Request - Request for memory cycle to Memory Bus	4R5
SCLR0	System Clear - Initialize Signal	4H4
SGAD1	Set Gate - Sets Address flip-flop	2LR
SR0	Status Request Control line from MPX-Bus	4B6
SREQ0	Set Request - Initiates a request for memory	3S4
SSX0	Set Status Transfer - Sets the Status Request flip-flop	3S5
SX	Status Transfer - Status Request flip-flop	3F6
SYN0	Sync to MPX-Bus	2S5
TAC0	Transmit Accept - To lower priority DMAs	4R1
TACK0	Transmit Acknowledge - To lower priority devices on MPX Bus	4F3
TAAR0	Toggle Auxiliary Address Register - Increments AAR	3M1
TAR0	Toggle Address Register - Increments AR	4S7
UAAH0	Unload Auxiliary Address Register High - Unloads AAR Bits 00:07	2R4
UAARL0	Unload Auxiliary Address Register Low - Unloads AAR Bits 08:15	2R4
WT	Write flip-flop	3F5
WRT0A	Write to Memory Bus, when selected	4R3

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MEMORY PROTECT

MODEL 70 MEMORY PROTECT INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-236 Memory Protect Module in a Model 70 Processor System. The module assembly consists of one 35-396 7" board and one 17-169 cable. The 35-396 7" board must be strapped to a blank 7" board or an active 7" board (e.g. Universal Clock Module) by an INTERDATA 16-398 Half Board Kit, so that it may be installed in a chassis designed for standard 15" boards. The Memory Protect Module may be installed in either the right or left half position, depending on the system configuration. See Figure 1.

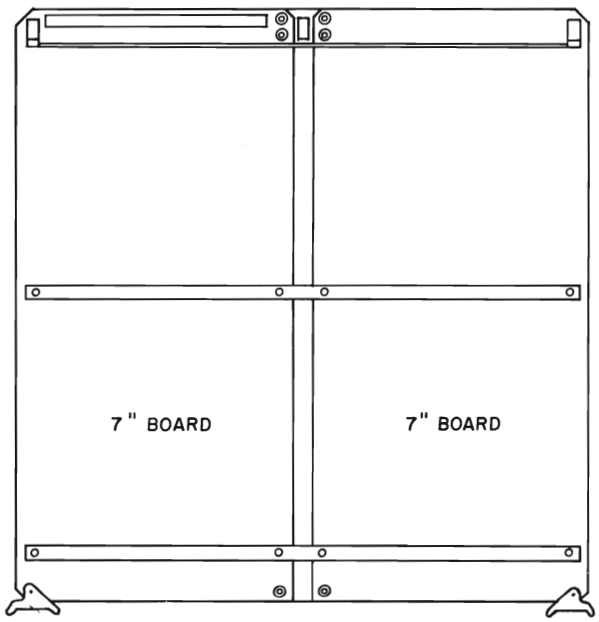


Figure 1. 7" Board Assembly

2. UNPACKING

When the Memory Protect Module is shipped with a system, it is installed at the factory so there is no special unpacking procedure. If the module assembly is purchased separately, it should be inspected for damage prior to installation.

3. LOCATION

The 35-396 Memory Protect Module 7" board, once assembled using a half board kit, may be installed in any available I/O slot of a standard 15" chassis which is located no more than one chassis from the Processor.

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NOTE

Normally it is required that the Memory Protect Module be installed as the highest priority device controller (with respect to interrupts) on the Multiplexor Bus to insure proper recognition and response to Memory Protect violation interrupts that may occur in the system. This is accomplished by installing the Memory Protect Module in the first available I/O slot with respect to the daisy chain priority line, and rerouting the RACK0/TACK0 line which is ordinarily connected first to the built-in Teletypewriter controller. See Section 4.

4. BACK PANEL WIRING

To insure that the Memory Protect has the highest priority on the Multiplexor Bus, the RACK0/TACK0 line on the Processor chassis back panel must be rerouted. Refer to Figure 2 during the following rerouting procedure.

1. Remove the RACK0/TACK0 jumper from the slot occupied by the Memory Protect Module. The jumper is located between Terminals 122 and 222 on the selected slot.

2. Break the daisy chain line from the next higher priority device controller and to the next lower priority device controller, at Terminals 122-1 and 222-1 on the Memory Protect Module's selected slot. Connect the TACK0 Terminal 222-1 from the next higher priority device to the RACK0 Terminal 122-1 on the next lower priority device controller on the Multiplexor Bus. This removes the Memory Protect Module from the daisy chain priority sequence, and re-establishes the daisy chain to lower priority device controllers.

3. Break the connection between Acknowledge Interrupt (ACKA00) Terminal 236-0 and Teletypewriter Receive Acknowledge (RACK0) Terminal 234-1 on the I/O Board, Slot 5. This disconnects the Teletypewriter device controller from the Acknowledge Interrupt (ACKA00) line.

4. Connect a jumper between Memory Protect Module RACK0 Terminal 122-1 and I/O Board ACKA00 Terminal 236-0. This connects the Memory Protect Module as the first device controller in the RACK0/TACK0 line.

5. Connect a jumper between Memory Protect Module TACK0 Terminal 222-1 and I/O Board Teletypewriter RACK0 Terminal 234-1. This connects the Teletypewriter as the second device controller in the RACK0/TACK0 line.

The Memory Protect Module is now the highest priority device controller in the daisy chain. The built-in Teletypewriter device controller is second in priority and the remaining device controllers are as before in their required sequence.

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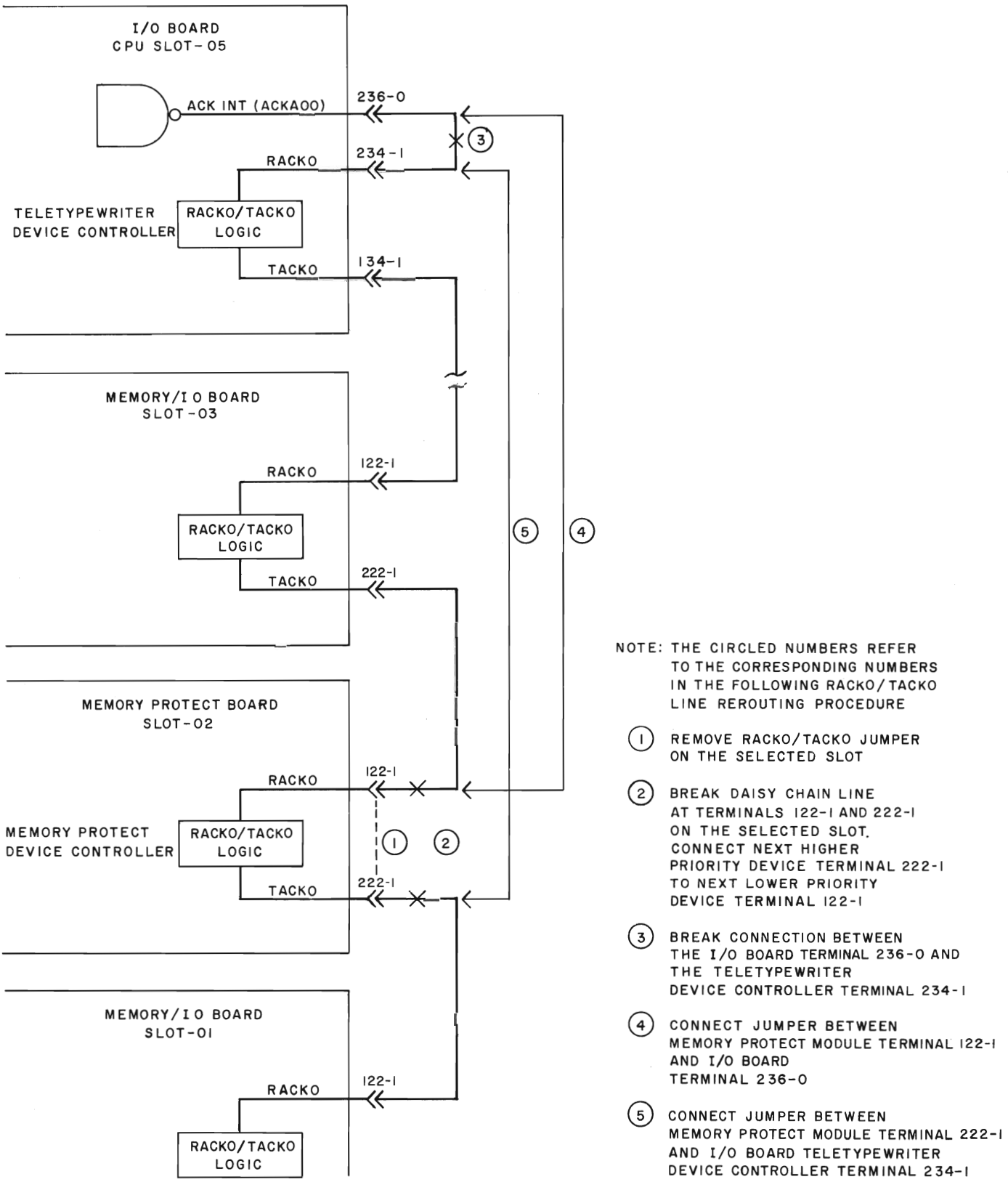


Figure 2. RACK0/TACK0 Rerouting with Memory Protect Module

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5. CABLE CONNECTION

Install the 17-169 cable between the 35-396 Memory Protect board and the 35-387 Memory Control board. See Figure 3. The Memory Control board is located in Slot 4 of the Central Processor Unit (CPU) chassis.

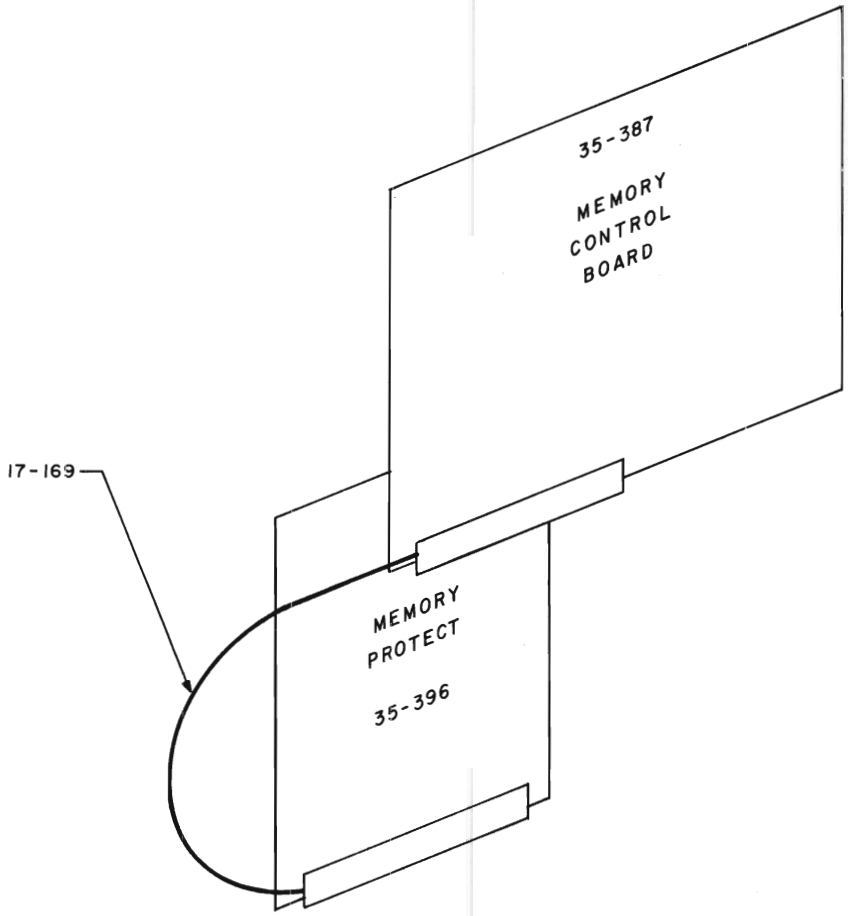


Figure 3. Cable Connection

6. STRAP OPTIONS

6.1 Address Strapping

The preferred address of the Memory Protect Controller is X'AE'. The module is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-236D08, Sheet 1.

6.2 Block Size Option

The Memory Protect Controller is strapped for 1,024 Byte blocks at the factory. To change the block size, refer to the Block Size Table on Sheet 2 of Functional Schematic 02-236D08.

NOTE

The alpha-numeric designations referred to on the functional schematic, indicate similar designations on the apparatus side of the printed circuit board.

7. INSTALLATION CHECKS

To insure proper operation of the Model 70 Memory Protect, Test Program 06-135 should be executed in accordance with its test program description.

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MODEL 70 MEMORY PROTECT MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-236 Model 70 Memory Protect provides a means of allocating selected blocks of memory to be protected. The Memory Protect Controller (MPC) converts a Write operation to any location in a protected block to a Read operation, notifies the Processor via an interrupt, and sets a status bit in the controller. The memory may be partitioned into a maximum of 64 blocks with individual protect control for each block. An overall protection override provides a means of loading any area in memory.

The Model 70 Memory Protect consists of one Memory Control mother-board and one cable. The cable interconnects the Memory Protect Controller with the Memory Control board of the Central Processor Unit (CPU). Refer to the Installation Specification, 02-236A20, for necessary installation information.

2. SCOPE

This specification describes the functional operation of the Memory Protect Controller and its associated circuits in the Processor. This specification contains a block diagram analysis, a functional diagram analysis, timing information, and a mnemonic list for the Memory Protect Controller. Strapping information for block size selection is found on Sheet 2 of Functional Schematic 02-236D08.

3. BLOCK DIAGRAM ANALYSIS

Refer to the block diagram of the Memory Protect Controller (MPC) on Sheet 3 of Functional Schematic 02-236D08.

Prior to installation, the Memory Protect should be strapped for the desired block size. The following block sizes may be selected; 512 bytes, 1,024 bytes, or 2,048 bytes. Refer to the table on Sheet 2 of Functional Schematics 02-236D08 for strapping information.

Having selected the desired block size, the MPC is setup by the Processor via the Multiplexor Channel Bus. This set-up includes the loading of the 64-bit Mask Register with the block or blocks to be protected, either selecting or over-riding the protect function, and either arming or disarming the I/O interrupts at the controller. The loading of the 64 bit Mask Register is accomplished by steering up to eight Data Availables (DAs), by the Control Circuit, to the Mask Register. The most significant bit of the first DA corresponds to block one, the next less significant bit of the first DA corresponds to block two, etc.

The Memory Protect Controller constantly monitors the true outputs from the Memory Address Register in the Processor (MA001A:MA061A) and generates Protected Address (PRTAD1) whenever a protected memory address, as defined by the 64-bit Mask Register, is accessed. Meanwhile, if protect is enabled at the Processor, and a Write operation is attempted, Protect (PRTECT0) is generated on the Memory Control board and sent to the MPC. PRTECT0 is ANDed with Protected Address (PRTAD1) and Override Protect (ORP1), by the MPC Control Circuit, to generate CWR0. CWR0 is in turn sent to the Read flip-flop on the Memory Control board. It sets the Read flip-flop which disables the Write attempt and causes a normal Read operation to be performed.

CWR0 also sets a status bit in the controller and generates an interrupt, when enabled, to indicate to the program that an attempt was made to Write to a protected area in memory.

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4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

To understand INTERDATA functional schematics, it must be noted that the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 and the last character 0 means that when D080 is active, the line is at a logical Zero level.

This section relates to Functional Schematic 02-236D08.

4.2 Multiplexor Bus Communication

When the Memory Protect Controller is addressed by the Processor, all highs are presented to the inputs of the NAND gate at 1G3. The output from this gate is inverted and applied to the J input of the Address flip-flop (AD)(1L3) while the non-inverted signal is applied to the K input of the Address flip-flop. The trailing edge of ADRS0 toggles the Address flip-flop set producing AD1.

The Processor is notified that the address was recognized by a device controller by activating SYN0 (1H7). SYN0 is generated by ADSYN0 (1D6), which is the ANDed output of ADRS1 and the recognition of the address. SYN0 is generated for each of the other control signals (CMD, DR, DA, and SR) by gating them with an active AD1 and applying the gated output to the NAND gate at 1E7.

If an interrupt is generated by this controller, the Attention flip-flop (1J9) is set, and Attention (ATN0) is sent to the Processor. When the Processor acknowledges this interrupt, Receive Acknowledge (RACK0)(1L8) becomes active. RACK0 is inverted and applied to the contention circuit (1R5) which generates either Attention Sync (ATSYN0), when ATN1 is active or Transmit Acknowledge (TACK0), when ATN1 is inactive. ATSYN1 (1H8) gates the address onto Data Lines 8:15, and its falling edge resets both the ATN and the Write Attempt (WATT) flip-flops. Interrupts may be enabled and disabled, via program control, by the setting or clearing of the ARM/DISARM flip-flop (1M7). Initialize (SCLR0 active) or an Output Command with Bit-8 active and Bit-9 inactive, sets this flip-flop to the Disarm state, and an Output Command with Bit-8 inactive and Bit-9 active, places it in the Arm state. In the Disarm state, a low is presented to the direct clear input of the ATN flip-flop, preventing it from becoming set.

4.3 Status and Command

The Status and Command Byte data is shown in Table 1.

TABLE 1. MEMORY PROTECT STATUS AND COMMAND BYTE DATA.

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE			PON	PWF		EX		
COMMAND BYTE	DISARM	ARM	PON	POFF				

PON	Indicates that protect is enabled.
PWF	Indicates that an attempt was made to Write into a protected memory area. This bit is reset by an Output Command, or an Acknowledge Interrupt instruction.
EX	Examine is set when PWF is set.
DISARM	Disables interrupts. They will not be queued.
ARM	Enables interrupts.
PON	Enables the protect function on the controller.
POFF	Disables the protect function on the controller.

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4.4 Load Mask Sequencer

The load mask sequencer steers up to eight Data Availables (DAs) to load the 64-bit Mask Register with the desired protect pattern. The four-bit counter (2L7) is initialized by CL1 which is the OR output from SCLR0 and CMG0 (1H9). When initialized, all outputs from the counter are at a logical Zero level. This causes the first DA to activate BADG20 which enables the loading of the two 4 x 4 register stacks located at 2G2 and 2G6. Since BAD01 and BAD11 are both low, the first DA loads Word '0' into the two registers. The trailing edge of DAG0 increments the counter, allowing the next DA to load Word '1' into the same two registers (BAD01 active). For the last four DA outputs, output C from the counter is high causing these DAs to activate BADG30 which enables the loading of the remaining two register stacks. If more than eight DAs are issued, wrap-around occurs (i.e., the ninth DA will once again load Word '0' into the first pair of registers).

4.5 Protect Pattern Recognition

The Memory Protect Controller constantly monitors the true outputs from the Memory Address Register (MAR) in the Processor (MA001A:MA061A). The MAR outputs are strapped in accordance with the table on Sheet 2 of Functional Schematic 02-236D08 for the desired block size, to generate Memory Address Lines MA01 to MA051 (2C3-267). The four most significant signals, MA01:MA031, are decoded by the four-to-four line decoder (2D2-2D9) to enable one of the four register stacks and to select one of the four-bit words of that register for a particular group of memory addresses.

Each of the four outputs from the four-bit register stacks is OR tied with the corresponding output from the other register stacks (i.e., the 1 output from register 35 is OR tied with the 1 output from register stacks 34, 33, and 32), but only the selected stack may be active. The two least significant memory address bits monitored by the Memory Protect Module for any given block size, MA41 and MA51, are used to select one of the four outputs of the selected register stack (2L3). This selection is accomplished by the four-to-one line multiplexor (2M8). If the selected data input to the multiplexor is high, the Protected Address signal (PRTAD1) is active.

Each time a Memory Write function is decoded by the Processor with Program Status Word (PSW) Bit-7 set, PRTECT0 is generated unless the Write function is a privileged write. The one-shot at 2K5 generates a pulse approximately 60 nanoseconds in duration on the trailing edge of PRTECT0. This pulse, when the protect function is enabled in the module, ORP1 and PRTAD1 active, generates CWR0 and ASATN0. These signals (CWR0 and ASATN0) cause the Write attempt by the Processor to be converted into a Read operation, and the Attention flip-flop in the Memory Protect Module to be set respectively.

5. TIMING

Refer to Figure 1. Worst case delays are indicated.

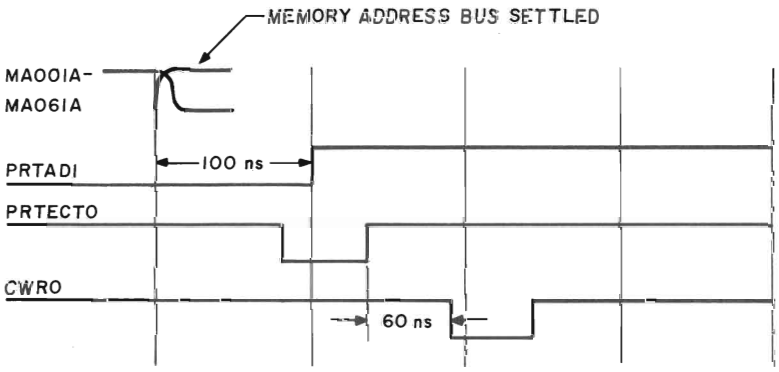


Figure 1. Memory Protect Timing

6. MAINTENANCE AND TESTS

The Memory Protect Module requires no adjustments. Before attempting any maintenance or testing, insure that the cable and the controller are installed properly. Refer to the Installation Specification, 02-236A20, for necessary installation information.

To test the Memory Protect Module, run the Memory Protect Test 06-123F04 in accordance with its test program description.

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7. MNEMONICS

The following list provides a brief description of each mnemonic in the Memory Protect Module. The source of each signal on Schematic Drawing 02-236D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AD	Address flip-flop	1M3
ADRS0	Address control line from CPU	1J4
ADSYN0	Address Sync - Causes Sync to be returned on an ADRS0	1M4
ASATN0	Set Attention - Sets the Attention flip-flop on a protect violation	2R4
ATN	Attention flip-flop	1J8
ATSYN0	Attention Sync - Causes Sync to be returned on an Acknowledge Interrupt	1S5
BAD01-11	Block Address - Selects the indicated word in the 64-bit Mask Register	2M6
BADG20-30	Block Address Gated - Enables the indicated pair of registers in the 64-bit Mask Register	2S6
CL1	Clear - Initialize the load mask sequencer on a Command or System Clear	1K9
CMD0	Command control line from the CPU	1A6
CWR0	Convert Write to Read - To CPU to change the Write operation into a Read operation	2S4
D080:D150	Data Lines from the CPU	1A1 - 1A5
DA0	Data Available control line from the CPU	1A7
DR0	Data Request control line from the CPU	1A7
MA001A:061A	Ungated Memory Address from the Memory Address Register	2A3 - 2A9
MA01:051	Memory Address lines selected by the Block Size strapping	2C4 - 2C7
ORP1	Override Protect - Overrides the protect function of the Memory Protect Module	1L1
PRTAD1	Protected Address - Indicates that the Memory Address Register in the CPU contains a protected address when active.	2N3
PRTECT0	Protect - Generated by the Processor when a non-privileged Write attempt is made	2J5
RACK0	Receive Acknowledge - Acknowledge from the lower priority device in the RACK0/TACK0 daisy chain	1L8
SCLR0	System Clear from the CPU	1A8
SR0	Status Request control line from the CPU	1A8
SYN0	Sync - Composite Sync signal to the CPU	1G7
TACK0	Transmit Acknowledge - Acknowledge to the higher priority device in the RACK0/TACK0 daisy chain	1S6

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02-236A22
March 1972

MODEL 70 MEMORY PROTECT PROGRAMMING SPECIFICATION

1. INTRODUCTION

The 02-236 Model 70 Memory Protect provides a means of allocating selected blocks of memory to be protected from user writing. The Memory Protect Controller (MPC) converts a Write operation to any location in a protected block to a Read operation, notifies the Processor via an interrupt, and sets a status bit in the controller. The memory may be partitioned into a maximum of 64 blocks with individual protect control for each block. Block sizes of 512 bytes, 1,024 bytes, or 2,048 bytes may be selected by strap options on the controller. Refer to Installation Specification 02-236A20, for block size strapping information. An overall protection override provides a means of disabling the protect function at the controller. Note that the protect function is enabled at the Processor only when Bit-7 of the current Program Status Word is set. When Bit-7 is reset, all Writes are treated the same as Privileged Writes (i.e. protect disabled).

2. CONFIGURATION

The Model 70 Memory Protect consists of one Memory Control mother-board and one cable. The cable interconnects the Memory Protect Controller with the Memory Control Board in the Central Processor Unit (CPU). The priority of the Memory Protect Controller on the Multiplexor Bus is determined by its installation in the systems chassis. Refer to 02-236A20 for installation information.

> NOTE
>
> It is imperative that the Memory Protect Controller have the highest priority on the Multiplexor Bus, to avoid ambiguity in identifying the source of a protect violation when executing interrupt routines with I/O interrupts enabled.

3. OPERATING PROCEDURES

The Model 70 Memory Protect is controlled by programmed I/O sequences using the Multiplexor Bus. See Sections 5 and 6.

4. DATA FORMAT

Refer to Appendix 1 for the definition of the Load Mask Bytes.

5. PROGRAMMING INSTRUCTIONS

The Output Command instruction (OC or OCR) causes a command byte, as defined in Table 1, to be sent to the controller. Any command causes all status except Protect On (PON) to be reset, and the Load Mask Sequencer to be initialized. The Sense Status instruction (SS or SSR) is used to read the status byte, as defined in Table 1, from the Memory Protect Controller. The status byte reflects the operational state of the controller. The least significant four bits (4:7) of the status byte are copied into the Condition Code of the current Program Status Word so they can be tested directly by the use of Branch instructions.

The Write Data (WD or WDR), Write Halfword (WH or WHR), or the Write Block (WB or WBR) instructions may be used to load the protect pattern into the controller.

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TABLE 1. MEMORY PROTECT STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE			PON	PWF		EX		
COMMAND BYTE	DISARM	ARM	PON	POFF				

STATUS

PON	Indicates that protect is enabled.
PWF	Indicates that an attempt was made to Write into a protected memory area. This bit is reset by an Output Command, or an Acknowledge Interrupt instruction.
EX	Examine is set when PWF is set.

COMMAND

DISARM	Disables interrupts. They will not be queued.
ARM	Enables interrupts.
PON	Enables the protect function at the controller.
POFF	Disables the protect function at the controller.

If an interrupt is pending, the Acknowledge Interrupt instruction (AI or AIR) clears the interrupt and causes the interrupting device address and status to be read into the Processor. Executing an Acknowledge Interrupt instruction when no interrupt is pending, results in a device address of zero and a status of X'04'.

6. PROGRAMMING SEQUENCE

The setting up of the Memory Protect Controller consists of loading the desired protect pattern into the controller, enabling the protect function, and either Arming or Disarming the interrupts. Any Output Command initializes the load sequencer in the controller so that the first byte to the protect module, following the Output Command, will load the Mask Register, Blocks 0:7. Refer to Appendix 1 for the correspondence between the load mask bytes, block size, and memory addresses protected. An active bit in the load mask byte masks (protects) the selected addresses. If more than eight bytes are used to load the Mask Register, wrap-around occurs (i.e. the ninth byte once again loads blocks 0:7). For the 2K byte block size option only four bytes are required to protect maximum memory, 64K. If more than four bytes are issued, bytes 4:7 load the Mask Register but are not used. The Protect Enable Command and Arm or Disarm Command may be issued simultaneously.

After setting up the Protect Controller, Bit-7 of the Program Status Word must be set to enable the protect function at the Processor.

7. INTERRUPTS

An interrupt can be used to signal the Processor that an attempt was made to Write into a protected area in memory. In the Arm state, interrupts are armed and enabled. In the Disarm state, interrupts are neither enabled not queued.

When an interrupt is acknowledged by an Acknowledge Interrupt instruction (AI or AIR) the interrupt is cleared and all status bits except PON are reset. The normal status returned by an Acknowledge Interrupt is X'20'.

8. INITIALIZATION

During power up, power down, or whenever the Initialize (INT) switch on the Display Panel is depressed, the Memory Protect Controller is placed in the Disarm state with all status conditions reset. The Load Mask Sequencer is initialized and the protect function is disabled at the controller.

9. DEVICE NUMBER

The Model 70 Memory Protect is normally assigned device address X'AE'. This address can be changed by the modification of straps on the controller. Refer to the Installation Specification 02-236A20, for details about the wiring alteration.

10. SAMPLE PROGRAM(S)

Not applicable to the Model 70 Memory Protect.

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APPENDIX 1
TABLE OF MEMORY ADDRESSES VS. BLOCKS

BLOCK	LOAD MASK DATA		MEMORY ADDRESSES (HEX)		
	BYTE	BIT	.5K BYTE	1K BYTE	2K BYTE
1	0	0	0000-01FF	0000-03FF	0000-07FF
2	0	1	0200-03FF	0400-07FF	0800-0FFF
3	0	2	0400-05FF	0800-0BFF	1000-17FF
4	0	3	0600-07FF	0C00-0FFF	1800-1FFF
5	0	4	0800-09FF	1000-13FF	2000-27FF
6	0	5	0A00-0BFF	1400-17FF	2800-2FFF
7	0	6	0C00-0DFF	1800-1BFF	3000-37FF
8	0	7	0E00-0FFF	1C00-1FFF	3800-3FFF
9	1	0	1000-11FF	2000-23FF	4000-47FF
10	1	1	1200-13FF	2400-27FF	4800-4FFF
11	1	2	1400-15FF	2800-2BFF	5000-57FF
12	1	3	1600-17FF	2C00-2FFF	5800-5FFF
13	1	4	1800-19FF	3000-33FF	6000-67FF
14	1	5	1A00-1BFF	3400-37FF	6800-6FFF
15	1	6	1C00-1DFF	3800-3BFF	7000-77FF
16	1	7	1E00-1FFF	3C00-3FFF	7800-7FFF
17	2	0	2000-21FF	4000-43FF	8000-87FF
18	2	1	2200-23FF	4400-47FF	8800-8FFF
19	2	2	2400-25FF	4800-4BFF	9000-97FF
20	2	3	2600-27FF	4C00-4FFF	9800-9FFF
21	2	4	2800-29FF	5000-53FF	A000-A7FF
22	2	5	2A00-2BFF	5400-57FF	A800-AFFF
23	2	6	2C00-2DFF	5800-5BFF	B000-B7FF
24	2	7	2E00-2FFF	5C00-5FFF	B800-BFFF
25	3	0	3000-31FF	6000-63FF	C000-C7FF
26	3	1	3200-33FF	6400-67FF	C800-CFFF
27	3	2	3400-35FF	6800-6BFF	D000-D7FF
28	3	3	3600-37FF	6C00-6FFF	D800-DFFF
29	3	4	3800-39FF	7000-73FF	E000-E7FF
30	3	5	3A00-3BFF	7400-77FF	E800-EFFF
31	3	6	3C00-3DFF	7800-7BFF	F000-F7FF
32	3	7	3E00-3FFF	7C00-7FFF	F800-FFFF
33	4	0	*	8000-83FF	
34	4	1		8400-87FF	
35	4	2		8800-8BFF	
36	4	3		8C00-8FFF	
37	4	4		9000-93FF	
38	4	5		9400-97FF	
39	4	6		9800-9BFF	
40	4	7		9C00-9FFF	N/A
41	5	0		A000-A3FF	
42	5	1		A400-A7FF	
43	5	2		A800-ABFF	
44	5	3		AC00-AFFF	
45	5	4		B000-B3FF	
46	5	5		B400-B7FF	
47	5	6		B800-BBFF	
48	5	7		BC00-BFFF	

* If more than 32K Bytes of memory exists, and the 512 Byte Block option is used, the pattern defined for the first 32K repeats itself for the second 32K.

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APPENDIX 1
TABLE OF MEMORY ADDRESSES VS. BLOCKS (Continued)

BLOCK	LOAD MASK DATA		MEMORY ADDRESSES (HEX)		
	BYTE	BIT	.5K BYTE	1K BYTE	2K BYTE
49	6	0		C000-C3FF	N/A
50	6	1		C400-C7FF	
51	6	2		C800-CBFF	
52	6	3		CC00-CFFF	
53	6	4		D000-D3FF	
54	6	5		D400-D7FF	
55	6	6		D800-DBFF	
56	6	7		DC00-DFFF	
57	7	0		E000-E3FF	
58	7	1		E400-E7FF	
59	7	2		E800-EBFF	
60	7	3		EC00-EFFF	
61	7	4		F000-F3FF	
62	7	5		F400-F7FF	
63	7	6		F800-FBFF	
64	7	7		FC00-FFFF	

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DRAWINGS

INTERDATA®

BACK PANEL PIN INDEX

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT.	I/O
ACKA00	—	—	—	20N6
ADRS0	—	—	—	20L6
AMOD1	9A1	10G9	—	—
ARST1	—	—	—	18J1
ATN0	—	—	—	18N1
B000	—	11S2	29K4	—
B010	—	11S2	29L4	—
B020	—	11S2	29M4	—
B030	—	11S3	29N4	—
B040	—	11S3	29A9	—
B050	—	11S4	29C9	—
B060	—	11S4	29D8	—
B070	—	11S4	29E8	—
B080	—	11S6	29F8	20B6
B090	—	11S6	29G8	20C6
B100	—	11S6	29H8	20D6
B110	—	11S7	29J8	20E6
B120	—	11S8	29K8	20F6
B130	4F5	11S8	29L8	20F6
B140	—	11S8	29M8	20G6
B150	—	11S9	29N8	20H6
BANK0	8H4	12M9	—	18K5
CATN0	—	—	—	18R1
CC121	—	—	29K4	17B9
CC131	—	—	29L4	17D9
CC141	—	—	29M4	17E9
CC151	—	—	29N4	17G9
CEMT0	—	13F7	27C9	—
CL070	—	—	—	19D6
CLKOFF0	—	—	—	19E5
CLR0	9N4	12K5	27D1	17R1
CLRIR0	9A9	—	28A1	—
CMD0	—	—	—	20M6
CS1	8M9	12A6	26A1	—
CSV1	—	14D9	—	17E1
CTF1	—	14S9	—	17J1
CTONE0	—	13K6	27C9	18E6
D000	—	16B6	—	—
D010	—	16C6	—	—
D020	—	16C6	—	—
D030	—	16D6	—	—
D040	—	16E6	—	—
D050	—	16F6	—	—
D060	—	1666	—	—
D070	—	16H6	—	—
D080	—	—	—	20B6
D090	—	—	—	20C6
D100	—	—	—	20D6
D110	—	—	—	20E6
D120	—	—	—	20F6
D130	—	—	—	20G6
D140	—	—	—	20H6
D150	—	—	—	20H6
DI	8K4	—	—	19K1
DA0	—	—	—	20M6
DCAK0	—	—	—	20L6
DCL0	8L4	10H1	25C1	19M9
DCO	—	—	—	18R1
DDC1	8B9	13H1	30R9	—
DECTRO	—	13F9	27C1	18E9
DISR0	6A7	—	—	—
DRD0	—	—	—	18M1
DR0	—	—	—	20N6
DST0	4A5	—	—	19L5
DTEST0	9E1	—	—	18N9
EN0	—	—	30M9	—
ER0	—	—	30E9	—
EXTCLK0	—	—	—	19E6
FAST0	—	—	—	18B5
FLI21	—	15A2	—	17C9
FMDBY1	4K1	—	30S1	—
FMDUA1	9D1	—	30K1	—
FPMBY0	9D1	—	30S9	—
FRCLOCO	9J4	10F1	—	—
FRNS1	—	14S7	—	17R5
GA000	—	12A5	—	17G1
GB000	—	14A4	—	17G1
GDEST1	8H4	10J1	—	—
GTP20	9F1	—	—	—
HIDUA0	8A1	—	—	—
HDEST0	8D9	15L1	—	—
HW01	9K1	—	—	—
GIP10	8K9	—	—	—
DT21	9N5	13L6	—	—

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
INH0	—	—	30C9	—
INHINC0	5R2	—	—	—
INTA0	4N1	—	—	17S9
IR001	4A5	—	28B5	—
IR011	4B5	—	28D5	—
IR021	4B5	—	28F5	—
IR031	4B5	—	28G5	—
IR041	4B5	—	28J5	—
IR051	4C5	—	28L5	—
IR061	4C5	—	28M5	—
IR071	4C5	—	28R5	—
IR080	—	10L1	28B9	—
IR090	—	10M1	28D9	—
IR100	—	10E4	28E9	—
IR110	—	10R4	28G9	—
IR120	—	10L1	28J9	—
IR130	—	10M1	28K9	—
IR140	—	10F4	28M9	—
IR150	—	10S4	28R9	—
JACC0	9L4	—	—	17C5
KILDSTO	4N5	13N9	—	19M5
KSKIP0	8F9	—	—	18J5
LAR1	8F9	12A1	—	—
LARYS0	9C4	10B1	—	—
LCC0	9M4	—	—	17C5
LDI00	8S4	—	—	20L1
LDI01	—	16B6	—	20K6
LDCTR0	8C9	—	27B1	—
LFLR0	8D9	—	—	17S1
LINE1	4C5	—	—	20R1
LIR0	8D9	—	28S1	—
LMAR0	8G9	—	25B1	—
LMDR1	4J1	—	26B1	—
LOAD1	6N4	12B6	—	—
LPSW1	8H9	—	29C1	17S1
LRAH0	5K1	—	—	18C9
LRALO	5R2	—	—	18K9
LRO	—	—	30E9	—
LSRLO	8D9	15N1	—	—
MA000	—	—	25A9	—
MA001	—	—	25A9	—
MA010	—	—	25B9	—
MA011	—	—	25B9	—
MA020	—	—	25C9	—
MA021	—	—	25C9	—
MA030	—	—	25D9	—
MA040	—	—	25E9	—
MA050	—	—	25F9	—
MA060	—	—	25F9	—
MA070	—	—	25H9	—
MA080	—	—	25H9	—
MA090	—	—	25J9	—
MA100	—	—	25K9	—
MA110	—	—	25L9	—
MA120	—	—	25M9	—
MA130	—	—	25N9	—
MA140	—	—	25R9	—
MAR150	9S5	—	25S9	—
MCLR1	—	—	30A1	—
MD000	—	—	26C5	—
MD010	—	—	26E5	—
MD020	—	—	26F5	—
MD030	—	—	26H5	—
MD040	—	—	26K5	—
MD050	—	—	26L5	—
MD060	—	—	26N5	—
MD070	—	—	26S5	—
MD080	—	—	26D9	—
MD090	—	—	26E9	—
MD100	—	—	26F9	—
MD110	—	—	26H9	—
MD120	—	—	26K9	—
MD130	—	—	26L9	—
MD140	—	—	26N9	—
MD150	—	—	26S9	—
MD160	—	—	27K4	—
MS000	—	—	26D1	—
MS010	—	—	26E1	—
MS020	—	—	26G1	—
MS030	—	—	26J1	—
JOE 1	9G5	—	27L9	—

MNEM	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
MS040	—	—	26K1	—
MS050	—	—	26M1	—
MS060	—	—	26R1	—
MS070	—	—	26S1	—
MS080	—	—	26D5	—
MS090	—	—	26E5	—
MS100	—	—	26G5	—
MS110	—	—	26J5	—
MS120	—	—	26K5	—
MS130	—	—	26M5	—
MS140	—	—	26N5	—
MS150	—	—	26S5	—
MS160	—	—	27J1	—
MSK1	—	—	29R8	18L1
NOMEM0	8A9	—	30R9	—
OP1	4L9	—	—	18L1
P00	5K4	—	30S1	—
P21	9F4	—	—	18N6
PARO	—	—	27J5	—
PC00	9E4	—	—	17M6
PC10	9F4	—	—	—
PFF1	—	—	27H9	17L6
PSW011	—	—	23F3	18K1
PSW021	—	—	29M1	17K6
PSW041	—	—	23B4	18B5
PSW071	—	—	29E4	—
RACK0	—	—	—	24A1
RAH040	5C4	—	—	—
RAH050	5E4	—	—	—
RAH060	5F4	—	—	—
RAH070	5G4	—	—	—
RAL080	5A9	—	—	—
RAL090	5B9	—	—	—
RAL100	5C9	—	—	—
RAL110	5D9	—	—	—
RAL120	5E9	—	—	—
RAL130	5F9	—	—	—
RAL140	5G9	—	—	—
RAL150	5H9	—	—	—
RCL0	5K1	—	—	19L9
RD000	8A4	10A1	—	17M1
RD001	8B4	13M1	—	17B1
RD010	8B4	10A1	—	17M1
RD011	8B4	13M1	—	17B1
RD020	8C4	13N1	—	—
RD021	8C4	13N1	—	17M1
RD030	8D4	10A1	—	17N1
RD031	8D4	13N1	—	18C1
RD040	8E4	—	30S9	18D6
RD041	8E4	10J1	—	18L1
RD050	8F4	—	30S9	18D6
RD051	8F4	10J1	—	18K1
RD060	8G4	10G1	—	18D6
RD061	8G4	13N1	—	18S1
RD070	8H4	10G1	—	18D6
RD071	8H4	13R1	—	18J1
RD080	8H4	10C1	—	18B1
RD081	8J4	10A1	—	18F1
RD090	8K4	10C1	29D4	18B1
RD091	8K4	10B1	—	18B1
RD100	8K4	10B1	—	18B1
RD101	8L4	10B1	—	18C1
RD110	8L4	10F1	29C4	18E1
RD111	8L4	10B1	—	18G1
RD120	8M4	—	—	—
RD121	8M4	12B6	—	18M1
RD130	8N4	—	—	—
RD131	8N4	12C6	—	18N1
RD140	8R4	—	—	20N1
RD141	8R4	15A2	—	18M1
RD150	8S4	—	—	20N1
RD151	8S4	13G1	—	18L1
RDSTB0	8A1	—	—	19L9
REQ0	—	—	30L1	—
S000	—	11S3	28B1	17H1
S001	—	12B1	—	17L1
S010	—	11S5	26D1	—
S011	—	12B1	—	—
S020	—	11S3	26F1	—
S021	—	12C1	—	—
READ1	—	—	27R9	—

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
S030	—	11S3	26H1	—
S031	—	12D1	—	—
S040	—	11S5	26J1	—
S041	—	12E1	—	—
S050	—	11S5	26L1	—
S051	—	12F1	—	—
S060	—	11S5	26N1	—
S061	—	12G1	—	—
S070	—	11S5	26R1	—
S071	—	12H1	—	—
S080	—	11S7	26C5	—
S081	5A5	12J1	—	20B1
S090	—	11S7	26D5	—
S091	5B5	12K1	—	20C1
S100	—	11S7	26F5	—
S101	5C5	12K1	—	20D1
S110	—	11S7	28G5	—
S111	5D5	12L1	—	20E1
S120	—	11S9	28J5	—
S121	5D1	12M1	—	20F1
S130	—	11S9	28K5	—
S131	5E1	12N1	—	20G1
S140	—	11S9	28M5	—
S141	5F1	12R1	—	20H1
S150	—	11S9	28R5	—
S151	5H1	12S1	—	20J1
SCL0	—	13G1	27D1	19J9
SCLR0	—	—	—	19N1
SCLRIA	5C1	12J5	30J9	19R1
SDUAD0	—	—	30K1	—
SHL1	8N9	13C5	—	—
SHOT1	—	13C9	—	17C1
SHR1	8N9	13B5	—	—
SKIP0	9C1	—	—	18J9
SNGL0	—	—	—	18R1
SRD001	8A1	—	—	—
SRD011	8B1	—	—	—
SRD021	8C1	—	—	—
SRD031	8D1	—	—	—
SRD041	8E1	—	—	—
SRD051	8F1	—	—	—
SRD061	8G1	—	—	—
SRD071	8H1	—	—	—
SRD081	8J1	—	—	—
SRD091	8K1	—	—	—
SRD101	8K1	—	—	—
SRD111	8L1	—	—	—
SRD121	8M1	—	—	—
SRD131	8N1	—	—	—
SRD141	8R1	—	—	—
SRD151	8S1	—	—	—
SRO	—	—	—	20R6
SSKIP0	9B9	—	—	18K6
SSMEM1	—	—	30J1	—
STFL0	8R9	—	—	17F1
STF0	8R9	—	—	17N1
STOP0	5B4	—	—	19L5
STFA0	4J5	—	—	19J5
STPC0	—	13R9	—	19L5
SUB1	—	13L4	—	17E1
SVAC0	8S9	13B4	—	17D1
SV0	4F5	—	—	17H1
SYSC0	8S9	13A4	—	17E1
SWTAL0	8L9	—	—	—
SYN0	4E1	—	—	23H7
SYSCL1	9A5	10H1	—	19G5
T21	5N5	—	—	19K9
T2INS1	—	—	30M9	19K9
TACK0	—	—	—	24A9
UDI00	8S4	16A6	—	18C5
UIR41	—	—	28C5	18F5
UMDR1	9R5	—	—	18C5
USRH0	—	16A1	—	18E5
USRL0	—	16A1	—	18D5
USTRB0	—	—	29A4	18C5
UTI	—	12L9	—	18H1
WAIT0	8L9	—	—	21R1
WO	—	—	30B9	—
WRTOA	—	—	27L1	—
XO	9R9	12A6	—	—

FO1	AS SHOWN WITH POWER FAIL DETECT CIRCUIT LOCATED ON SHEET 19
FO2	AS SHOWN LESS POWER FAIL DETECT CIRCUIT LOCATED ON SHEET 19

CONNECTOR 3 PIN INDEX

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
XI	9S9	—	26A1	—
+15	—	—	—	19D1
-15	—	—	—	19J1
12VAC	—	—	—	19A3
12VAC	—	—	—	19A4

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
CWR0	—	—	27R9	—
ESN00	—	—	—	21M2
INIT0	—	—	—	19A4
LA0	—	—	—	21F9
LB0	—	—	—	21F9
LC0	—	—	—	21F9
LD0	—	—	—	21F9
MA00IA	—	—	25A7	—
MA01IA	—	—	25B7	—
MA02IA	—	—	25C7	—
MA03IA	—	—	25D7	—
MA04IA	—	—	25E7	—
MA05IA	—	—	25F7	—
MA06IA	—	—	2567	—
POFF0	—	—	—	19A4
PRTECT0	—	—	27N9	—
SD001	—	—	—	21E6
SD011	—	—	—	21F6
SD021	—	—	—	21F6
SD031	—	—	—	21F6
SD041	—	—	—	21G6
SD051	—	—	—	21H6
SD061	—	—	—	21H6
SD071	—	—	—	21J6
SH10	—	—	—	21A9
SL00	—	—	—	21A9
SRG0	—	—	—	21B9
SSGL1	—	—	—	21H7
SSNC0	—	—	—	21N2
WAIT1	—	—	—	21R9
GND	—	—	—	21J6

TTY STUB CABLE INDEX

PIN NO.	I/O LOC.
103-2	22N7
102-2	22N8
204-2	22N8
203-2	22N8
104-2	22N9
202-2	22N9

TEST POINT INDEX

DESIG	MNEM	LOC.	BOARD
A	TMG1A	22S6	I/O
B	ENABL1	24D9	I/O
C	ATN1	24B9	I/O
D	READ1	22S6	I/O
E	SYSCLI	19G5	I/O
F	ADI	22K2	I/O
G	ARM0	24F9	I/O

DESIG	MNEM	LOC	BOARD
A	READ 1	27N9	MEM CON.
B	DCH1	30J1	MEM CON.
C	CLMR0	30H9	MEM CON.
D	MB0	30F1	MEM CON.
E	STARTO	30F1	MEM CON.
F	FE1	30F7	MEM CON.

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION	
ROM	35-388 M03 E04
ALU	35-389 M01 R06
MEM. CONT	35-387 M02 R02
I/O	35-390 M02 R12
MEM CONT	35-387 M01 E04
ROM	35-388 M02 R06
ROM (50)	35-412 M02 RC5

NOTE:
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

REVISIONS

REVISED SHTS 2, 4, 8, 9, 18 & 19.
RC | PB | — | PB | 14 MAR 72 | 185

REVISED SHTS 1, 2, 4, 5, 3, 18, 19, 20, 21, 23, 26, 29 & 30.
B2 | PB | — | PB | 3 JULY 72 | 155

RELEASED FOR PRODUCTION
ENG. MNG. DATE 8/1/72

CHG:
SHT 1 LOC N8,9
35-388 M02 & 35-387 M01 WAS R00, 35-389 M01 WAS R01, 35-390 M02 WAS R01

REVISED:
SHT. INDEX REV. LEV OF SHT #1, 4, 8, 9, 27, 29 & 30
B4 | PB | 1511 | MA | 10/13/72 | R01

CHANGE:
SHT 1 LOC N8, 35-387 M01 WAS R01
35-388 M02 WAS R01
35-390 M02 WAS R05

REVISED:
SHT INDEX REV. LEV SHT 19, 29, 1, 4, 8, 30, 37
B6 | RJ | 1533 1538 | MA | 11/9/72 | R02

CHANGE:
SHT 1 LOC N8, 35-390 M02 WAS R06

REVISED:
SHT INDEX REV. LEVEL SHT 4, 5, 8, 9, 20, 26, 35
B6 | RJ | 1554 | | | M03

CHG 35-388 M03 WAS 35-388 M02 R03, 35-387 M02 WAS 35-387 M01 R02
LOC M, N-8. CHG SHT INDEX FOR SHTS. 1, 31, 32, 37 & 38.
ADDED 31A, 32A, 37A & 38A TO SHT INDEX
B4 | | V604 | MA | 1/9/73 | E04

CHG SHT INDEX FOR SHT 1. 35-389 M01 WAS R02 (PC BD. INDEX)
B4 | RC | 1640 | MA | 2/15/73 | E05

CHG SHT 1, 35-389 M01 TO M02
CHG SHT 19, 10. 35-388 M03 WAS R00
35-389 M01 WAS R05
B4 | RC | 1672 | MA | 2/15/73 | R06

CHG SHT INDEX FOR SHT 1 & 27. ADDED 35-387 M01 TO PC BD INDEX
B4 | MA | V664 | MA | 2/15/73 | E07

CHG SHT 19 & 35-390 M02 WAS E07
B4 | RC | V699 | MA | 3/21/73 | E08

CHG SHT 21 & 36
B4 | MA | 1754 | MA | 5/3/73 | R09

REV LEVEL OF SHT 10 WAS R06. REV LEVEL OF SHT 13 WAS R00 IN P.C. BRD. INDEX REV LEVEL OF ALU WAS SPEC AS R04.
B4 | MA | 1853 | MA | 6-29-73 | R10

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SHEET	REV. LEVEL
INDEX	SHEET NO.

16 01 | 06 03 | 03 04 08 | 01 | 02 11 03 10 | 03 37 | 02 04 24 | 04 | 01 05 09 24 | 04

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38

NOTES

REVISIONS CONT.
CHG. SHT'S 17, 19, 30, 34, 35
35-390 M02 WAS R09 PER ECN 1924
CHG. SHTS 2, 10, 17, & 21 LOC L7 MNEM. SWTALO WAS

LOC'D ON 21M5 (I/O BD)
35-389 M01 WAS R05
35-390 M02 WAS R10
B6 | | V926 | MA | 9-25-73 | R11
CHG'D SH. 9 AREA M16 R5
TP | | 1980 | MA | 10-23-73 | R12

35-388 M03 WAS R03
35-412 M02 WAS R04
B6 | | 2006 | MA | 11-2-73 | R13
REVISED SHT'S 19 & 35. LOC N8 35-390 M02 WAS R11
B6 | | 2008 | MA | 12-14-73 | R14

REVISED SHEETS 1 & 30
JH | | 2196 | MA | 7-15-74 | R15
REVISED SHEET 19
JH | | 2191 | MA | 6-11-74 | R16

NAME	TITLE	DATE
E. ROE	DRAFT	2, 14, 73, 74
R CERO	CHK	7-10-
P GALAS	ENGR	7-10-72
M FUCHS	Q.C.	7-10-72
RE JONES	DIR ENG	7-10-72

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
TASK NO. 03116 | DWG NO. Q-051 M01 ERG D08 | SHEET OF 1-38

BRUNING 44-231-15043

BACK PANEL MAP

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CONN.	TITLE BD. LOC. TERM. NO.	ROM 07 ROW 1	ROM 07 ROW 2	ALU 06 ROW 1	ALU 06 ROW 2	I/O CTRL 05 ROW 1	I/O CTRL 05 ROW 2	MEM CTRL 04 ROW 1	MEM CTRL 04 ROW 2
1	41	P5	GND	P5	GND	P5	GND	P5	GND
	40	GND	SRD041	GND	KILDSTO	GND	KILDSTO	GND	
	39	SRD051	SRD061			+12V	12VAC		
	38	SRD071	SRD001		CLKOFF0	LDI00	CATNO	WRTOA	
	37	LOADI	KSKIP0		SCLR0		SNGLO	MDI50	MDI60
	36	SRD011	SRD021	SYSCLI		FAST0	KSKIP0	MDI30	MDI40
	35	SRD031	SRD121	LOADI		SYSCLI	ARST1	MDI10	MDI20
	34	SRDI31	SRD141			TACK0	RACK0	MD090	MDI00
	33	SRDI51	SRD081			CLKOFF0	EXTCLK0	MD070	MD080
	32	DI	SKIP0		SCLO	DI	SKIP0	MD050	MD060
	31	DTEST0	GDEST1	GDEST1	USRLO	USRLO	DTEST0	MD030	MD040
	30	UDI00	LDI00	UDI00	USRH0	USRH0	UDI00	MD010	MD020
	29	UMDR1	SRD091		SHOT1	SHOT1	PFF1	PFF1	MD000
	28	SRDI01	DDC1	DDC1	CSV1	CSV1	UMDR1	DDC1	SSMEM1
	27	SRDIII	KILDSTO	S000	B000	B080	S000	S000	B000
	26	P21	SWTAL0	S010	B010	B090		S010	B010
	25	PC00	SVSC0	S020	B020	B100	RCLO	S020	B020
	24	RCLO	LRAH0	S030	B030	B110	LRAH0	S030	B030
	23	JACC0	SV0	S040	B040	B120	JACC0	S040	B040
	22	LCC0	RALI10	S050	B050	B130	LCC0	S050	B050
	21	LINE1	RALI00	S060	B060	B140	LINE1	S060	B060
	20	LFLR0	RAL090	S070	B070	B150	LFLR0	S070	B070
	19		RAL080	S080	B080			S080	B080
	18	GIPI0	LRALO	S090	B090		LRALO	S090	B090
	17	GTP20	DISR0	S100	B100	SV0		S100	B100
	16	OPI		S110	B110	SVSC0	OPI	S110	B110
	15	DT21	SVAC0	S120	B120	PC00	SVAC0	S120	B120
	14	B130		S130	B130	NOTE 1	WAIT0	S130	B130
	13		WAIT0	S140	B140	P21	DCAK0	S140	B140
	12	DST0	LDCTR0	S150	B150		DST0	S150	B150
	11	SCLO	S081	S081	S001	S001	SCLO	SCLO	LDCTR0
	10	RAH040	S091	S091	S011	S081	USTRB0	USTRB0	MS000
	09	STF0	S101	S101	S021	S091	STF0	MS010	MS020
	08	STFL0	S111	S111	S031	S101	STFL0	MS030	MS040
	07	RAH050	S121	S121	S041	S111		MS050	MS060
	06	INHINC0	S131	S131	S051		S131	MS070	MS080
	05	RAH060	S141	S141	S061		S141	MS090	MS100
	04	HIDJAC0	S151	S151	S071		S151	MS110	MS120
	03	BANK0	RAH070	CTF1	BANK0	BANK0	CTF1	MS130	MS140
	02	STPA0	FRCLOC0	FRCLOC0	FRNSI	FRNSI	STPA0	MS150	MS160
	01	GND	CLR0	GND	CLR0	GND	CLR0	GND	CLR0
	00	P5	GND	P5	GND	P5	GND	P5	GND
		1	2	1	2	1	2	1	2
0	41	P5	GND	P5	GND	P5	GND	P5	GND
	40	GND	SCLRIA	GND	SCLRIA	GND	SCLRIA	GND	SCLRIA
	39	FPMBY0	IR000		LARI	SCLR0	RD001	IR001	FPMBY0
	38	CS1	IR011	CS1	GA000	GA000	RD011	IR011	CS1
	37	FMDBY1	IR021		GB000	GB000	ATN0	IR021	FMDBY1
	36	FMDUA1	IR031			LDI01	ACKA00	IR031	FMDUA1
	35	LIR0	IR041			SR0	CL070	IR041	LIR0
	34	LPSWI	IR051	LDI01		DR0	DC0	IR051	LPSWI
	33	LMAR0	IR061	SVSC0	SVAC0	DA0	DRD0	IR061	LMAR0
	32	LMDR1	IR071	AMOD1	DT21	ADRS0	CMD0	IR071	LMDR1
	31	MAR150	HW0	D070	IR080	D150	LPSWI	IR080	MAR150
	30	JOE1	SYN0	D060	IR090	D140	SYN0	IR090	JOE1
	29	NOMEM0	AMOD1	D050	IR100	D130	T21	IR100	NOMEM0
	28	P00	T21	D040	IR110	D120	RDSTB0	IR110	P00
	27	PSW071	RDSTB0	D030	IR120	D110	INTA0	IR120	PSW071
	26	X0	CLRIR0	D020	IR130	D100	PSW041	IR130	PSW041
	25	SHR1	HDEST0	D010	IR140	D090	PSW021	IR140	PSW021
	24	SHL1	LAR1	D000	IR150	D080	PSW011	IR150	PSW011
	23	SYSCL1	LARYS0	LARYS0	X0	T2INS1	CC121	CC121	T2INS1
	22	INTA0	LSRLO	LSRLO	DECTR0	DECTR0	CC131	CC131	DECTR0
	21	X1	DCLO	CTONE0	DCLO	DCLO	CC141	CC141	DCLO
	20	RD000	RD001	RD001	RD000	RD000	CC151	CC151	X1
	19	RD010	RD011	RD011	RD010	RD010	CTONE0	CTONE0	CLRIR0
	18	RD020	RD021	RD021	RD020	VIR41	RD021	MCLR1	VIR41
	17	RD030	RD031	RD031	RD030	RD030	RD031	RD040	REQ0
	16	RD040	RD041	RD041	SHR1	RD040	RD041	RD050	ENO
	15	RD050	RD051	RD051	SHL1	RD050	RD051	MA130	MA140
	14	RD060	RD061	RD061	RD060	RD060	RD061	MA110	MA120
	13	RD070	RD071	RD071	RD070	RD070	RD071	MA090	MA100
	12	RD080	RD081	RD081	RD080	RD080	RD081	MA070	MA080
	11	RD090	RD091	RD091	RD090	RD090	RD091	MA050	MA060
	10	RDI00	RDI01	RDI01	RDI00	RDI00	RDI01	MA030	MA040
	09	RDI10	RDI11	RDI11	RDI10	RDI10	RDI11	MA020	MA021
	08	RDI20	RDI21	RDI21	FLR121	FLR121	RDI21	RD090	RDI10
	07	RDI30	RDI31	RDI31	STPC0	STPC0	RDI31	MA010	MA011
	06	RDI40	RDI41	RDI41		RDI40	RDI41	MA000	MA001
	05	RDI50	RDI51	RDI51	UTI	RDI50	RDI51	PAR0	CEMT0
	04	STOP0	RALI20	SUB1	CEMT0	STOP0	SUB1	INH0	EPO
	03	RALI50	SSKIP0		HDEST0	UTI	SSKIP0	WO	LRO
	02	RALI40	RALI30			+15V	-15V	RESET	SDUA0
	01	GND	P210	GND		GND	MSKI	GND	MSKI
	00	P5	GND	P5	GND	P5	GND	P5	GND
		1	2	1	2	1	2	1	2

CONN.	TITLE BD. LOC. TERM. NO.	MEM/IO 03 ROW 1	MEM/IO 03 ROW 2	MEM/IO 02 ROW 1	MEM/IO 02 ROW 2	MEM/IO 01 ROW 1	MEM/IO 01 ROW 2	MEM/IO 00 ROW 1	MEM/IO 00 ROW 2
1	41	P5	GND					P5	GND
	40	GND	GND					GND	GND
	39	P15	015					P15	P15
	38	N15	N15					N15	N15
	37	MDI60	MDI60					MDI60	MDI60
	36	MDI30	MDI40					MDI30	MDI40
	35	MDI10	MDI20					MDI10	MDI20
	34	MD090	MDI00					MD090	MDI00
	33	MD070	MD080					MD070	MD080
	32	MD050	MD060					MD050	MD060
	31	MD030	MD040					MD030	MD040
	30	MD010	MD020					MD010	MD020
	29	EXVT	MD000					EXVT	MD000
	28	TEMPA	VT					TEMPA	VT
	27	WRT0	TEMPB					WRT0	TEMPB
	26	SCLR0	HW0					SCLR0	HW0
	25								
	24								
	23	SYN0	ATN0					SYN0	ATN0
	22	RACK0	TACK0					RACK0	TACK0
	21	CL070	DA0					CL070	DA0
	20	DR0	CMD0					DR0	CMD0
	19	SR0	ADRS0					SR0	ADRS0
	18	DI40	DI50					DI40	DI50
	17	DI20	DI30					DI20	DI30
	16	DI00	DI10					DI00	DI10
	15	DO80	DO90					DO80	DO90
	14	DO60	DO70					DO60	DO70
	13	DO40	DO50					DO40	DO50
	12	DO20	DO30					DO20	DO30
	11	DO00	DO10					DO00	DO10
	10	MA030	MA040					MA030	MA040
	09	MA020	MA021					MA020	MA021
	08	MA01	MA02					MA01	MA02
	07	MA010	MA011					MA010	MA011
	06	MA000	MA001					MA000	MA001
	05	PAR0	MA00					PAR0	MA00
	04	INH0	ER0					INH0	ER0
	03	WO	LR0					WO	LR0
	02	P15	N15					P15	N15
	01	GND	GND					GND	GND
	00	P5	GND					P5	GND
		1	2	1	2	1	2	1	2
0	41	P5	GND					P5	GND
	40	GND	GND					GND	GND
	39	P15	REQ0					P15	REQ0
	38	'115	ENO					N15	ENO
	37	ACT0	TAC0					ACT0	TAC0
	36								
	35								
	34							XRACK0	
	33	MA130	MA140					MA130	MA140
	32	MA110	MA120					MA110	MA120
	31	MA090	MA100					MA090	MA100
	30	MA070	MA080					MA070	MA080
	29	MA050	MA060					MA050	MA060
	28	RDACK0	TDACK0					RDACK0	TDACK0
	27	DC0	DCR0					DC0	DCR0
	26	SCLR0	HW0					SCLR0	HW0
	25								
	24								
	23	SYN0	ATN0					SYN0	ATN0
	22	RACK0	TACK0					RACK0	TACK0
	21	CL070	DA0					CL070	DA0
	20	DR0	CMD0					DR0	CMD0
	19	SR0	ADRS0					SR0	ADRS0
	18	DI40	DI50					DI40	DI50
	17	DI20	DI30					DI20	DI30
	16	DI00	DI10					DI00	DI10
	15	DO80	DO90					DO80	DO90
	14	DO60	DO70					DO60	DO70
	13	DO40	DO50					DO40	DO50
	12	DO20	DO30					DO20	DO30
	11	DO00	DO10					DO00	DO10
	10	MA030	MA040					MA030	MA040
	09	MA020	MA021					MA020	MA021
	08	MA01	MA02					MA01	MA02
	07	MA010	MA011					MA010	MA011
	06	MA000	MA001					MA000	MA001
	05	PAR0	MA00					PAR0	MA00
	04	TNH0	ER0					INH0	ER0
	03	WO	LR0					WO	LR0
	02	P15	N15					P15	N15
	01	GND	GND					GND	GND
	00	P5	GND					P5	GND
		1	2	1	2	1	2	1	2

NOTES 1. CIRCUIT AVAIL. NO CONNECTION ON BACK PANEL - SEE SHT 2/IMS.

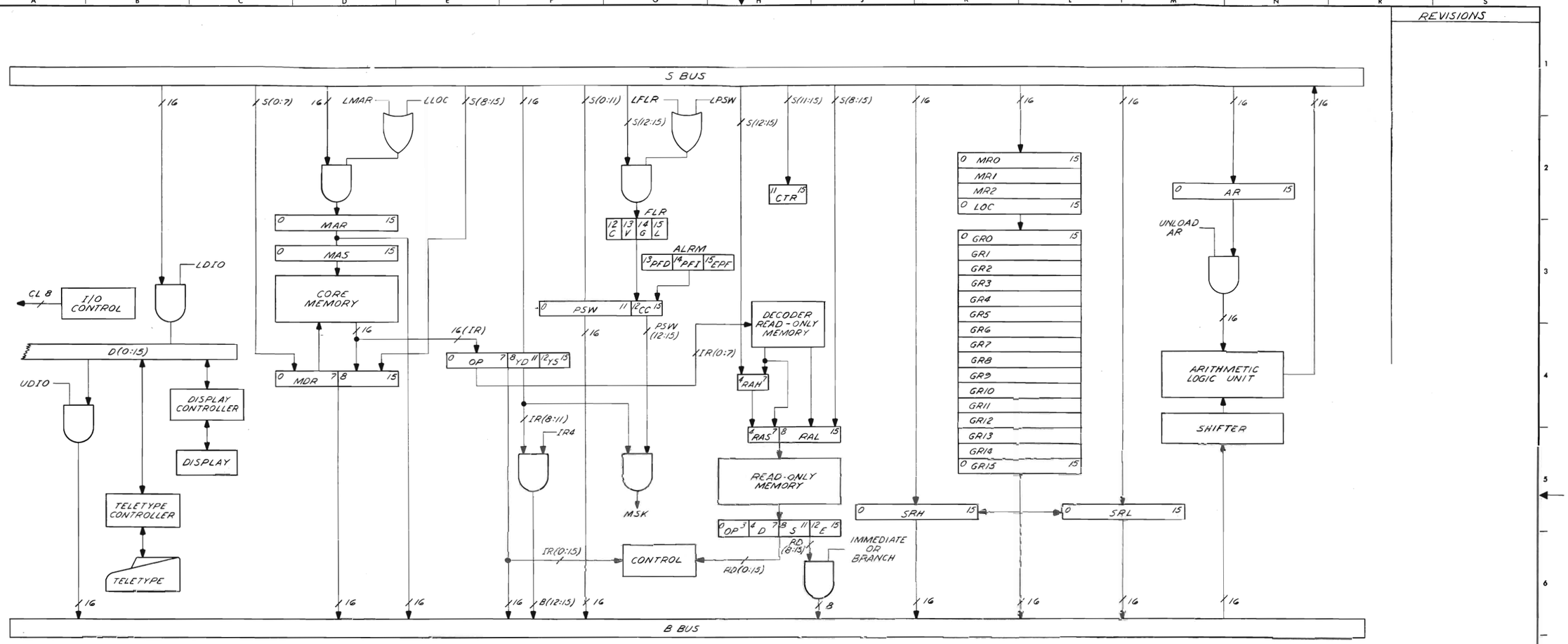
REVISIONS			
ADDED NOTE 1 LOC E4 : A9			
BG	1926	9-25-73	R01

NAME	TITLE	DATE	TITLE
K. LAFFERTY	DRAFT	27 MAR 72	BACK PANEL MAP MODEL 70 PROCESSOR (CPU)
	CHK		
	ENGR		
	DIR ENG		

TASK NO. 03116 | DWG NO. 01-051 M01 R01 D08 | SHEET OF 2-38

INTERDATA®

REVISIONS



	INSTRUCTION	DESTINATIONS	SOURCES
0000	DO	RAH/MR0	MR0
0001	COMMAND	RAL/MR1	MR1
0010	TEST	PSW/MR2	MR2
0011	BRANCH	LOC	LOC
0100	LOAD	FLR	PSW
0101	LOAD IMMEDIATE	MAR	MAR
0110	OR	SRH	SRH
0111	OR IMMEDIATE	SRL	SRL
1000	AND	AR	NULL
1001	AND IMMEDIATE	IR	IR
1010	EXCLUSIVE OR	MDR	MDR
1011	EXCLUSIVE OR IMMEDIATE	IO	IO
1100	ADD	CTR	IR4
1101	ADD IMMEDIATE	YS	YS
1110	SUBTRACT	YD	YD
1111	SUBTRACT IMMEDIATE	YDPI	YDPI

DO FUNCTIONS

4	5	6	7	8	9	10	11	12	13	14	15	
1	0									1		MR
0	1									1		MW
1	1									1		PW
		1								1		INC
			1							1		JAM
				1						1		PC
					1					1		CLR
						1				1		SWA
							1			1		CWA
								1		1		ALRM
									1	1		
										1	1	POW
1	0	1	0	1	1	0	0	0	0	1	0	P2N
1	0	1	1	1	1	0	0	0	0	1	0	P2J

COMMAND FUNCTIONS

4	5	6	7	8	9	10	11	12	13	14	15	
1	0											MR
0	1											MW
1	1											PW
		1	1	0						1	1	MPY
		1	0	1						0	1	DIV
		1	0	0	1							RPT
			1									SRI
				1								SLI
						1	0					SUT
						0	1					CUT
						1	1					TUT
								1				SB
									1			CB
										1		CI
											1	CO

TEST FUNCTIONS

4	5	6	7	8	9	10	11	12	13	14	15	
1												FAST
	1											ATN
		1										ARST
			1									CATN
				1								SNGL
					1							UT
						1						MALF
							1					PPF
								1				DC
									1			DRD
										1		MSK
											1	OP

EXTENDED FIELD

12	13	14	15		
1	0			SL	LOAD
0	1			SR	
1	1			CS	
		1		CI	
			1	CO	
		0	0	DCAK	IO = DEST/SOURCE
		0	1	ADRS/ACK	
		1	0	DA/DR	
		1	1	CMD/STAT	
1				NA	NON LOAD
	0			NF	
		1		CI	
			1	CO	

BRANCH

0	0	0	0	
1				C
	1			V
		1		G
			1	L

CTR

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NOTES

NAME	TITLE	DATE
W ZILLGER	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DRAFTING	

TITLE BLOCK DIAGRAM
MODEL 70 PROCESSOR

TASK NO. 03116
DWG NO. 01-051M01 008
SHEET 3 OF 36

BRUNING 44 231 15043

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D ROM AND
I/O CONTROL

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.

REVISIONS					
CHG: LOC C8 NMEM. WAS GDROMB, GDROMA. LOC J3, R82-12 WAS R2071	BM	PB	1511	11/4/72	R01
CHG: LOC A4 IC A96-07 WAS NC.	BM	PB	1554	11/10/72	R03
CHG. A107 LOC F2 WAS 19-016 MG.	BM	PB	1672		R06

NAME	TITLE	DATE
E. ROE	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-051M01R2-008
SHEET 4-38 OF

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BRUNING 44 231 15043

See Mod

INTERDATA®

CLR80

PSW07 127-0 9B9 RACLR0 445, 9H1 SCLR0 839

SCLR1A 846 240-0

211-1 SOB1 SRALO80 4F9 LRALI

210-1 SOA1 SRALO90 4F9

209-1 S121 SRALO0 4F9

208-1 S111 SRALO10 4F9

207-1 S121 110-1 RAH40 6A1 RAH041 4D9 SRAH040

206-1 S131 7A2 RAH050 107-1 6A2 RAH051 4D9 SRAH050

205-1 S141 6A2 RAH060 105-1 6A5 RAH061 4D9 SRAH060

204-1 S151 6A2 RAH070 203-1 6A4 RAH071 4E9 SRAH070 S150A

E17 6.8K P5

E16 6.8K P5

RCLO 124-1

LRAHO 224-1

LRALO

E59 1K P5 LRALI

E13 1K P5 RCLI

INHINGO 106-1 218-1 LRALO

PFO

A16 19-040 4 STAGE CARRY LOOK AHEAD

A18 19-040 4 STAGE CARRY LOOK AHEAD

ROM ADDRESS REGISTER

219-1 RAL080 7A1

RAL081 6A1

L9 TRA081

220-1 RAL090 7A1

L6 TRA091 6A1

221-1 RAL100 7A1

L6 TRA101 6A1

222-1 RAL110 7A1

L6 TRA111 6A1

209-07 RAL120 7A1

R6 TRA121 6A1

202 RAL130 7A1

R6 TRA131 6A1

103-1 RAL140 7A1

N6 TRA141 6A1

RAL150 7A1

N6 TRA151 6A1

P2 TRA081

NOTES

1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.

REMOVED: LOC 04
REMOVED SHT REF 3 A4
FROM RAH050

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NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-05M01R03008
SHEET 5 OF 38

BRUNING 44-231 15043

INTERDATA®

5J9 RAL 151
5H9 RAL 141
5G9 RAL 131
5F9 RAL 121
5E9 RAL 111
5D9 RAL 101
5C9 RAL 091
5A9 RAL 081

5E4 RAH 051

5G4 RAH 070
5F4 RAH 060

A25 19-058 5G

ENO00 7D2

ENO10 7D4

5H4 RAH 071

A25 19-058 5G

5G4 RAH 061

A35 19-058 5G

EN100 7D6

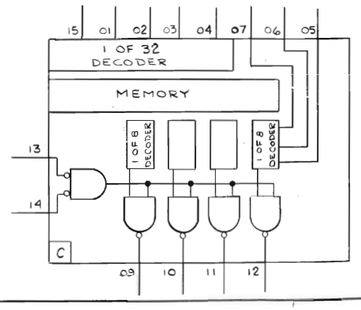
P5
R15 1K
217-1 DISRO

A35 19-058 5G

EN110 7D8

A01 19-049-F04
A02 19-049-F05
A03 19-049-F06
A04 19-049-F07
A11 19-049-F08
A12 19-049-F09
A13 19-049-F10
A14 19-049-F11
A21 19-049-F12
A22 19-049-F13
A23 19-049-F14
A24 19-049-F15
A31 19-049-F16
A32 19-049-F17
A33 19-049-F18
A34 19-049-F19

7H9 SRD001
7H9 SRD011
SRD031 7J9
SRD021 7J9
7K9 SRD041
7K9 SRD051
SRD071 7L9
SRD061 7L9
7M9 SRD081
7M9 SRD091
SRD111 7N9
SRD101 7N9
7R9 SRD121
7R9 SRD131
7R9 SRD141
7R9 SRD151



ROM PAGE 0,1,2 & 3

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NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO 03116
DWG NO 01-051.MD1 D08
SHEET 6 OF 38

BRUNING 44231 15043

INTERDATA®

5H9 RAL 150
5G9 RAL 140
5F9 RAL 130
5E9 RAL 120
5D9 RAL 110
5C9 RAL 100
5B9 RAL 090
5A9 RAL 080

5D4 RAH 050

6E2 EN000
6E3 EN010
8A9
6E5 EN100
8A4
6E7 EN110
8A4

A41 19-049-F20
A42 19-049-F21
A43 19-049-F22
A44 19-049-F23
A51 19-049-F24
A52 19-049-F25
A53 19-049-F26
A54 19-049-F27
A61 SEE NOTE 2
A62 SEE NOTE 2
A63 SEE NOTE 2
A64 SEE NOTE 2
A71 SEE NOTE 2
A72 SEE NOTE 2
A73 SEE NOTE 2
A74 SEE NOTE 2

R1 470 R2 470 R3 470 R4 470
R5 470 R6 470 R7 470 R8 470
R9 470 R43 470 R13 470 R14 470
R10 470 R41 470 R11 470 R18 470

P5

8B1, 4H9 SRD001
8C1, 6H9 SRD011
SRD031 6J9, 8D1
SRD021 6J9, 8D1
8E1, 6K9 SRD041
6K9 SRD051
SRD071 6L9, 8H1
SRD061 6L9, 8G1
8J1, 6M9 SRD081
6M9 SRD091
SRD111 8M1, 6N9
SRD101 6N9, 8L1
8N1, 6R9 SRD121
8N1, 6R9 SRD131
8R1, 6R9 SRD141
8S1, 6R9 SRD151

1 OF 32 DECODER
MEMORY
1 OF 8 DECODER
1 OF 8 DECODER

ROM PAGE 4, 5, 6 & 7

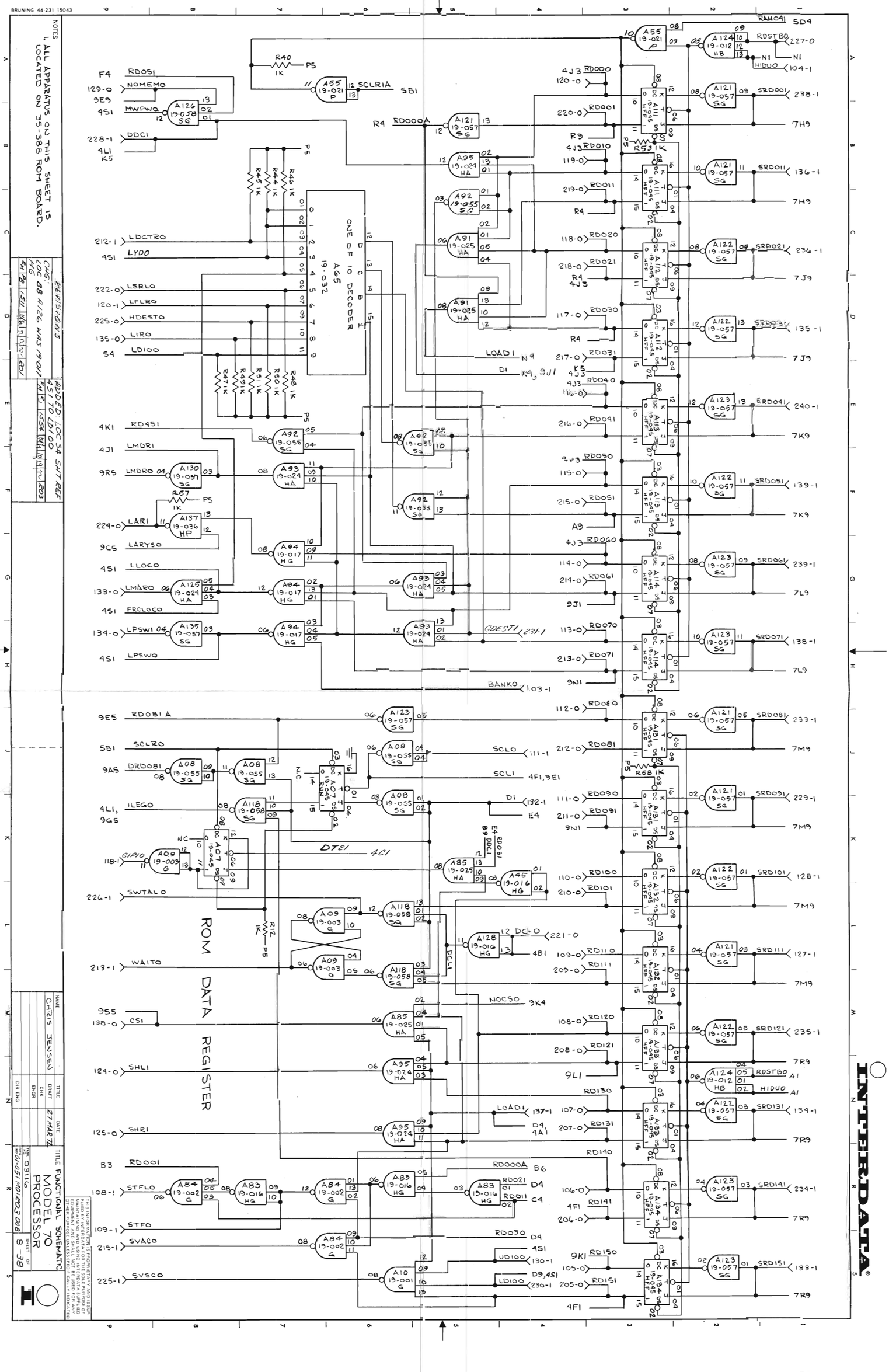
NOTES
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2. COMPONENTS ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THE ASSEMBLY.

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NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	27MAR72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 01-051M01
SHEET 7 OF 38

BRUNING 44-231 15043


ROM DATA REGISTER
ONE OF 10 DECODER A65 19-032
NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.
REVISIONS
ADDED LOC 54 SHT REF
CHG LOC 88 TO LOC 89
LOC 88 WAS 9D17
TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
DRAWN CHRIS JENSEN
DATE 27 MAR 74
SIZE B
SHEET 8 OF 38
INTERDATA

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DECOUPLING CAPACITORS

PHASE CONTROL

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.
2. THIS ROM BOARD MUST USE BACKPANEL NO. 11-115 F01 R04

REVISIONS

CHG: LOC C6 A139-13 WAS-11
LOC N9 NMEM WAS GOROMO. LOC N4 A99 WAS A

BY	DATE	REV
RM	1511	R01
RM	1554	R03
TD	1980	R04

CHG. LOC M1 IC A177 DI WAS PIN 04 MSSTO WAS PIN 05

AREA M1 ADD. REF R5 TO MSSTO AREA R5;
A181 MSSTO T21SYI WAS A181 T21SYI

NAME	TITLE	DATE
E. ROE	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR

TASK NO. 03116
DWG NO. 01-051 M01 R04 A208

SHEET OF 9-38

BRUNING 44 231 15043

INTERDATA®

REGISTER STACK ADDRESS DECODING

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NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-389 ALU BOARD.

CHG. R29-32 LOC L8 WAS I/K
RH | RC | 1672 | 11/H | 206

IN AREA H1 A100 PIN 9 WAS SPEC AS DEST 13L4. IN SAME AREA A100 PIN 8 GOING TO DEST 13L3 WAS NOT SPEC.
BC | 1853 | 11/H | 6-29-73 | R07

LOC A5, B5 R43 & R44 WERE 1K, LOC F8 & G8 RESISTORS WERE 1K, LOC G4 ADDED A62 19-009
BG | KK | 1928 | MM | 9-25-73 | R08

NAME	TITLE	DATE
E. ROE	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 01-051 M01F0 8008
SHEET 10-38

BRUNING 44-231 15043

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10H5 WM50
10G5 WMA1
10G5 WMB1
10E1 RM50
10F4 RMA1
10F4 RMB1

10L9 GW00
10B9 GR00
10H9 RA1
10F9 RB1
10R9 WB1
10S9 WA1

10L9 GW10
10C9 GR10

10M9 GW20
10D9 GR20
RA1
RB1

10N9 GW30
10E9 GR30

19-041 A07 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A08 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A09 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A10 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A11 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03

14D9 5030
14C9 5020
14B9 5010
14A9 5000

14A1, 13C5, 16B5
14A1, 16B5
14B1, 16C5
14C1, 16D5

B000 (227-1
B010 (226-1
B020 (225-1
B030 (224-1

5030 (124-1
5020 (125-1
5010 (126-1
5000 (127-1

14D1, 16E5
14E1, 16F5
14K1, 16G5
14M1, 16H5

19-041 A18 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A19 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A20 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A21 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A22 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03

14G9 5070
14F9 5060
14E9 5050
14E9 5040

B040 (223-1
B050 (222-1
B060 (221-1
B070 (220-1

5070 (120-1
5060 (121-1
5050 (122-1
5040 (123-1

14A1, 13C4, 16H5
14B1, 13C4, 16J5
14C1, 13D4, 16K5
14D1, 13E4, 16L5

19-041 A29 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A30 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A31 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A32 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A33 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03

14L9 5110
14K9 5100
14J9 5090
14H9 5080

B080 (219-1
B090 (218-1
B100 (217-1
B110 (216-1

5110 (116-1
5100 (117-1
5090 (118-1
5080 (119-1

14E1, 13E4, 16L5
14K1, 13F4, 16M5
14M1, 13F4, 16N5
14M1, 13G4, 16R5

19-041 A40 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
SEL-B SEL-A EN (READ) SEL-B SEL-A EN (WRITE) | INPUTS A B C D | OUTPUTS 1 2 3 4
19-041 A41 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A42 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A43 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03
19-041 A44 — 04 05 11 13 14 12 | A | 10 09 07 06 | 15 01 02 03

14R9 5150
14N9 5140
14M9 5130
14M9 5120

B120 (215-1
B130 (214-1
B140 (213-1
B150 (212-1

5150 (112-1
5140 (113-1
5130 (114-1
5120 (115-1

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-389 ALU BOARD.

REGISTER STACK

NAME	TITLE	DATE
L. VALENTY	DRAFT	27 MAR 72
	CHK	
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	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 01-051 M01 DOB
SHEET 11 OF 35

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INTERDATA

A55 19-030 INPUTS A B C D OUTPUTS A B C D

A53 19-030

A51 19-030

A39 19-030

	RD 0	RD 1	RD 2	M1	S0	S1	S2	S3
D, C	0	0	0	0	1	0	0	1
T, B	0	0	1	1	1	1	1	1
L	0	1	0	1	1	1	1	1
O	0	1	1	1	1	1	0	1
N	1	0	0	1	0	1	1	1
X	1	0	1	1	1	0	0	1
A	1	1	0	0	1	0	0	1
S	1	1	1	0	0	1	1	0

"A" REGISTER

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NOTES 1. ALL APPARATUS ON THIS SHEET LOCATED ON 35-389 ALU BOARD.

NAME	TITLE	DATE
E. ROE	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 21-051M01 DOC 12-38
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RD0001 RD0011 RD0021 RD0031 RD0071 RD0061 RD0081 RD0010A RD0020 RD0000A

CSRO CSLO MPYO DDCO RD151 RD101 RD111 RD121 RD131 RD141 RD151 SCLO

SVSCO SVACO RD0081 RD031 SMRL SMLL SRELS1 SRHO01 CSRI CSLI SHOT1

MPYO CLRBCO CMND1 CTLT21 CEMTO_NG CEMTO DIRECTRO

A1 CS20 A1 MD20 A1 CS40 DIV0 DIV1 PR5 STSCLO STSRZO KLDSTO

A1 CS40 A1 MD40 A1 CS80 A1 MD80 A1 CS160 A1 MD160 A1 CS320 A1 MD320

A1 CS640 A1 MD640 A1 CS1280 A1 MD1280 A1 CS2560 A1 MD2560 A1 CS5120 A1 MD5120

A1 CS10240 A1 MD10240 A1 CS20480 A1 MD20480 A1 CS40960 A1 MD40960 A1 CS81920 A1 MD81920

A1 CS163840 A1 MD163840 A1 CS327680 A1 MD327680 A1 CS655360 A1 MD655360 A1 CS1310720 A1 MD1310720

A1 CS2621440 A1 MD2621440 A1 CS5242880 A1 MD5242880 A1 CS10485760 A1 MD10485760 A1 CS20971520 A1 MD20971520

A1 CS41943040 A1 MD41943040 A1 CS83886080 A1 MD83886080 A1 CS167772160 A1 MD167772160 A1 CS335544320 A1 MD335544320

A1 CS671088640 A1 MD671088640 A1 CS1342177280 A1 MD1342177280 A1 CS2684354560 A1 MD2684354560 A1 CS5368709120 A1 MD5368709120

A1 CS10737418240 A1 MD10737418240 A1 CS21474836480 A1 MD21474836480 A1 CS42949672960 A1 MD42949672960 A1 CS85899345920 A1 MD85899345920

A1 CS171798691840 A1 MD171798691840 A1 CS343597383680 A1 MD343597383680 A1 CS687194767360 A1 MD687194767360 A1 CS1374389534720 A1 MD1374389534720

A1 CS2748779069440 A1 MD2748779069440 A1 CS5497558138880 A1 MD5497558138880 A1 CS10995116277760 A1 MD10995116277760 A1 CS21990232555520 A1 MD21990232555520

A1 CS43980465111040 A1 MD43980465111040 A1 CS87960930222080 A1 MD87960930222080 A1 CS175921860444160 A1 MD175921860444160 A1 CS351843720888320 A1 MD351843720888320

A1 CS703687441776640 A1 MD703687441776640 A1 CS1407374883553280 A1 MD1407374883553280 A1 CS2814749767106560 A1 MD2814749767106560 A1 CS5629499534213120 A1 MD5629499534213120

A1 CS11258999068426240 A1 MD11258999068426240 A1 CS22517998136852480 A1 MD22517998136852480 A1 CS45035996273704960 A1 MD45035996273704960 A1 CS90071992547409920 A1 MD90071992547409920

A1 CS180143985094819840 A1 MD180143985094819840 A1 CS360287970189639680 A1 MD360287970189639680 A1 CS720575940379279360 A1 MD720575940379279360 A1 CS1441151880758558720 A1 MD1441151880758558720

A1 CS2882303761517117440 A1 MD2882303761517117440 A1 CS5764607523034234880 A1 MD5764607523034234880 A1 CS11529215046068469760 A1 MD11529215046068469760 A1 CS23058430092136939520 A1 MD23058430092136939520

A1 CS46116860184273879040 A1 MD46116860184273879040 A1 CS92233720368547758080 A1 MD92233720368547758080 A1 CS184467440737095516160 A1 MD184467440737095516160 A1 CS368934881474191032320 A1 MD368934881474191032320

A1 CS737869762948382064640 A1 MD737869762948382064640 A1 CS1475739525896764129280 A1 MD1475739525896764129280 A1 CS2951479051793528258560 A1 MD2951479051793528258560 A1 CS5902958103587056517120 A1 MD5902958103587056517120

A1 CS11805916207174113034240 A1 MD11805916207174113034240 A1 CS23611832414348226068480 A1 MD23611832414348226068480 A1 CS47223664828696452136960 A1 MD47223664828696452136960 A1 CS94447329657392904273920 A1 MD94447329657392904273920

A1 CS188894659314785808547840 A1 MD188894659314785808547840 A1 CS377789318629571617095680 A1 MD377789318629571617095680 A1 CS755578637259143234191360 A1 MD755578637259143234191360 A1 CS1511157274518286468382720 A1 MD1511157274518286468382720

A1 CS3022314549036572936765440 A1 MD3022314549036572936765440 A1 CS6044629098073145873530880 A1 MD6044629098073145873530880 A1 CS12089258196146291747061760 A1 MD12089258196146291747061760 A1 CS24178516392292583494123520 A1 MD24178516392292583494123520

A1 CS48357032784585166988247040 A1 MD48357032784585166988247040 A1 CS96714065569170333976494080 A1 MD96714065569170333976494080 A1 CS193428131138340667952988160 A1 MD193428131138340667952988160 A1 CS386856262276681335905976320 A1 MD386856262276681335905976320

A1 CS773712524553362671811952640 A1 MD773712524553362671811952640 A1 CS1547425049106725343623905280 A1 MD1547425049106725343623905280 A1 CS3094850098213450687247810560 A1 MD3094850098213450687247810560 A1 CS6189700196426901374495621120 A1 MD6189700196426901374495621120

A1 CS12379400392853802748991242240 A1 MD12379400392853802748991242240 A1 CS24758800785707605497982484480 A1 MD24758800785707605497982484480 A1 CS49517601571415210995964968960 A1 MD49517601571415210995964968960 A1 CS99035203142830421991929937920 A1 MD99035203142830421991929937920

A1 CS198070406285660843983859875840 A1 MD198070406285660843983859875840 A1 CS396140812571321687967719751680 A1 MD396140812571321687967719751680 A1 CS792281625142643375935439503360 A1 MD792281625142643375935439503360 A1 CS1584563250285286751870879006720 A1 MD1584563250285286751870879006720

A1 CS3169126500570573503741758013440 A1 MD3169126500570573503741758013440 A1 CS6338253001141147007483516026880 A1 MD6338253001141147007483516026880 A1 CS12676506002282294014967032053760 A1 MD12676506002282294014967032053760 A1 CS25353012004564588029934064107520 A1 MD25353012004564588029934064107520

A1 CS50706024009129176059868128215040 A1 MD50706024009129176059868128215040 A1 CS101412048018258352119736256430080 A1 MD101412048018258352119736256430080 A1 CS202824096036516704239472512860160 A1 MD202824096036516704239472512860160 A1 CS405648192073033408478945025720320 A1 MD405648192073033408478945025720320

A1 CS811296384146066816957890051440640 A1 MD811296384146066816957890051440640 A1 CS1622592768292133633915780102881280 A1 MD1622592768292133633915780102881280 A1 CS3245185536584267267831560205762560 A1 MD3245185536584267267831560205762560 A1 CS6490371073168534535663120411525120 A1 MD6490371073168534535663120411525120

A1 CS12980742146337069071326240823050240 A1 MD12980742146337069071326240823050240 A1 CS25961484292674138142652481646100480 A1 MD25961484292674138142652481646100480 A1 CS51922968585348276285304963292200960 A1 MD51922968585348276285304963292200960 A1 CS103845937170696552570609926584401920 A1 MD103845937170696552570609926584401920

A1 CS207691874341393105141219853168803840 A1 MD207691874341393105141219853168803840 A1 CS415383748682786210282439706337607680 A1 MD415383748682786210282439706337607680 A1 CS830767497365572420564879412675215360 A1 MD830767497365572420564879412675215360 A1 CS1661534994731144841129758825350430720 A1 MD1661534994731144841129758825350430720

A1 CS3323069989462289682259517650700861440 A1 MD3323069989462289682259517650700861440 A1 CS6646139978924579364519035301401722880 A1 MD6646139978924579364519035301401722880 A1 CS13292279957849158729038070602803445760 A1 MD13292279957849158729038070602803445760 A1 CS26584559915698317458076141205606891520 A1 MD26584559915698317458076141205606891520

A1 CS53169119831396634916152282411213783040 A1 MD53169119831396634916152282411213783040 A1 CS106338239662793269832304564822427566080 A1 MD106338239662793269832304564822427566080 A1 CS212676479325586539664609129644855132160 A1 MD212676479325586539664609129644855132160 A1 CS425352958651173079329218259289710264320 A1 MD425352958651173079329218259289710264320

A1 CS850705917302346158658436518579420528640 A1 MD850705917302346158658436518579420528640 A1 CS1701411834604692317316873037158841057280 A1 MD1701411834604692317316873037158841057280 A1 CS3402823669209384634633746074317682114560 A1 MD3402823669209384634633746074317682114560 A1 CS6805647338418769269267492148635364229120 A1 MD6805647338418769269267492148635364229120

A1 CS13611294676837538538534984297270728458240 A1 MD13611294676837538538534984297270728458240 A1 CS27222589353675077077069968594541456916480 A1 MD27222589353675077077069968594541456916480 A1 CS54445178707350154154139937189082913832960 A1 MD54445178707350154154139937189082913832960 A1 CS108890357414700308308279874378165827665920 A1 MD108890357414700308308279874378165827665920

A1 CS217780714829400616616559748756331655331840 A1 MD217780714829400616616559748756331655331840 A1 CS435561429658801233233119497512663310663681680 A1 MD435561429658801233233119497512663310663681680 A1 CS871122859317602466466238995025326621327363360 A1 MD871122859317602466466238995025326621327363360 A1 CS1742245718635204932932477990050653242654726720 A1 MD1742245718635204932932477990050653242654726720

A1 CS3484491437270409865864955980101306485309453440 A1 MD3484491437270409865864955980101306485309453440 A1 CS6968982874540819731729911960202612970618906880 A1 MD6968982874540819731729911960202612970618906880 A1 CS13937965749081639463459823920405225941237813760 A1 MD13937965749081639463459823920405225941237813760 A1 CS27875931498163278926919647840810451882475627520 A1 MD27875931498163278926919647840810451882475627520

A1 CS55751862996326557853839295681620903764951255040 A1 MD55751862996326557853839295681620903764951255040 A1 CS111503725992653115707678591363241807529902510080 A1 MD111503725992653115707678591363241807529902510080 A1 CS223007451985306231415357182726483615059805020160 A1 MD223007451985306231415357182726483615059805020160 A1 CS446014903970612462830714365452967230119610040320 A1 MD446014903970612462830714365452967230119610040320

A1 CS892029807941224925661428730905934460239220080640 A1 MD892029807941224925661428730905934460239220080640 A1 CS1784059615882449851322857461811868920478440161281280 A1 MD1784059615882449851322857461811868920478440161281280 A1 CS3568119231764899702645714923623737840956880322562560 A1 MD3568119231764899702645714923623737840956880322562560 A1 CS7136238463529799405291429847247475681913760645125120 A1 MD7136238463529799405291429847247475681913760645125120

A1 CS14272476927059598810582859694494951827527521290250240 A1 MD14272476927059598810582859694494951827527521290250240 A1 CS28544953854119197621165719388989903655055042580500480 A1 MD28544953854119197621165719388989903655055042580500480 A1 CS57089907708238395242331438777979807310110085161000960 A1 MD57089907708238395242331438777979807310110085161000960 A1 CS114179815416476790484662877555959614620220170322001920 A1 MD114179815416476790484662877555959614620220170322001920

A1 CS228359630832953580969325755111919229240440340644003840 A1 MD228359630832953580969325755111919229240440340644003840 A1 CS456719261665907161938651510223838458480880681288007680 A1 MD456719261665907161938651510223838458480880681288007680 A1 CS913438523331814323877303020447676916961761362576015360 A1 MD913438523331814323877303020447676916961761362576015360 A1 CS1826877046663628647754606040895353833923522725153120030720 A1 MD1826877046663628647754606040895353833923522725153120030720

A1 CS3653754093327257295509212081790707667847045450306240061440 A1 MD3653754093327257295509212081790707667847045450306240061440 A1 CS7307508186654514591018424163581415335694090900612480122880 A1 MD7307508186654514591018424163581415335694090900612480122880 A1 CS14615016373309029182036848327162830671388180801224960245760 A1 MD14615016373309029182036848327162830671388180801224960245760 A1 CS29230032746618058364073696654325661342776361602449920491520 A1 MD29230032746618058364073696654325661342776361602449920491520

A1 CS58460065493236116728147393308651322685552723204899840983040 A1 MD58460065493236116728147393308651322685552723204899840983040 A1 CS116920130986472233456294786617302645371105446409799681966080 A1 MD116920130986472233456294786617302645371105446409799681966080 A1 CS233840261972944466912589573234605290742210892819599363932160 A1 MD233840261972944466912589573234605290742210892819599363932160 A1 CS467680523945888933825179146469210581484421785639198727864320 A1 MD467680523945888933825179146469210581484421785639198727864320

A1 CS935361047891777867650358292938421162968843571278397455728640 A1 MD935361047891777867650358292938421162968843571278397455728640 A1 CS1870722095783555735300716585876842325937687142556794911457280 A1 MD1870722095783555735300716585876842325937687142556794911457280 A1 CS3741444191567111470601433171753684651875374285113589822914560 A1 MD3741444191567111470601433171753684651875374285113589822914560 A1 CS7482888383134222941202866343507369303750748570227179645829120 A1 MD7482888383134222941202866343507369303750748570227179645829120

A1 CS14965776766268445882405732687014738607501497140454359291658240 A1 MD14965776766268445882405732687014738607501497140454359291658240 A1 CS29931553532536891764811465374029477215002994280908718583316480 A1 MD29931553532536891764811465374029477215002994280908718583316480 A1 CS59863107065073783529622930748058954430005988561817437166632960 A1 MD59863107065073783529622930748058954430005988561817437166632960 A1 CS119726214130147567059245861496117908860011977123634874333265920 A1 MD119726214130147567059245861496117908860011977123634874333265920

A1 CS239452428260295134118491722992235817720023954247269748666531840 A1 MD239452428260295134118491722992235817720023954247269748666531840 A1 CS478904856520590268236983445984471635440047908494539497333063680 A1 MD478904856520590268236983445984471635440047908494539497333063680 A1 CS957809713041180536473966891968943270880095816989078994666127360 A1 MD957809713041180536473966891968943270880095816989078994666127360 A1 CS1915619426082361072947933783937886541760191633978157989332254720 A1 MD1915619426082361072947933783937886541760191633978157989332254720

A1 CS3831238852164722145895867567875773083520383267956315978664509440 A1 MD3831238852164722145895867567875773083520383267956315978664509440 A1 CS7662477704329444291791735135751546167040766535912631957329018880 A1 MD7662477704329444291791735135751546167040766535912631957329018880 A1 CS15324955408658888583583470271503092334080533071825263914658037760 A1 MD15324955408658888583583470271503092334080533071825263914658037760 A1 CS30649910817317777167166940543006184668160066143650527829317075520 A1 MD30649910817317777167166940543006184668160066143650527829317075520

A1 CS61299821634635554334333881086012369336320132287301055658634151040 A1 MD61299821634635554334333881086012369336320132287301055658634151040 A1 CS122599643269271108668667762172024738672640264574602111317268302080 A1 MD122599643269271108668667762172024738672640264574602111317268302080 A1 CS245199286538542217337335524344049477345280529149204222634536604160 A1 MD245199286538542217337335524344049477345280529149204222634536604160 A1 CS490398573077084434674671048688098954690561058298408445269073208320 A1 MD490398573077084434674671048688098954690561058298408445269073208320

A1 CS980797146154168869349342097376197909381122116596816890538146416640 A1 MD980797146154168869349342097376197909381122116596816890538146416640 A1 CS1961594292308337738698684194752395818762244233193633781076292833280 A1 MD1961594292308337738698684194752395818762244233193633781076292833280 A1 CS3923188584616675477397368389504791637524488466387267562152585666560 A1 MD3923188584616675477397368389504791637524488466387267562152585666560 A1 CS7846377169233350954794736779009583275048976932774535124305171333120 A1 MD7846377169233350954794736779009583275048976932774535124305171333120

A1 CS15692754338466701909589473558019166550097953865549070248610342666240 A1 MD15692754338466701909589473558019166550097953865549070248610342666240 A1 CS31385508676933403819178947116038333100195907731098140497220685332480 A1 MD31385508676933403819178947116038333100195907731098140497220685332480 A1 CS62771017353866807638357894232076666200391815462196280994441370664960 A1 MD62771017353866807638357894232076666200391815462196280994441370664960 A1 CS125542034707733615276715788464153332400783630924392561988882741329920 A1 MD125542034707733615276715788464153332400783630924392561988882741329920

A1 CS251084069415467230553431576928306664801567261848785123977765482659840 A1 MD251084069415467230553431576928306664801567261848785123977765482659840 A1 CS502168138830934461106863153856613329603134523697570247955530965319680 A1 MD502168138830934461106863153856613329603134523697570247955530965319680 A1 CS1004336277661868922213726307713226659206269047395140495911061930639360 A1 MD1004336277661868922213726307713226659206269047395140495911061930639360 A1 CS2008672555323737844427452615426453318412538094790280991822123861278720 A1 MD2008672555323737844427452615426453318412538094790280991822123861278720

A1 CS4017345110647475688854905230852906636825076189580561983644247722557440 A1 MD4017345110647475688854905230852906636825076189580561983644247722557440 A1 CS8034690221294951377709810461705813273650152379161123967288495445114880 A1 MD8034690221294951377709810461705813273650152379161123967288495445114880 A1 CS16069380442589902755419620923411626547300304758322247934576990890229760 A1 MD16069380442589902755419620923411626547300304758322247934576990890229760 A1 CS32138760885179805510839241846823253094600609516644495869153981780459520 A1 MD32138760885179805510839241846823253094600609516644495869153981780459520

A1 CS64277521770359611021678483693646506189201219033288991738307963560919040 A1 MD64277521770359611021678483693646506189201219033288991738307963560919040 A1 CS128555043540719222043356967387293012378402438066577983476615927121838080 A1 MD128555043540719222043356967387293012378402438066577983476615927121838080 A1 CS257110087081438444086713934774586024756804876133155966953231854243676160 A1 MD257110087081438444086713934774586024756804876133155966953231854243676160

A1 CS514220174162876888173427869549172049513609752266311933906463708487352320 A1 MD514220174162876888173427869549172049513609752266311933906463708487352320 A1 CS1028440348325753776346855739098344099027219504532623867812927416974704640 A1 MD1028440348325753776346855739098344099027219504532623867812927416974704640 A1 CS2056880696651507552693711478196688198054439009065247735625854833949409280 A1 MD2056880696651507552693711478196688198054439009065247735625854833949409280

A1 CS4113761393303015105387422956393376396108878018130495471251709667898818560 A1 MD4113761393303015105387422956393376396108878018130495471251709667898818560 A1 CS8227522786606030210774845912786752792217756036260990942503419335797637120 A1 MD8227522786606030210774845912786752792217756036260990942503419335797637120 A1 CS16455045573212060421549691825573505584435512072521981885006838671595274240 A1 MD16455045573212060421549691825573505584435512072521981885006838671595274240

A1 CS32910091146424120843099383651147011168871024145043963770013677343190548480 A1 MD32910091146424120843099383651147011168871024145043963770013677343190548480 A1 CS65820182292848241686198767302294022337742048290087927540027354686381096960 A1 MD65820182292848241686198767302294022337742048290087927540027354686381096960 A1 CS131640364585696483372397534604588044675484096580175855080054709372762193920 A1 MD131640364585696483372397534604588044675484096580175855080054709372762193920

A1 CS263280729171392966744795069209176089350968192161350171710160109418745524387840 A1 MD263280729171392966744795069209176089350968192161350171710160109418745524387840 A1 CS526561458342785933489590138418352178701936384322700343420320218837491048775680 A1 MD526561458342785933489590138418352178701936384322700343420320218837491048775680

A1 CS1053122916685571866979180276836704357403872768645400686840640437674982097551360 A1 MD1053122916685571866979180276836704357403872768645400686840640437674982097551360 A1 CS2106245833371143733958360553673408714807745537290801373681280875349964195102720 A1 MD2106245833371143733958360553673408714807745537290801373681280875349964195102720

A1 CS4212491666742287467916721107346817429615491075581602747362561750699928390205440 A1 MD4212491666742287467916721107346817429615491075581602747362561750699928390205440 A1 CS8424983333484574935833442214693634859230982151163205494725123501399856780410880 A1 MD8424983333484574935833442214693634859230982151163205494725123501399856780410880

A1 CS16849966666969149871666884429387269718461964302326410989450247002799713560821760 A1 MD16849966666969149871666884429387269718461964302326410989450247002799713560821760 A1 CS33699933333938299743333768858774539436923928604652821978900494005599427121643520 A1 MD33699933333938299743333768858774539436923928604652821978900494005599427121643520

A1 CS67399866667876599486667537717549078873847857209305643957800988011198854243287040 A1 MD67399866667876599486667537717549078873847857209305643957800988011198854243287040 A1 CS134799733335753198973335075435098157747695715418611287915601976022397708486574080 A1 MD134799733335753198973335075435098157747695715418611287915601976022397708486574080

A1 CS269599466671506397946670150870196315495391430837222575831203952044795416973148160 A1 MD269599466671506397946670150870196315495391430837222575831203952044795416973148160 A1 CS539198933343012795893340301740392630990782861674445151662407904089591833946296320 A1 MD539198933343012795893340301740392630990782861674445151662407904089591833946296320

A1 CS1078397866686025591786680603480785261981565722861348890303324815808179183892592640 A1 MD1078397866686025591786680603480785261981565722861348890303324815808179183892592640 A1 CS2156795733372051183573361206961570523963131445722697780606649631616358367785185280 A1 MD2156795733372051183573361206961570523963131445722697780606649631616358367785185280

A1 CS4313591466744102367146722413923141047926263891445395561213299263232716735570370560 A1 MD4313591466744102367146722413923141047926263891445395561213299263232716735570370560 A1 CS8627182933488204734293444827846282095852527782890791122426598526465433471140741120 A1 MD8627182933488204734293444827846282095852527782890791122426598526465433471140741120

A1 CS17254365866976409468586889655692564191705055565781582244853197052930866942281482240 A1 MD17254365866976409468586889655692564191705055565781582244853197052930866942281482240 A1 CS34508731733952818937173779311385128383410111131563164489706394105861733884562964480 A1 MD34508731733952818937173779311385128383410111131563164489706394105861733884562964480

A1 CS69017463467905637874347558622770256766820222263126328979412788211723467769125928960 A1 MD69017463467905637874347558622770256766820222263126328979412788211723467769125928960 A1 CS138034926935811275748695117245540513533640444526252657958825576423446935538251857920 A1 MD138034926935811275748695117245540513533640444526252657958825576423446935538251857920

A1 CS276069853871622551497390234491081027067280889052505315917651152846893871076503715840 A1 MD276069853871622551497390234491081027067280889052505315917651152846893871076503715840 A1 CS552139707743245102994780468982162054134561778105010631835302305693787742152007431680 A1 MD552139707743245102994780468982162054134561778105010631835302305693787742152007431680

A1 CS1104279415486490205989560937964324108269123556210021263671604610387575484304014863360 A1 MD1104279415486490205989560937964324108269123556210021263671604610387575484304014863360 A1 CS2208558830972980411979121875928648216538247112420042527343209220775150968608029726720 A1 MD2208558830972980411979121875928648216538247112420042527343209220775150968608029726720

A1 CS4417117661945960823958243751857296432076494224840085054686418441550301937216059453440 A1 MD4417117661945960823958243751857296432076494224840085054686418441550301937216059453440 A1 CS8834235323891921647916487503714592864152988449681700109373836882903100603874432118906880 A1 MD8834235323891921647916487503714592864152988449681700109373836882903100603874432118906880

A1 CS17668470647783843295832975007429185728305976899363400218747673765806201207748864237760 A1 MD17668470647783843295832975007429185728305976899363400218747673765806201207748864237760 A1 CS35336941295567686591665950014858371456611953798726800437495347531612402415497728475520 A1 MD35336941295567686591665950014858371456611953798726800437495347531612402415497728475520

A1 CS70673882591135373183331900029716742913223907597453600874990695063224804830995456951040 A1 MD70673882591135373183331900029716742913223907597453600874990695063224804830995456951040 A1 CS141347765182270746366663800059433485826447815194907201749981390126449609661990913902080 A1 MD141347765182270746366663800059433485826447815194907201749981390126449609661990913902080

A1 CS282695530364541492733327600118866971652895630389814403499962780252899219323981827804160 A1 MD282695530364541492733327600118866971652895630389814403499962780252899219323981827804160 A1 CS565391060729082985466655200237733943305791260779628806999925560505798438647963655608320 A1 MD565391060729082985466655200237733943305791260779628806999925560505798438647963655608320

A1 CS1130782121458165970933310400475467886611582521559257613999851120101596876295927311216640 A1 MD1130782121458165970933310400475467886611582521559257613999851120101596876295927311216640 A1 CS2261564242916331941866620800950935773223165043118515227999702240203193752591855422432480 A1 MD2261564242916331941866620800950935773223165043118515227999702240203193752591855422432480

A1 CS4523128485832663883733241601901871546446330086237030455999404480406387505183710844960 A1 MD4523128485832663883733241601901871546446330086237030455999404480406387505183710844960 A1 CS9046256971665327767466483203803743092892660172474060911998808960812775010367421689920 A1 MD9046256971665327767466483203803743092892660172474060911998808960812775010367421689920

A1 CS18092513943330655534932966407607486185785320344948121823997617921625550020734843379840 A1 MD18092513943330655534932966407607486185785320344948121823997617921625550020734843379840 A1 CS36185027886661311069865932815214972371570640689896243647995235843251100041469686759680 A1 MD36185027886661311069865932815214972371570640689896243647995235843251100041469686759680

A1 CS72370055773322622139731865630429944743141281379792487295990471686502200082939373519360 A1 MD72370055773322622139731865630429944743141281379792487295990471686502200082939373519360 A1 CS144740111546645244279463731260859889486282562759584974591980943373004400165878747038720 A1 MD144740111546645244279463731260859889486282562759584974591980943373004400165878747038720

A1 CS289480223093290488558927462521719778972565125519169949183961886746008800331757494077440 A1 MD289480223093290488558927462521719778972565125519169949183961886746008800331757494077440 A1 CS578960446186580977117854925043439557945130251038339898367923773492017600663514988154880 A1 MD578960446186580977117854925043439557945130251038339898367923773492017600663514988154880

A1 CS1157920892373161954235709850086879115890260502076679796735847546984035201327029976309760 A1 MD1157920892373161954235709850086879115890260502076679796735847546984035201327029976309760 A1 CS2315841784746323908471419700173758231780521004153359593471695093968070402654059952619520 A1 MD2315841784746323908471419700173758231780521004153359593471695093968070402654059952619520

A1 CS4631683569492647816942839400347516463561042008306719186943390187936140805308119905239040 A1 MD4631683569492647816942839400347516463561042008306719186943390187936140805308119905239040 A1 CS9263367138985295633885678800695032927122084016613438373886780375872281610616239810478080 A1 MD9263367138985295633885678800695032927122084016613438373886780375872281610616239810478080

A1 CS18526734277970591267771357601390065854244168033226876747773560751744563221232479620956160 A1 MD18526734277970591267771357601390065854244168033226876747773560751744563221232479620956160 A1 CS37053468555941182535542715202780131708488336066453753495547121503489126442464959241912320 A1 MD37053468555941182535542715202780131708488336066453753495547121503489126442464959241912320

A1 CS74106937111882365071085430405560263416976672132907506991095242006978252884929919483824640 A1 MD74106937111882365071085430405560263416976672132907506991095242006978252884929919483824640 A1 CS148213874223764730142170860811120526833953344265815013982190484013956505769859838967649280 A1 MD148213874223764730142170860811120526833953344265815013982190484013956505769859838967649280

A1 CS296427748447529460284341721622241053667906688531630027964380968027913011539719677935298560 A1 MD296427748447529460284341721622241053667906688531630027964380968027913011539719677935298560 A1 CS592855496895058920568683443244482107335813377063260055928761936055826023079439355870597120 A1 MD592855496895058920568683443244482107335813377063260055928761936055826023079439355870597120

A1 CS1185710993790117841137366886488964214671626754126520111857523872111652046158878711741194240 A1 MD1185710993790117841137366886488964214671626754126520111857523872111652046158878711741194240 A1 CS2371421987580235682274733772977928429343253508253040223715047744223304092317757423482388480 A1 MD2371421987580235682274733772977928429343253508253040223715047744223304092317757423482388480

A1 CS4742843975160471364549467545955856858686507016506080447430095488446608184635514846964776960 A1 MD4742843975160471364549467545955856858686507016506080447430095488446608184635514846964776960 A1 CS9485687950320942729098935091911713717372014033012160894860190976893216369271029693929553920 A1 MD9485687950320942729098935091911713717372014033012160894860190976893216369271029693929553920

A1 CS18971375900641885458197870183823427434744028066024321789720381953786432738542059387859107840 A1 MD18971375900641885458197870183823427434744028066024321789720381953786432738542059387859107840 A1 CS37942751801283770916395740367646854869488056132048643579440763907572865477084118774775718215680 A1 MD37942751801283770916395740367646854869488056132048643579440763907572865477084118774775718215680

A1 CS75885503602567541832791480735293709738976112264097287158881527815145730954168237549431436321360 A1 MD75885503602567541832791480735293709738976112264097287158881527815145730954168237549431436321360 A1 CS151771007205135083665582961470587419477952224528194574317763055630291461908336475098862872642720 A1 MD151771007205135083665582961470587419477952224528194574317763055630291461908336475098862872642720

A1 CS303542014410270167331165922941174838955904449056389148635526110260583823816672950197725745285440 A1 MD303542014410270167331165922941174838955904449056389148635526110260583823816672950197725745285440 A1 CS607084028820540334662331845882348677911809898112778297271052220521167647633345901900395451490570880 A1 MD607084028820540334662331845882348677911809898112778297271052220521167647633345901900395451490570880

A1 CS1214168057641080669324663691764697355823619796225556594542104441042335295266691803800790902981141760 A1 MD1214168057641080669324663691764697355823619796225556594542104441042335295266691803800790902981141760 A1 CS2428336115282161338649327383529394711647239592451113189084208882084670590533383607601581805962283520 A1 MD2428336115282161338649327383529394711647239592451113189084208882084670590533383607601581805962283520

A1 CS4856672230564322677298654767058789423294479184902226378168417764169341180766767215203163611924567040 A1 MD4856672230564322677298654767058789423294479184902226378168417764169341180766767215203163611924567040 A1 CS9713344461128645354597309534117578846588958369804452756336835528338682361533534430406327223849134080 A1 MD9713344461128645354597309534117578846588958369804452756336835528338682361533534430406327223849134080

A1 CS19426688922257290709194619068235157693177916739608905512673671056677364723067068860812654447698268160 A1 MD19426688922257290709194619068235157693177916739608905512673671056677364723067068860812654447698268160 A1 CS38853377844514581418389238136470315386355833479217811025347342113354729446134137721625309395396536320 A1 MD38853377844514581418389238136470315386355833479217811025347342113354729446134137721625309395396536320

A1 CS77706755689029162836778476272940630772711666958435622050694684226709458892268275443250618790793072640 A1 MD77706755689029162836778476272940630772711666958435622050694684226709458892268275443250618790793072640 A1 CS155413511378058325673556952545881261545423333916871244101389368453418917784536550886501237581586145280 A1 MD155413511378058325673556952545881261545423333916871244101389368453418917784536550886501237581586145280

A1 CS310827022756116651347113905091762523090846667833742488202778736906837835569073101773002475163172290560 A1 MD310827022756116651347113905091762523090846667833742488202778736906837835569073101773002475163172290560 A1 CS621654045512233302694227810183525046181693335667484976404557473813675671139146202203546004950326580480 A1 MD621654045512233302694227810183525046181693335667484976404557473813675671139146202203546004950326580480

A1 CS1243308091024466605388455620367050092363386671334969952809114947627351342278292404407092009900653160960 A1 MD1243308091024466605388455620367050092363386671334969952809114947627351342278292404407092009900653160960 A1 CS2486616182048933210776911240734100184726773342669939905618229895254702684556584808814184019801306321920 A1 MD2486616182048933210776911240734100184726773342669939905618229895254702684556584808814184019801306321920

A1 CS4973232364097866421553822481468200369453546685339879811236459790509405369113169617628368039603612643840 A1 MD4973232364097866421553822481468200369453546685339879811236459790509405369113169617628368039603612643840 A1 CS9946464728195732843107644962936400738907093370679759622472919581018810738226339235256736079207225287680 A1 MD9946464728195732843107644962936400738907093370679759622472919581018810738226339235256736079207225287680

A1 CS19892929456391465686215289925872801477814186741359519244945839162037621476452678470513472158414450575360 A1 MD19892929456391465686215289925872801477814186741359519244945839162037621476452678470513472158414450575360 A1 CS39785858912782931372430579851745602955628373482719038489891678324074043242904957356941026944316901150720 A1 MD39785858912782931372430579851745602955628373482719038489891678324074043242904957356941026944316901150720

A1 CS79571717825565862744861159703491205911256746965438076979783356648148086485809914713882053888633802301440 A1 MD79571717825565862744861159703491205911256746965438076979783356648148086485809914713882053888633802301440 A1 CS159143435651131725489722319406982411822513493930876153959566713296296172971619829427764107777267604602880 A1 MD159143435651131725489722319406982411822513493930876153959566713296296172971619829427764107777267604602880

A1 CS318286871302263450979444638813964823645026987861752307919133426592592345943239658855528215554535209205760 A1 MD318286871302263450979444638813964823645026987861752307919133426592592345943239658855528215554535209205760 A1 CS636573742604526901958889277627929647290053975723504615838266853185184691886479317711056431109070418409520 A1 MD636573742604526901958889277627929647290053975723504615838266853185184691886479317711056431109070418409520

A1 CS1273147485209053803917778555255859294580107951447009231676533706370369383772958635422112862218140836819040 A1 MD1273147485209053803917778555255859294580107951447009231676533706370369383772958635422112862218140836819040 A1 CS2546294970418107607835557110511718589160215902894018463353067412740738766545917270844225724436281673638080 A1 MD2546294970418107607835557110511718589160215902894018463353067412740738766545917270844225724436281673638080

A1 CS5092589940836215215671114221023437178320431805788036926706134825481477533091835434540451448872562347276160 A1 MD5092589940836215215671114221023437178320431805788036926706134825481477533091835434540451448872562347276160 A1 CS10185179881672430431342228442046874356640863611576073853412269650962954066183670869080902897125124694552320 A1 MD10185179881672430431342228442046874356640863611576073853412269650962954066183670869080902897125124694552320

A1 CS20370359763344860862684456884093748713281727223152147706824539301925908132367341738161805794250249389104640 A1 MD20370359763344860862684456884093748713281727223152147706824539301925908132367341738161805794250249389104640 A1 CS40740719526689721725368913768187497426563454446304295413649078603851816264734683476323611589588500498778209280 A1 MD40740719526689721725368913768187497426563454446304295413649078603851816264734683476323611589588500498778209280

A1 CS81481439053379443450737827536374994853126908892608590827298157207703632529469366952647223179176000997556418560 A1 MD81481439053379443450737827536374994853126908892608590827298157207703632529469366952647223179176000997556418560 A1 CS162962878106758886901475655072749989706253817785217181654596414407265059058938733905294446358352001995112837120 A1 MD162962878106758886901475655072749989706253817785217181654596414407265059058938733905294446358352001995112837120

A1 CS325925756213517773802951310145499979412507635570434363309192828814530118117877467810588892716704003990225674240 A1 MD325925756213517773802951310145499979412507635570434363309192828814530118117877467810588892716704003990225674240 A1 CS651851512427035547605902620290999958825015271140868726618385657629060236235754935621177785433408007980451348480 A1 MD651851512427035547605902620290999958825015271140868726618385657629060236235754935621177785433408007980451348480

A1 CS1303703024854071095211805240581999917650030542281737453236771315258120472471509871242355570866816015960902696960 A1 MD1303703024854071095211805240581999917650030542281737453236771315258120472471509871242355570866816015960902696960 A1 CS2607406049708142190423610481163999835300061084563474906473542630516240944943019742484711141733632031921805393920 A1 MD2607406049708142190423610481163999835300061084563474906473542630516240944943019742484711141733632031921805393920

A1 CS5214812099416284380847220962327999670600122169126949812947085261032481889886039484969422283467264063843610787840 A1 MD5214812099416284380847220962327999670600122169126949812947085261032481889886039484969422283467264063843610787840 A1 CS10429624198832568761694441924655999341200244338253899625894170522064963779772078969938844566934528127687221575680 A1 MD10429624198832568761694441924655999341200244338253899625894170522064963779772078969938844566934528127687221575680

A1 CS20859248397665137523388883849311998682400488676507799251788341044129927559544157939877689133869056255374443151360 A1 MD20859248397665137523388883849311998682400488676507799251788341044129927559544157939877689133869056255374443151360 A1 CS41718496795330275046777767698623997364800977353015598503576682088259855119088315879755378267738112510748886302720 A1 MD41718496795330275046777767698623997364800977353015598503576682088259855119088315879755378267738112510748886302720

A1 CS83436993590660550093555535397247994729601954706031197007153364176519710238176631759510756535476225021497772605440 A1 MD83436993590660550093555535397247994729601954706031197007153364176519710238176631759510756535476225021497772605440 A1 CS166873987181321100187111070794495989459203909412062394014306728353039420476353263519021513070952450042995545210880 A1 MD166873987181321100187111070794495989459203909412062394014306728353039420476353263519021513070952450042995545210880

A1 CS333747974362642200374222141588991978918407818824124788028613456706078840952706527038043026141904900085991090421760 A1 MD333747974362642200374222141588991978918407818824124788028613456706078840952706527038043026141904900085991090421760 A1 CS667495948725284400748444283177983957836815637648249576057226913412157681905413054076086052283809800171982180843520 A1 MD667495948725284400748444283177983957836815637648249576057226913412157681905413054076086052283809800171982180843520

A1 CS1334991897450568801496888566355967915673631275296499152114453826824315363810826108152172104567619600343964361687040 A1 MD1334991897450568801496888566355967915673631275296499152114453826824315363810826108152172104567619600343964361687040 A1 CS2669983794901137602993777132711935831347262550592998304228907653648630727621652216304344209135239200687928723374080 A1 MD2669983794901137602993777132711935831347262550592998304228907653648630727621652216304344209135239200687928723374

INTERDATA®

SHIFTER & ALU

B080 IIS5 · CRY0 S1 · B010 IIS2 · B000 IIS1 · SHCA 12B9 · SHC8 12C9 · B090 IIS5 · B020 IIS2 · B100 IIS5 · B030 IIS2 · B110 IIS5 · B040 IIS3 · B120 IIS7 · B050 IIS3 · B060 IIS3 · B130 IIS7 · B070 IIS3 · B150 IIS7 · B140 IIS7

15R1, DIV1 13J9 · SRL001 · 15J9, 16B1 CRY0 A1, 15A2

A82 19-016 HG · A79 19-016 HG · A100 19-037 SG

A28 19-038 · DUAL 4 LINE TO 1 LINE DATA SELECTOR A27 19-038 · A26 19-038 · A25 19-038 · A24 19-038 · A35 19-038 · A36 19-038 · A37 19-038

GB000 237-0 · SUB0 13K5

M1 · S01 · S11 · S21 → 13K5, 13H5, 13J5, 13J5

A105 19-029 HG · S6 C11 · E6 CG471 · E6 CP471 · C11 · J6 CG811 · J6 CP811 · M6 CG251 · M6 CP251

GA030 12D5 · GA020 12C5 · GA010 12B5 · GA000 12A5 · GB000 · GB010 · GB020 · GB030

4 BIT ALU A23 19-039 (B3, B2, B1, B0; A3, A2, A1, A0; P, G, F3, F2, F1, F0; CN, S0, S1, S2, S3, A=B)

CP031 · CG031

A57 19-040 · 13K5 DOC0 · 10B1 RD030 · 15A2 RD141 · 15A2 FLR121

A99 19-018 HG

GB040 · GB050 · GB060 · GB070 · GA040 12E5 · GA050 12F5 · GA060 12F5 · GA070 12G5 · A6 CP471 · A6 CG471 · A34 19-039

GB080 · GB090 · GB100 · GB110 · GA080 12H5 · GA090 12J5 · GA100 12K5 · GA110 12L5 · B6 CPB11 · B6 CGB11 · A45 19-039

GB120 · GB130 · GB140 · GB150 · GA120 12M5 · GA130 12N5 · GA140 12R5 · GA150 12R5 · B6 CP251 · B6 CG251 · A56 19-039

C11 A5

A45 VM-P5 1K · A46 VM-P5 1K · A47 VM-P5 1K · A48 VM-P5 1K · A49 VM-P5 1K

FRNS1 202-1

A49 19-015 HG: 01, 03, 05, 07, 09, 11, 13 · A48 19-015 HG: 01, 03, 05, 07, 09, 11, 13 · A47 19-015 HG: 01, 03, 05, 07, 09 · A46 19-050 HG: 01, 02, 08

11A3 S000 · 12A1 S001 · 11A3 S010 · 12B1 S011 · 11A3 S020 · 12C1 S021 · 11A3 S030 · 12D1 S031 · CSV1 228-1 · 15R1

11A5 S040 · 12E1 S041 · 11A5 S050 · 12F1 S051 · 11A5 S060 · 12G1 S061 · 11A5 S070 · 12G1 S071 · 11A7 S080 · 12H1 S081 · 11A7 S090 · 12J1 S091 · 11A7 S100 · 12K1 S101 · 11A7 S110 · 12L1 S111 · 11A9 S120 · 12M1 S121 · 11A9 S130 · 12N1 S131 · 11A9 S140 · 12R1 S141 · 11A9 S150 · 12S1 S151 · CTF1 103-1

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-389 ALU BOARD.

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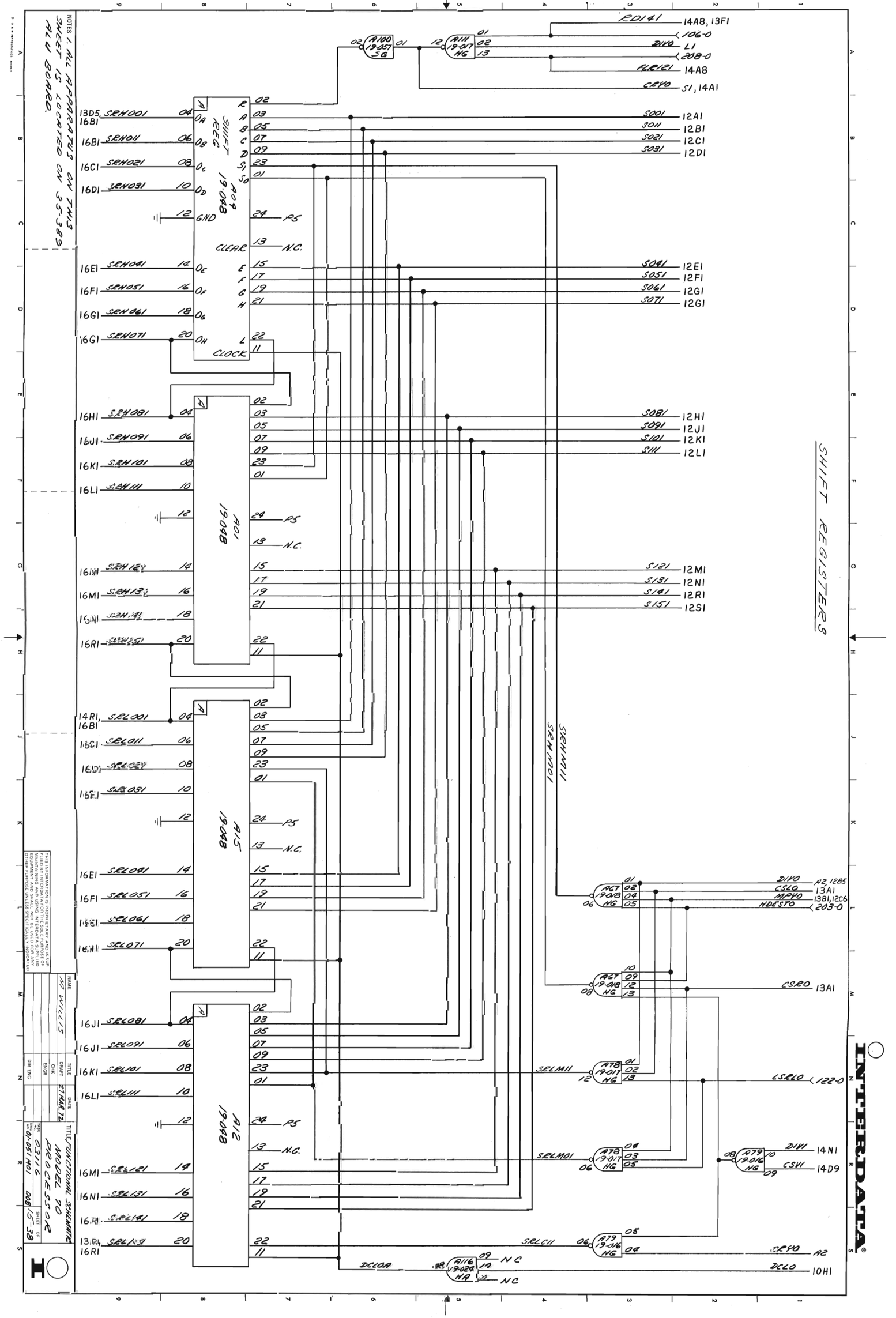
NAME	TITLE	DATE
L VALENTY	DRAFT	27 MAR 72
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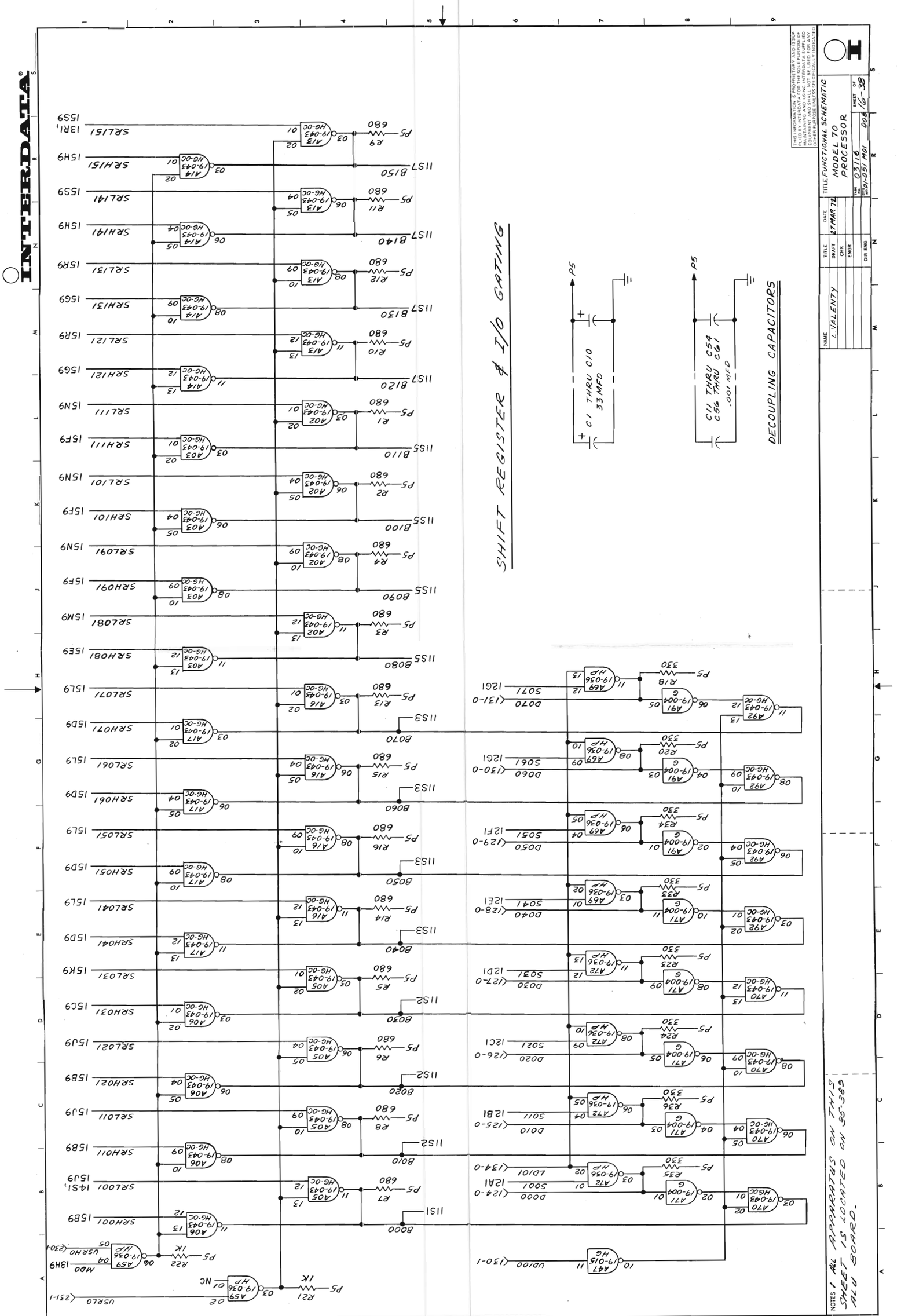
TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO. 03116 · TYPE NO. 01-051M01 D08 · SHEET 14 OF 38

ALU

BRUNING 44231 15043


NOTES: 1. ALL TERMINATORS ON THIS SHEET IS LOCATED ON 35-389 ALU BOARD.
SHIFT REGISTERS
SRHM01
SRHM11
SELM11
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SRL001
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A10 19-057-3G
A11 19-047 HG
A12 19-048
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A14 19-048
A15 19-048
A16 19-024 HA
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A18 19-011 HG
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A1299 19-017 HG
A1300 19-018 HG
A1301 19-016 HG
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A1497 19-016 HG
A1498 19-011 HG
A1499 19-017 HG
A1500 19-018 HG
A1501 19-016 HG
A1502 19-016 HG
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A1504 19-016 HG
A1505 19-016 HG
A1506 19-016 HG
A1507 19-016 HG
A1508 19-011 HG
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A1510 19-018 HG
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A1513 19-016 HG
A1514 19-016 HG
A1515 19-016 HG
A1516 19-016 HG
A1


INTERDATA
SHIFT REGISTER & I/O GATING
DECOUPLING CAPACITORS
C1 THRU C10
33 MFD
C11 THRU C54
C56 THRU C61
.001 MFD
P5
TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR
DWG 03116
SHEET 16 OF 38
NAME L VALENTY
DATE 27 MAR 72
NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 30-339 I/O BOARD.

INTERDATA®

FLAGS AND ALARM REGISTERS

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD.

REVISIONS	
LOC K6 ADDED R110 & L2 BGW1 1924 9-25-73 R01	N2 & S3 A41 WAS 19-015 (6 PLACES) BGW1 1926 9-25-73 R02
LOC D4 & F4, R34, R35 & R37 WERE 1K, LOC H2 & M2 A66 WAS 19-043 3 PLACES, LOC K3, M3	

NAME	TITLE	DATE
N. WILLIS	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO. 05116 SHEET OF 17-38

DWG NO. 01-051 M01 ROR2D08

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BRUNING 44-231 15043

INTERDATA®

A131 19-026

A121 19-026

A132 19-026

TEST AND BRANCH

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD.

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NAME	TITLE	DATE
E. ROE	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116 SHEET OF
DWG NO. 01-051M01 008 18-38

BRUNING 44.231-5043

INTERDATA®

PPF CIRCUIT

SEE NOTE 2

12 VAC

139-1

239-1

107-3 INITOA

101-3 INITO

105-3 PDFFO

DISPLAY

PFDTO

POWDNO

PFDI

SCLR20

SCLR17

SCLR08

CLKSTPO

CLKSTPI

TF80

TFA1

TFB1

STPSYS1

STPSYS0

P.P.F. AND CLOCKS

REVISIONS
ADDED CONN 107-3 LOC A4
E-M RC V699 1/27/73 E08
LOC J7 DELETED GATE A129, OUTPUT PIN 8 (NC)
BG RM 2008 4/14/74 R10
NOTE 2 ADDED, CORRESP. ASTERISK WERE NOT SPEC.
J-H JCH 2/21/75 6-10-76 R11

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD.
2. * = USED ON F00 VARIATION ONLY.

CHG LOC C5 C10 & C16 W/AS 470 PF
E-M E 5748 11/4 10/19/72 E02
LOC B8 R32 WAS 1.5K
LOC R9 R17 WAS 1K
BG RM2 1924 4/14 9-25-73 R09

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NAME	TITLE	DATE
E. ROE	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 01-057, M01, R11
SHEET OF 19-38

© D & W REPROGRAPHICS 40058.4

INTERDATA®

I/O GATING

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD.

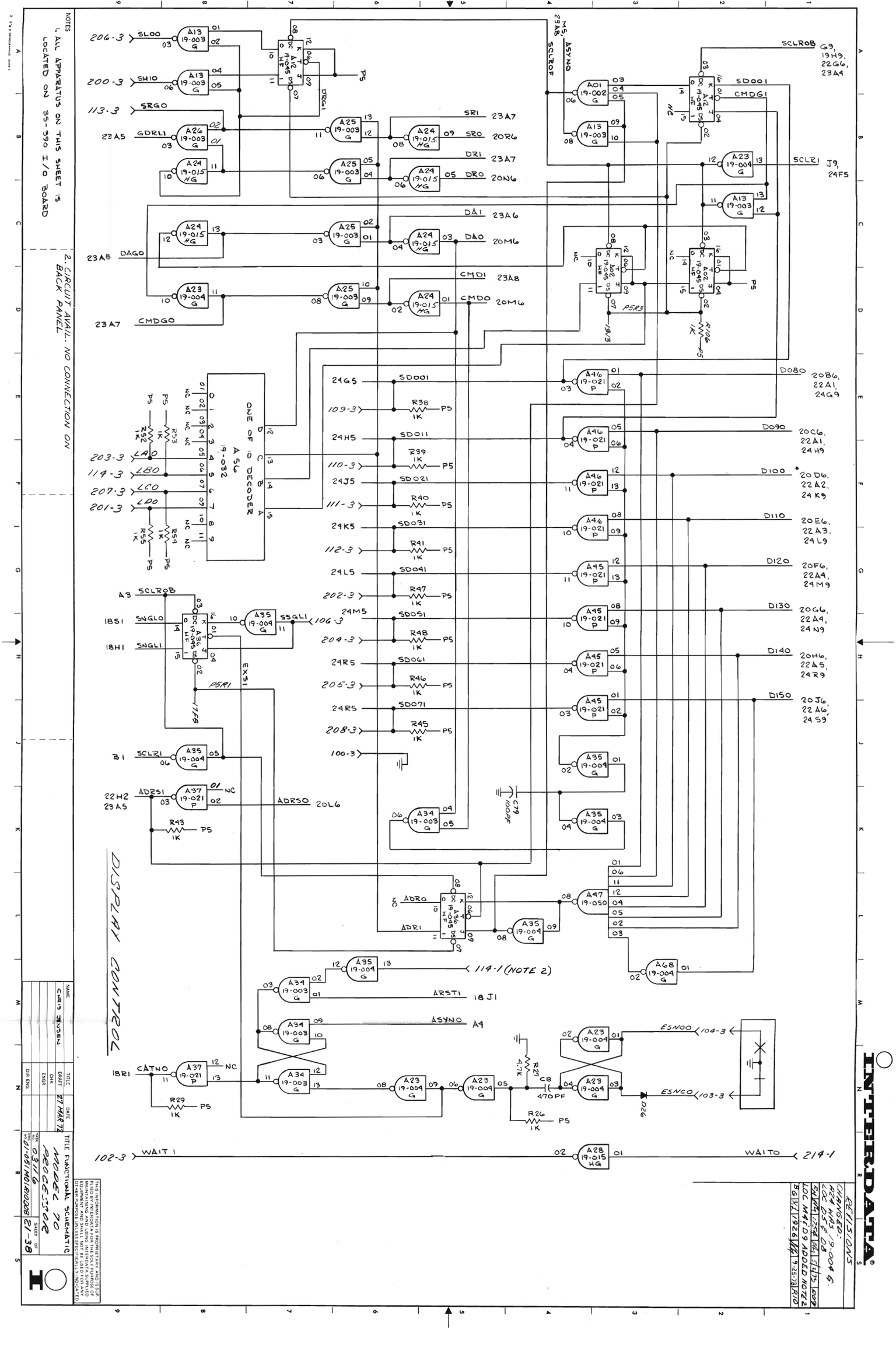
REVISIONS
LOC L4-R4 A76, AB7, AB8 WERE 19-055, DELETED IK RES FROM OUTPUT OF SAME
BG RJ 1554 RO3

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 01-051, M01, R03008
SHEET 20 OF 38

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BRUNING 44-231 13043


NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD
2. CIRCUIT AVAIL. NO CONNECTION ON BACK PANEL
DISPLAY CONTROL
ONE OF 10 DECODER A 56 19-032
SDO001
SDO011
SDO021
SDO031
SDO041
SDO051
SDO061
SDO071
D080
D090
D100
D110
D120
D130
D140
D150
SCLR0B
SCLR1
ADR0
ADR1
ADRS0
ADRS1
ARST1
ASYNO
WAIT1
WAIT0
ESNO0
ESNC0
CMDG1
DR1
SR1
DA1
CMD1
R38 1K
R39 1K
R40 1K
R41 1K
R97 1K
R48 1K
R46 1K
R45 1K
R43 1K
R29 1K
R26 1K
R27 4.7K
C8 470 PF
C79 .0005F
D26
NAME CHRIS JENSEN
DRAFT
DSGN
ENGR
DIR ENG
DATE 27 MAR 74
TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
DWG NO 03116-01-05 M01 REV 008
SHEET 21-38
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INTERDATA
REVISIONS
CHANGED: 19-004 &
DOC MAY 09 ADDED NOTE 2

INTERDATA®

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TTY

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD

NAME	TITLE	DATE	TITLE
L. VALENTY	DRAFT	27 MAR 72	FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03116 DWG NO. 01-051 M01 SHEET OF 22-38

D & W REPROGRAPHICS 40055-4

0022

P5 R44 10K C11 .15uF
P5 RG3 10K R49 10K C12 .15uF
P5 R50 2.2K C13 470PF R51 3.3K
A48 19-031 A59 19-031 R57 1K P5
TP1 NC
A60 19-004 G
22A9 TMGO
22F8 DDO
A78 19-004 G DDI
A61 19-003 G
A50 19-003 G SRDYO EOC1 H6
S7 EOCO
A39 19-004 G
A6 TDAGO
A60 19-004 G
A39 19-004 G TDAG1
A50 19-003 G RDY1 RDY0 22A9
A61 19-003 G ASTO
A60 19-004 G ASTI
A61 19-003 G
C14 470PF
P5 R11 1K
19H9, 21A1, 22G6 SCLROB
A50 19-003 G
22A9 DDOA
C78 470 PF
A39 19-004 G STO
K T J DC A19 DS 19-019 1
K 19-045 V DC TMG DS 0 A49 1 TMG1
TMGO
24D1 DDI
A39 19-004 G DDOA
NC CLK1 C11
21B9 GDRL1 (DSPLY)
A39 19-004 G GDRLO
A38 19-003 G ADRSBI 24H5
22AB TMGI
K 19-014 V DC A14 DS 0 1 N.C.
A15 19-001 G READ TDRO
A60 19-004 G
22J1 ADMHI
21K9, 22H2 ADRS1 (DSPLY)
A38 19-003 G ASYNOA (TTY)
ATSYNO 22A6 24A9
A38 19-003 G ADRSAI 24G5
DRGOA 22G3
P5 R12 1K
C3 EOC1
22R1 BRKOA
A106 19-003 G
A67 19-003 G
A03 19-021 P LBB1 22K2 24G1
C7 470 PF
A67 19-003 G
A01 19-002 G DAGOA
A3 TDAGO
21C5 DA1
21B5 DR1
A26 19-003 G DRGOA
A27 19-001 G STRBI
A37 19-021 P STRBO 24G5
N.C.
R28 1K P5
P5 R15 1K
A04 19-003 G CLSRO 24D1
INPUTS A B C D OUTPUTS A B C D
19-035 A16
NC CNT DWN CARRY EOCO A3
CNT LOAD CLEAR BORROW NC
4-BIT COUNTER
21B5 SRI
A26 19-003 G SRGOA
21D9 CMDGO (DSPLY)
22K1 ADI
21D5 CMDI
24D1 CMDGOA
A27 19-001 G SYNI
A37 19-021 P SYNO (230-0
ASYNOA (TTY)
A61 19-003 G
A60 19-004 G
DAGOA 24E1
TTY
21C9 DAGO (DSPLY)
21A9 ASYNO (DSPLY)
A01 19-002 G
A39 19-004 G
2254 READO
2256 TMGIA
24D1, 2256 READI
22N2 BSYIA
A67 19-003 G
A78 19-004 G BSYI 24M5

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NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD

NAME	TITLE	DATE
L. VALENTY	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR. ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR
TASK NO 03116
DWG NO 01-051 M01 008
SHEET 23 OF 38

© D & W REPROGRAPHICS 40056-4

INTERDATA®

TTY

A116 19-030 4 BIT SHIFT REG.

A126 19-030 4 BIT SHIFT REG.

A93 19-038 DUAL 4/1 MUX

A104 19-038 DUAL 4/1 MUX

A92 19-038 DUAL 4/1 MUX

A103 19-038 DUAL 4/1 MUX

C17 100 PF

C19 470 PF

R82 1K

R83 3.3K

C23 THRU C31 33MFD

C32 THRU C73 .001 MFD C80 THRU C95

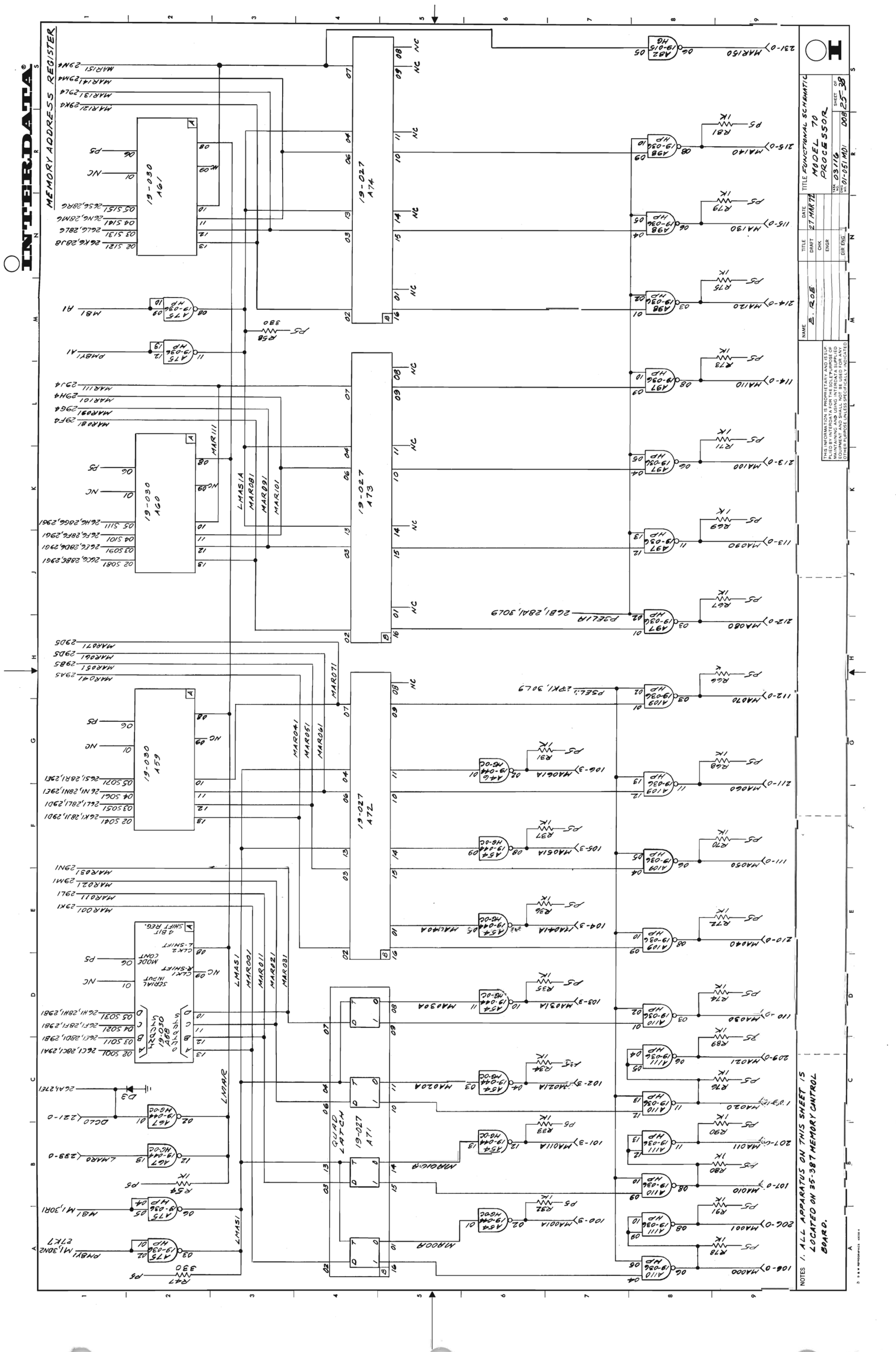
DECOULPING CAPACITORS

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD

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NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	27 MAR 72
	CHK	
	FNGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 01-051 H01 008
SHEET 24 OF 38


INTERDATA
MEMORY ADDRESS REGISTER
TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR
DATE 27 MAR 72
DATE 03/16
SHEET 25 OF 38
NAME E. ROE
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NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 85-387 MEMORY CONTROL BOARD.

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NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-387 MEMORY CONTROL BOARD

CHG.: LOC FS SHT REF FOR MDR021 WAS 29L1.
REMOVED: SHT LOC FOR MDRCLRO LOC.C1.
EH RJ 1/3 5 4 10 6 1 10 19 72 1803

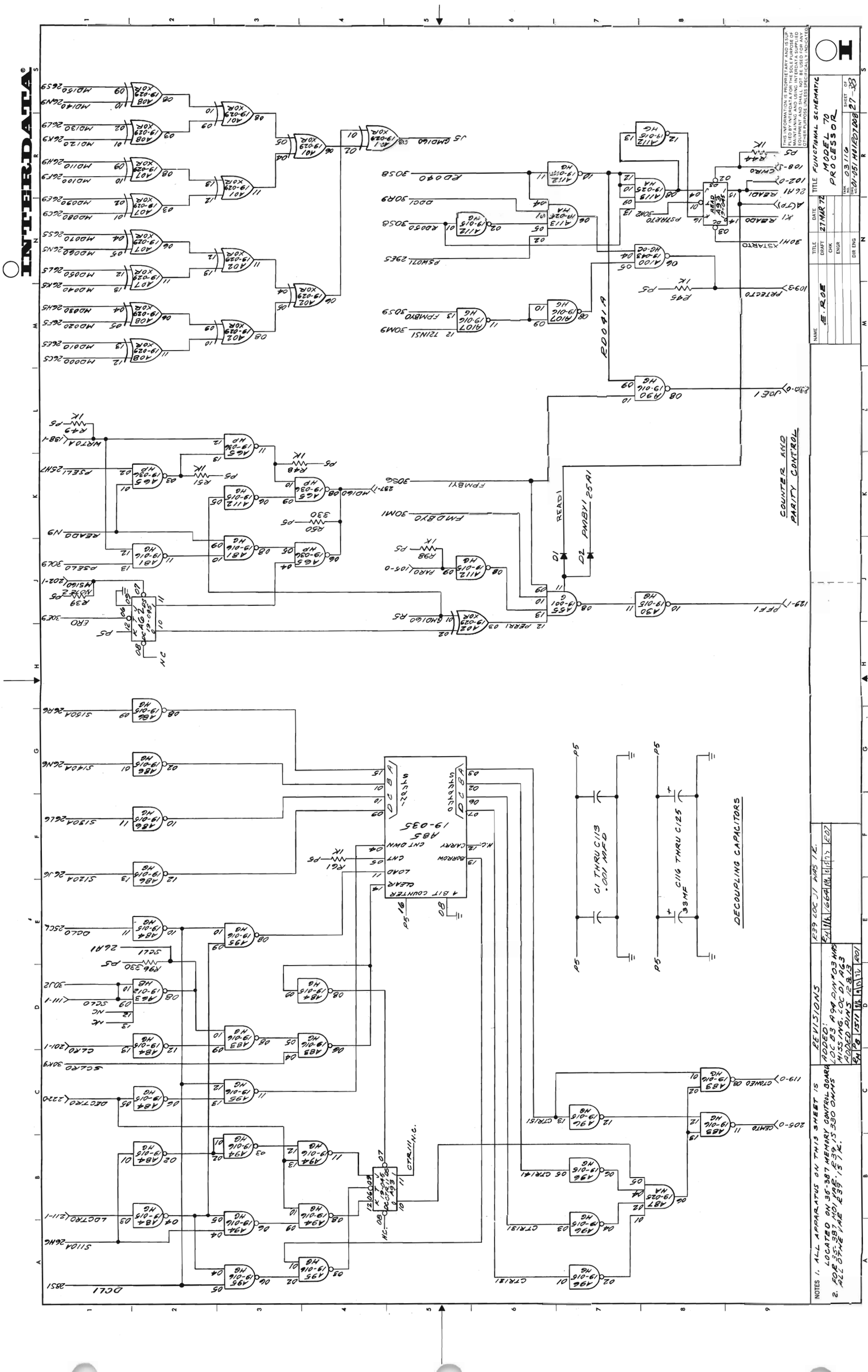
NAME	TITLE	DATE
L. VALENTY	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

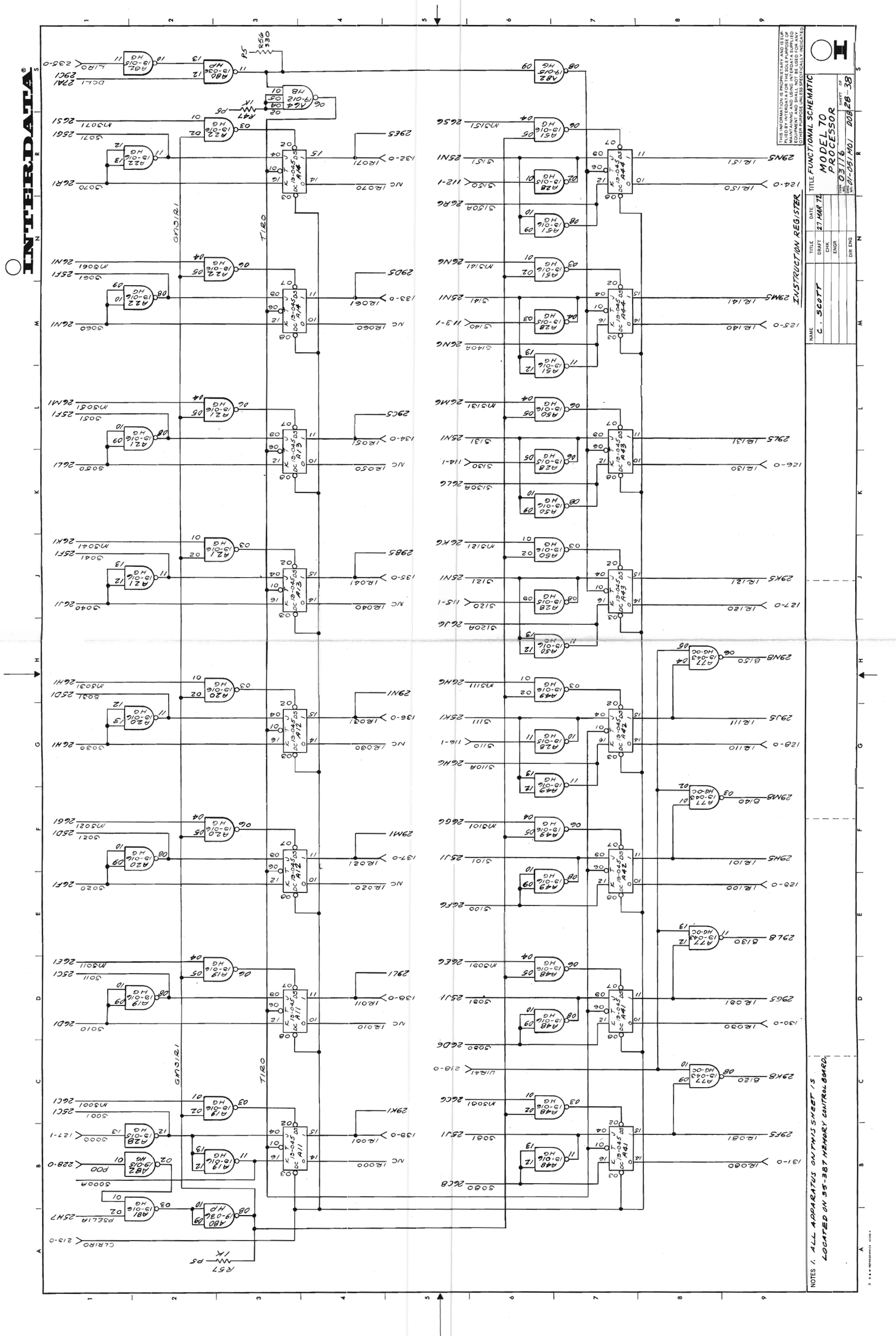
TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-051 M01 RD3308
SHEET 26-38

MEMORY DATA REGISTER

BRUNING 44 231 15043


INTERDATA
MODEL 70
PROCESSOR
FUNCTIONAL SCHEMATIC
COUNTER AND PARITY CONTROL
DECOUPLING CAPACITORS
C1 THRU C113 .001 MFD
C114 THRU C125 33 MF
A85 19-035
4 BIT COUNTER
REVISIONS
NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 32-387 MEMORY CONTROL BOARD
2. FOR 32-387 NO. E38, E39, E39/5 USE 330 OHMS AT OTHER LOC E39


INTERDATA
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NAME C. SCOTT
DATE 27 MAR 72
DRAFT
CHK
ENGR
DIR ENG
TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
DWG NO 03776
SHEET OF
ECO NO 01-05110 01
INSTRUCTION REGISTER
NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 55-387 MEMORY CONTROL BOARD.

INTERDATA®

A56
19-030
4 BIT SHIFT REGISTER
INPUTS A B C D
MODE CONT
SERIAL INPUT
OUTPUTS A B C D
CLK 1 R SHIFT
CLK 2 L SHIFT

A47
19-030

A57
19-030

A09
19-038

A10
19-038

A17
19-038
DUAL 4 LINE TO 1 LINE DATA SELECTOR

A18
19-038

A31
19-038

A32
19-038

A39
19-038

A40
19-038

A66
19-026

PSW031
PSW021
PSW011
PSW001

PJW AND B BUS GATING

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NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-387 MEMORY CONTROL BOARD.

REVISIONS

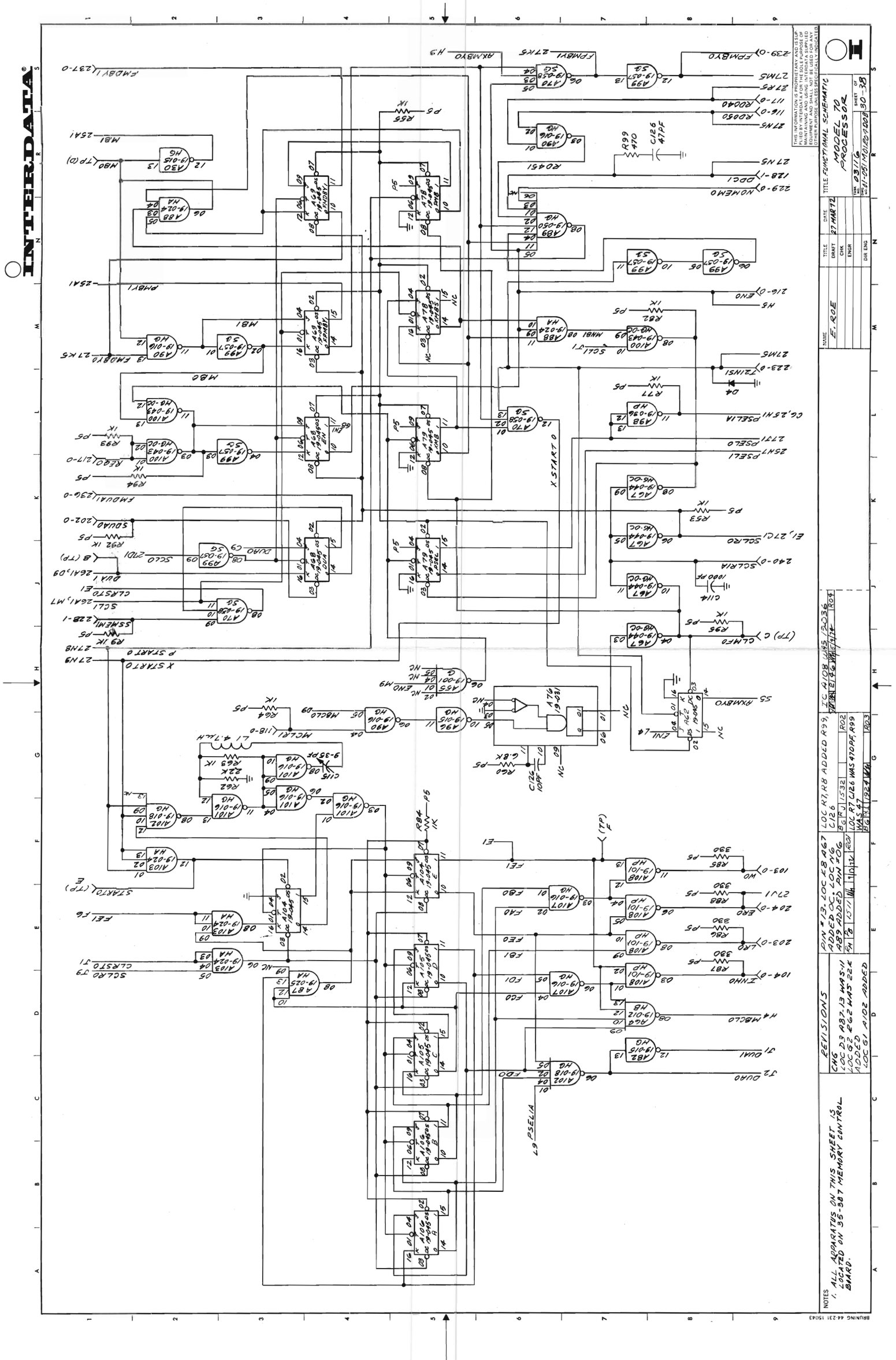
CHG LOC C8 A25-13 WAS-03 ADDED: LOC F1 A26 ADDED "OC." RM PA 5/11 WG 7/0/72 E01

CHG: LOC C2 IC A88-12, 01, 02, 13 WAS 08, 09, 10 11 RESP. RM RJ 5/48 WG 10/9/72 E02

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	27 MAR 72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR

TASK NO. 03116
DWG NO. 01-051 MAI ED2 008
SHEET 29 OF 38


INTERDATA
MODEL 70
PROCESSOR
TITLE FUNCTIONAL SCHEMATIC
SIZE D
SHEET 23 OF 30
DWG NO 91-05101-01
REVISIONS
NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 85-587 MEMORY CONTROL BOARD.
BRUNING 44-231 15043

INTERDATA®

MOD 70 ROM
35-388M02

A65 A76 A77 A78 A79 A80
R44 R45 R46 R47 R48 R49 R50 R51
C42
A86 A87 A88 A89 A90
C43
A81 A82 A83 A84 A85 A96 A97 A98 A99 A100
C44 C45 C46 C47 C48 C49 C50 D1 R52 C51 C52
A91 A92 A93 A94 A95 A106 A107 A108 A109 A110
C10
R53
A111 A112 A113 A114 A116 A117 A118 A119 A120
C53 C54 R61 C55 C56 C57 R54 C58 R56 R57
A121 A122 A123 A124 A125 A126 A127 A128 A129 A130
C61 C62
A141 A135
C59
R58 R59 R60
A131 A132 A133 A134 A136 A137 A138 A139 A140
R62
C60
C5 C6 C7 C8
CONNECTOR 0

RON 35-388M02

SEE SHT 31A

COMPONENT	REFERENCE DESIGNATION
CAPACITOR	C1 THRU C62
DIODE	D1
I.C.	A01 THRU A05, A06 THRU A60, A65 THRU A70, A76 THRU A100, A106 THRU A114, A116 THRU A141
RESISTOR	R1 THRU R62

BY THRU 35-388-403
PER ECN NO. 7604
BY RHM DATE 12/12/72

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NOTES

NAME	TITLE	DATE
P.EDWARDS	DRAFT	7-28-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-051M01 REV008
SHEET 31 OF 38

BRUNING 44-231 16042

INTERDATA®

MOD 70 ROM
35-388 M03

A76 A77 A78 A79 A80
A86 A87 A88 A89 A90
A83 A84 A85 A96 A97 A98 A99 A100
A91 A92 A93 A94 A95 A106 A107 A108 A81 A109 A110
A111 A112 A113 A114 A116 A117 A118 A82 A119 A120
A121 A122 A123 A124 A125 A126 A127 A128 A141 A129 A130
A145 A135 A136 A137 A138 A139 A140
A131 A132 A133 A134

R44 R45 R46 R47 R48 R49 R50 R51
C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 R52 D1 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 C10

CONNECTOR 0

C5 C6 C7 C8

ROM 35-388 M03

COMPONENT	REFERENCE DESIGNATION
CAPACITOR	C1 THRU C62
DIODE	D1
I. C.	A01 THRU A04, A06 THRU A60, A65 THRU A70, A76 THRU A100, A106 THRU A114, A116 THRU A140, A142 THRU A145
RESISTOR	R1 THRU R62

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NOTES

NAME	TITLE	DATE
B GRAY	DRAFT	10-25-72
R CERO	CHK	11-7-72
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03024
DWG NO. 01-051M01 D08
SHEET 36 OF 38

BRUNING 44-231 16042

INTERDATA®

MOD 70 ROM
35-388M02

C1 C2 C3 C4

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43

C9 C11 C12 C13 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41

A01 A02 A03 A04 A06 A07 A08 A09 A10
A11 A12 A13 A14 A15 A16 A17 A18 A19 A20
A21 A22 A23 A24 A25 A26 A27 A28 A29 A30
A31 A32 A33 A34 A35 A36 A37 A38 A39 A40
A41 A42 A43 A44 A45 A46 A47 A48 A49 A50
A51 A52 A53 A54 A55 A56 A57 A58 A59 A60
A66 A67 A68 A69 A70

SUPPLIED
BY PART NO. 35-388M03SMT32A
PER ECN NO. 1604
BY RHM DATE 12-12-72

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ROM 35-388M02

NOTES

NAME	TITLE	DATE
EDWARDS	DRAFT	7-28-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-051M01R04 DOB
SHEET 32 OF 39

BRUNING 44-231 16042

INTERDATA®

MOD 70 ROM
35-388 M03

C1 C2 C3 C4

R1 R2 R3 R4 R5 R6 R7 R8 R14 R39 R43 R9 R18 R11 R10 R41

A01 A02 A03 A04 A06 A07 A08 A09 A10

A11 A12 A13 A14 A15 A16 A17 A18 A19 A20

A21 A22 A23 A24 A25 A26 A27 A28 A29 A30

A31 A32 A33 A34 A35 A36 A37 A38 A39 A40

A41 A42 A43 A44 A45 A46 A47 A48 A49 A50

A51 A52 A53 A54 A55 A56 A57 A58 A59 A60

A65 A66 A67 A68 A69 A70

C9 C11 C12 C13 C14 R13 R12 C26 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 R15 C25 C27 C28 R16 R17 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 R40 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 C39 C41 R42 C40

CONNECTOR 1

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ROM 35-388 M03

NOTES

NAME	TITLE	DATE
B GRAY	DRAFT	10-25-72
R CERO	CHK	11-7-72
	ENGR	
	DIR ENG	

TITLE: MODEL 70 PROCESSOR

TASK NO 03024 DWG NO 01-051 M01 008 SHEET 32 OF 38

BRUNING 44-231 6042

INTERDATA®

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ALU
35-389 M01

A56 A57 A58 A59 A63 A64 A65 A66
A67 A69 A70 A71 A72 A74 A75 A76 A77
A78 A79 A81 A82 A83 A84 A85 A86 A87 A88
A89 A90 A91 A92 A93 A94 A95 A96 A98 A99
A100 A101 A102 A103 A104 A105 A106 A107 A108 A109 A110
A111 A112 A113 A114 A115 A116 A117 A118 A119 A120 A121

C6 C7 C8 C9 C10

CONNECTOR O

ALU 35-389M01

COMPONENT	REFERENCE DESIGNATION
CAPACITOR	C1 THRU C61
RESISTOR	R1 THRU R49
I.C.	A01 THRU A59, A63 THRU A69, A74 THRU
	A72, A74 THRU A75, A81 THRU 2
	A98 THRU A121

NOTES

NAME	TITLE	DATE
P.EDWARDS	DRAFT	8-1-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-05117M01 REV B
SHEET 33 OF 38

BRUNING 44-231 16042

INTERDATA®

ALU
35-389M01

C1 C2 C3 C4 C5

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R45 R46 R47 R110

C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30

L2

A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11
A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22
A23 A24 A25 A26 A27 A28 A29 A30 A31 A32 A33
A34 A35 A36 A37 A38 A39 A40 A41 A42 A43 A44
A45 A46 A47 A48 A49 A50 A51 A52 A53 A54 A55

CONNECTOR J

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NOTES

REVISIONS			
LOC N7 ADDED R110 & L2			
BG	KJ	1924	9-25-73 R01

ALU 35-389M01

NAME	TITLE	DATE	TITLE: FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
REDWARDS	DRAFT	8-1-72	
	CHK		
	ENGR		
	DIR ENG		TASK NO 03116
			DWG NO 01-05TM01/R01008
			SHEET 34 OF 38

BRUNING 44 231 16042

INTERDATA®

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I/O 35-390M02

A67 A68 A69 A70 A71 A72 A73 A74 A75 A76 A77

A78 A79 A80 A81 A82 A83 A84 A85 A86 A87 A88

A89 A90 A91 A92 A93 A94 A95 A96 A97 A98 A99

A100 A101 A102 A103 A104 A105 A106 A107 A108 A109 A110

A111 A112 A113 A114 A115 A116 A117 A118 A119 A120 A121

A122 A123 A124 A125 A126 A130 A131 A132

R63 Baud rate potentiometer

C59 C61 C62 C12 R64 C63 R105

R108 C64 R67 R68 R69 R70 R71 R72 R73 R74 C65 R102 R75 C77 C66

CONNECTOR 2

R89 R90 R91 D20 R92 R93 R94 D21 D22 R95 C21 R96 R97 D23 D24 R98 D25 C22 R99 R100 R101

Q7 Q8

D14 R81 D15 C67 C18 C68 R82 C19 C94 R83 C69 C70 C71 C72

R84 R85 R86 D16 D17 D18 D19 R76 C73 C80 C81 C82 R87

D12 R104 C20 C86 R109 C87 C88 C89 C90 C91 R88 C92 C93

C28 C29 C30 C31

CONNECTOR 0

I/O 35-390M02

COMPONENT	REFERENCE DESIGNATION
CAPACITOR	C1 THRU C73, C77 THRU C95
RESISTOR	R1 THRU R9, R11 THRU R58, R60 THRU R110
DIODES	D1 THRU D26
TRANSISTORS	Q1 THRU Q8
CHOKE	L1, L2
RELAY	K1
I.C.	A01 THRU A126, A130 THRU A132

NOTES

REVISIONS	REF. DESIG. ADDED L2
DELETED 6 1K RESISTORS 2 UNDER A76, 2 UNDER A87, 2 UNDER A88	RES. WERE R60 THRU R109
B G WH 1924 11/4 9-25-78 R04	
LOC K7 DELETED I.C. A129	
B G RJ 1554 11/4 10 19 72 R03	

NAME	TITLE	DATE
PEDWARDS	DRAFT	8-1-72
	CHK	
	ENGR	
	DIR ENG	

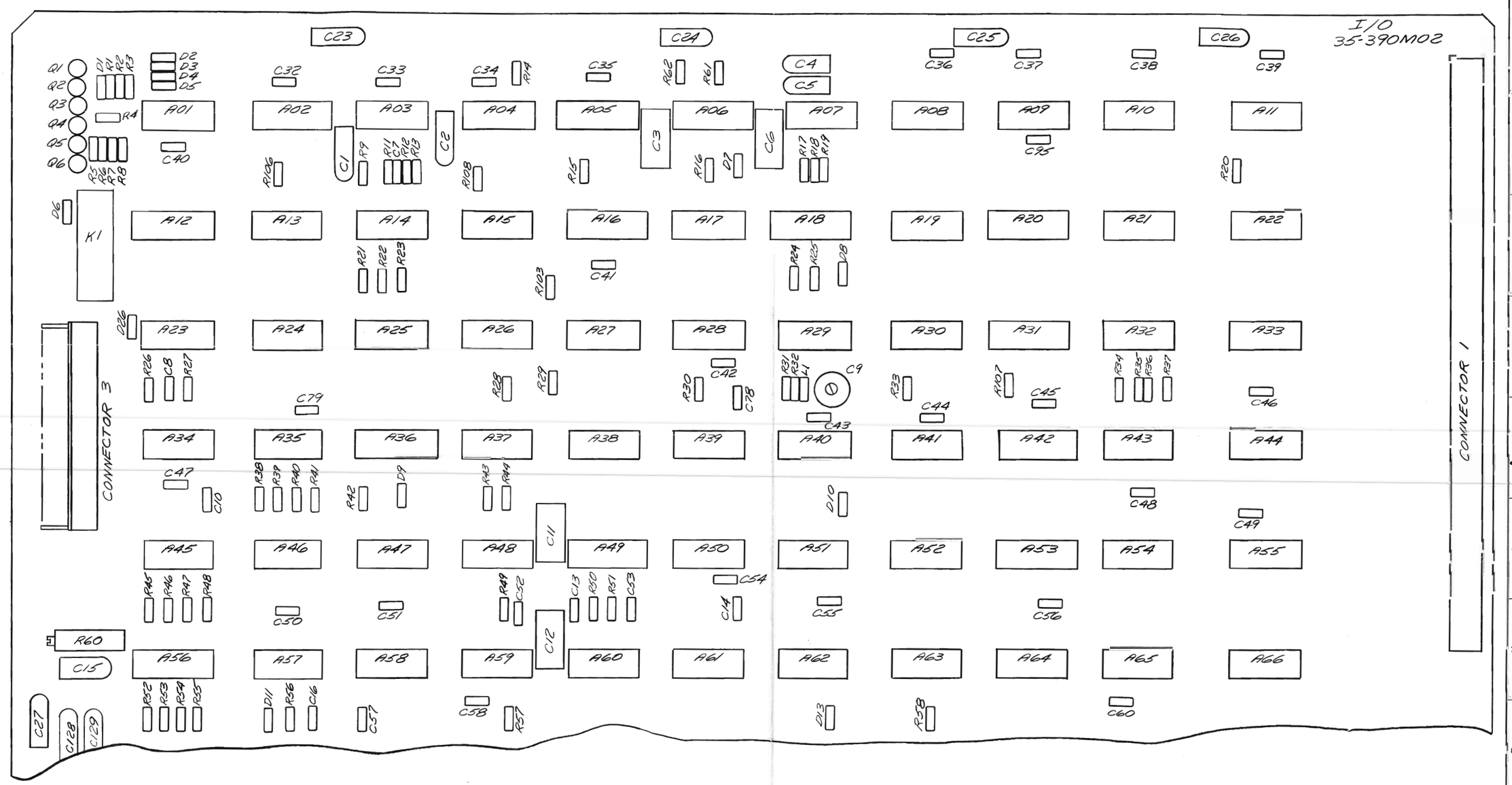
TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO. 03116 DWG NO. 01-05IN01R05D08 SHEET 35 OF 38

BRUNING 44-231 16042

INTERDATA®

I/O
35-390M02



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I/O 35-390M02

NOTES

ADDED:
C128 & 129 LOC A8

EM	MA	V574	MA	6/14/73	E09

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
EDWARDS	DRAFT	8-1-72	
	CHK		
	FNGR		
	DIR ENG		TASK NO 03116
			DWG NO 01-025M01 E09 028
			SHEET 36 OF 38

BRUNING 44-231 16042

INTERDATA®

MEMORY CONT.
35-387M01

A1A A55 A56 A57 A58 A59 A60 A61 A62 A63 A64 A65 A66 A67 A68 A69 A70 A71 A72 A73 A74 A75 A76 A77 A78 A79 A80 A81 A82 A83 A84 A85 A86 A87 A88 A89 A90 A91 A92 A93 A94 A95 A96 A97 A98 A99 A100 A101 A102 A103 A104 A105 A106 A107 A108 A109 A110 A111 A112 A113

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 C100 C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 C111 C112 C113 C114 C115 C120 C121 C122 C123 C124 C125 C126

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81 R82 R83 R84 R85 R86 R87 R88 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99

D1 D2 D3 D4

L1

CONNECTOR 0

DO NOT MANUFACTURE W/O SUPERSEDE
BY PART NO. 35-387M02 SHT 37A
PER ECN NO. 1604
BY EH DATE 12-12-72

MEM. CONT. 35-387M01

COMPONENT	REFERENCE DESIGNATION
CAPACITOR	C1 THRU C127
RESISTOR	R1 THRU R40, R42, R44 THRU R51, R53 THRU R60, R62 THRU R99
DIODE	D1 THRU D4
CHOKE	L1
I.C.	A01 THRU A111

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NOTES

REVISIONS				
LOC C7 ADDED R99 C127				
BG	RJ	1532	12/11/72	R01

NAME	TITLE	DATE
PEDWARDS	DRAFT	7-31-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TAB NO. 03116
DWG NO. 01-05170 ROAD 08

SHEET 37 OF 38

BRUNING 44-231 16042

INTERDATA®

MEMORY CONTROL 35-387 M02

C120 C121 C122 C123 C124 C125

A54 A55 A56 A57 A58 A59 A60 A61 A62 A63 A64 A65 A66 A67 A68 A69 A70 A71 A72 A73 A74 A75 A76 A77 A78 A79 A80 A81 A82 A83 A84 A85 A86 A87 A88 A89 A90 A91 A92 A93 A94 A95 A96 A97 A98 A99 A100 A101 A102 A103 A104 A105 A106 A107 A108 A109 A110 A111 A112 A113

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 C100 C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 C111 C112 C113 C114 C115 C126 C127

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81 R82 R83 R84 R85 R86 R87 R88 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99

D1 D2 D3 D4 L1

■A ■B ■C ■D ■E ■F

CONNECTOR 0

NOTES

MEMORY CONTROL 35-387 M02

COMPONENT	REFERENCE DESIGNATION
CAPACITOR	C1 THRU C127
RESISTOR	R1 THRU R40, R42, R44 THRU R51, 53 THRU R60 THRU R99
DIODE	D1 THRU D4
CHOKE	L1
I.C.	A01 THRU A111

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NAME	TITLE	DATE
B GRAY	DRAFT	10-20-72
R CERO	CHK	11-7-72
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03024
SPEC NO. 01-05IM01 008
SHEET 37 OF 38

BRUNING 44-231 16042

INTERDATA®

MEMORY CONT.
35-387M01

C116 C117 C118 C119

C1 A01 C2 A02 C3 A03 C4 A04 C5 A05 C6 A06 C7 A07 C8 A08

C9 A09 C10 A10 C11 A11 C12 A12 C13 A13 C14 A14 C15 A15 C16 A16

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17

C17 A17 C18 A18 C19 A19 C20 A20 C21 A21 C22 A22 C23 A23 C24 A24

C25 A25 C26 A26

C27 A27 C28 A28

CONNECTOR 3

C31 A31 C32 A32

C29 A29 R18 C30 A30

R19 R20 R21 R22 R23 R24

C33 A33 C34 A34 C35 A35 C36 A36

R97 C37 A37

C38 A38

R25 R26 R27 R28 R29 R30

C39 A39 C40 A40 C41 A41 C42 A42 C43 A43 C44 A44 C45 A45

C46 A46 C47 A47 C48 A48 C49 A49 C50 A50 C51 A51 C52 A52 C53 A53

R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41

CONNECTOR 1

DO NOT MANUFACTURE W/O AUTH

SUPERSEDES
BY PART NO. 35-387M02 SHT 38A
PER ECN NO. 1604
BY EM DATE 12-12-72

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NOTES

MEM. CONT. 35-387M01

NAME	TITLE	DATE
P.EDWARDS	DRAFT	7-31-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-035M01ED4D08B
SHEET 38 OF 38

BRUNING 44-231 16042

INTERDATA®

MEMORY CONTROL
35-387 M02

C116 C117 C118 C119

C1 A01 C2 A02 C3 A03 C4 A04 C5 A05 C6 A06

C7 A07 C8 A08

C9 A09 C10 A10 C11 A11 C12 A12 C13 A13 C14 A14

C15 A15 C16 A16

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17

C17 A17 C18 A18 C19 A19 C20 A20 C21 A21 C22 A22

C23 A23 C24 A24

C25 A25 C26 A26

C27 A27 C28 A28

CONNECTOR 1

CONNECTOR 3

C31 A31 C32 A32 C33 A33 C34 A34 C35 A35 C36 A36

R18 C30 A30

R19 R20 R21 R22 R23 R24

C29 A29

R97 C37 A37

C38 A38

R25 R26 R27 R28 R29 R30

C39 A39 C40 A40 C41 A41 C42 A42 C43 A43 C44 A44

C45 A45

C46 A46 C47 A47 C48 A48 C49 A49 C50 A50 C51 A51

C52 A52 C53 A53

R31 R32 R33 R34 R35 R36 R37

R38 R39 R40 R42

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NOTES

MEMORY CONTROL 35-387 M02

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
B GRAY	DRAFT	10-20-72	MODEL 70 PROCESSOR
R ZERO	CHK	11-9-72	
	ENGR		TASK NO 03024
	DIR ENG		DWG NO 01-051M01 D06 SHEET 38 OF 38

BRUNING 44-231 16042

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INTERDATA®

X ACCESS

P5 — R69 100 — R70 100 — C19 .001 MFD — R358 15 — A19 — R66 100 — Q34 20-020 — R76 (NOTE 1) 3W — R75 75 3W — C21 100PF — (TP) DXC — P15 102-0 — 2G1 — C129 15MFD

3J3 LRIA 09 — A20 19-036 HP — 08 — SCLROA 10 — 126-0 — HI. 2A1

P5 — R67 100 — R68 100 — C18 .001MFD — R359 15 — A19 — R65 100 — Q33 20-020 — R74 (NOTE 1) 3W — R73 75 3W — C20 100PF — (TP) NXC — N15 202-0 — 2S1 — C131 15MFD

3J3 WIA 12 — A20 19-036 HP — 11 — A1 SCLROA 13

MAO 30 110-0
MAO 40 210-0
MAO 50 127-0

3L2 LROA — TP — 12

D(MS) 19-032 1 OUT OF 10 DECODER A26 — C B A(LS) 13 14 15 — 7 6 5 4 3 2 1 0 — 09 07 06 05 04 03 02 01

WOA 3J4 — D(MS) 19-032 1 OUT OF 10 DECODER A21 — C B A(LS) 13 14 15 — 7 6 5 4 3 2 1 0 — 09 07 06 05 04 03 02 01

R81 51.1 — P5

R96 100 Q52 — R94 100 Q51 — R92 100 Q50 — R90 100 Q49 — R88 100 Q48 — R86 100 Q47 — R84 100 Q46 — R82 100 Q45 — R97 100 Q44 — R95 100 Q43 — R93 100 Q42 — R91 100 Q41 — R89 100 Q40 — R87 100 Q39 — R85 100 Q38 — R83 100 Q37

R105 470 — R104 470 — R103 470 — R102 470 — R101 470 — R100 470 — R99 470 — R98 470

XC00 XC01 XC02 XC03 XC04 XC05 XC06 XC07 — CORE PLANE WIRES — XC00-0 -1 -2 -3 -4 -5 -6 XC00-7 — XC07-0 -1 -2 -3 -4 -5 -6 XC07-7

R138 51.1 — P5

A29 R107 100 Q53 — A29 R109 100 Q54 — A29 R111 100 Q55 — A29 R113 100 Q56 — A28 R115 100 Q57 — A28 R117 100 Q58 — A28 R119 100 Q59 — A28 R121 100 Q60 — A31 R122 100 Q61 — A31 R124 100 Q62 — A31 R126 100 Q63 — A31 R128 100 Q64 — A30 R130 100 Q65 — A30 R132 100 Q66 — A30 R134 100 Q67 — A30 R136 100 Q68

230-0 MAO 80 15 — 130-0 MAO 70 14 — 229-0 MAO 60 13 — A(LS) B C — 19-032 1 OUT OF 10 DECODER A27 — 2A5, EROA 3J4 12 — D(MS) 0 — 7 6 5 4 3 2 1 0

2A3, INHOA 3J4 12 — D(MS) 0 — A(LS) B C — 19-032 1 OUT OF 10 DECODER A32 — 7 6 5 4 3 2 1 0

XL00NO XL00PO XL01NO XL01PO XL02NO XL02PO XL03NO XL03PO XL04NO XL04PO XL05NO XL05PO XL06NO XL06PO XL07NO XL07PO

R123 1K — R106 1K — D129 D130
R125 1K — R108 1K — D131 D132
R127 1K — R110 1K — D133 D134
R129 1K — R112 1K — D135 D136
R131 1K — R114 1K — D137 D138
R133 1K — R116 1K — D139 D140
R135 1K — R118 1K — D141 D142
R137 1K — R120 1K — D143 D144

D241 D242 D243 D244 D245 D246 D247 D248 D249 D250 D251 D252 D253 D254 D255 D256

N15 P15

NOTES
1. VALUE TO BE DETERMINED AT TIME OF MANUFACTURE.
2. UNLESS OTHERWISE SPECIFIED ALL TRANSISTORS ARE 20-010

163		R04	PE BA 1236 WH 11/13/71 R02
ADDED NOTE 2 & PART NO. ON TRANS. SHT 1-5			ON SHT. 6K8 - DELETED BACK PANEL ADDRESS CONNECTION TABLE. (SEE USER'S MANUAL)
BG 1618 WH 2-13-73		R05	PE BA 1272 WH 11/14/72 R03
SEE INFO TO RIGHT			CHG SHT 3 & 7 TO B ADDED SHTS. 7A & 8A

REVISIONS:
ON SH. 3R3, R251 WAS 2.2K; C114 WAS 68 PF.
JFT BA 1140 10-5-71 R01
ON SHT. 1 & 2 DELETED VALUE OF R74, R76, R78, & R80. ADDED NOTE 1. ON SHT. 3R3, R251 WAS 6.8K

SHEETS 4 & 5 SENSE AMPS WERE 19-033
BG 1767 WH 5-23-73 R06
SHT 6 REVISED NOTE FOR MS000-MS160
BG WH 1960 WH 10-74 R07

NAME	TITLE	DATE
D. DWORZAK	DRAFT	10FEB71
R F CERO	CHK	1 JULY 71
B ACKERMAN	ENGR	6 JULY 71
M ENOS	QC	6 JULY 71
R E JONES	DIR ENG	6 JULY 71

TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY
TASK NO. 03070
DWG NO. 02-211R07
SHEET 1 OF 8

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D & W REPROGRAPHICS 40086-4

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Y ACCESS

P5 — R64 100 — R63 100 — C16 .001 MFD — A19 — R72 100 — Q36 20-010 — R80 (NOTE 1) 3W — R79 75 3W — C23 100 PF — (TP) PYC — P15 IG2 — C130 15 MFD

3J5 ERW13P1 01 — A20 19-036 HP — 03 — HI, IA1 SCLROA 02

P5 — R62 100 — R61 100 — C15 .001 MFD — A19 — R71 100 — Q35 20-010 — R78 (NOTE 1) 3W — R77 75 3W — C22 100 PF — (TP) NYC — N15 IS1 — C132 15 MFD

3J5 ERW13N1 04 — A20 19-036 HP — 06 — A1 SCLROA 05

MA090 <131-0
MA100 <281-0
MA110 <32-0

3J6 ERW13P0 12 — D(MS) — 1 OUT OF 10 DECODER A18 19-032 — C B A(LS) 13 14 15

ERW13N0 3J6 12 — D(MS) — 1 OUT OF 10 DECODER A13 19-032 — C B A(LS) 13 14 15

R36 51.1 P5

R38 100 Q25 — R40 100 Q26 — R42 100 Q27 — R44 100 Q28 — R46 100 Q29 — R48 100 Q30 — R50 100 Q31 — R52 100 Q32 — R37 100 Q17 — R39 100 Q18 — R41 100 Q19 — R43 100 Q20 — R45 100 Q21 — R47 100 Q22 — R49 100 Q23 — R51 100 Q24

R53 470 — R54 470 — R55 470 — R56 470 — R57 470 — R58 470 — R59 470 — R60 470

XC00 XC01 XC02 XC03 XC04 XC05 XC06 XC07

CORE PLANE WIRES

XC00-0 -1 -2 -3 -4 -5 -6 XC00-7 — XC07-0 -1 -2 -3 -4 -5 -6 XC07-7

YL00NO R19 1K R4 1K D2 D1 — D114 D113
YL00PO
YL01NO R21 1K R6 1K D4 D3 — D116 D115
YL01PO
YL02NO R8 1K R23 1K D6 D5 — D118 D117
YL02PO
YL03NO R10 1K R25 1K D8 D7 — D120 D119
YL03PO
YL04NO R27 1K R12 1K D10 D9 — D122 D121
YL04PO
YL05NO R29 1K R14 1K D12 D11 — D124 D123
YL05PO
YL06NO R16 1K R31 1K D14 D13 — D126 D125
YL06PO
YL07NO R18 1K R33 1K D16 D15 — D128 D127
YL07PO

N15 P15

3F1

233-0) MA140 15 A(LS)
133-0) MA130 14 B
232-0) MA120 13 C

R35 51.1 P5

A10 09 10 08 07 R20 100 Q9
A10 11 12 06 05 R22 100 Q10
A10 13 14 04 03 R24 100 Q11
A10 15 16 02 01 R26 100 Q12
A11 09 10 08 07 R28 100 Q13
A11 11 12 06 05 R30 100 Q14
A11 13 14 04 03 R32 100 Q15
A11 15 16 02 01 R34 100 Q16

A12 19-032 1 OUT OF 10 DECODER — A(LS) B C — 7 6 5 4 3 2 1 0

IA5 EROA 12 D(MS) 0

A8 07 08 10 09 R3 100 Q1
A8 05 06 12 11 R5 100 Q2
A8 03 04 14 13 R7 100 Q3
A8 01 02 16 15 R9 100 Q4
A9 07 08 10 09 R11 100 Q5
A9 05 06 12 11 R13 100 Q6
A9 03 04 14 13 R15 100 Q7
A9 01 02 16 15 R17 100 Q8

A7 19-032 1 OUT OF 10 DECODER — A(LS) B C — 7 6 5 4 3 2 1 0

IA9 INHOA 12 D(MS) 0

NOTES
1. VALUE TO BE DETERMINED AT TIME OF MANUFACTURE.

REV.	DESCRIPTION	APPVD
155.1	REVISED PER LAB PROTOTYPE. D. DWORZAK 3 MAY 71	

NAME: D. DWORZAK
TITLE: DRAFT / CHK / ENGR / DIR ENG
DATE:

TITLE: FUNCTIONAL SCHEMATIC SERIES 5 MEMORY
TASK NO. 03070
DWG NO. 02-211R07 D08
SHEET OF 2-8

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LOGIC, DECOUPLING & SENSE AUX CIRCUITS

LOGIC

MA00 205-0
MA01 108-0
MA02 208-0
LRO 203-0
WO 103-0
ERO 204-0
INHO 104-0
2A2
MA13 0

A3 19-024 HA
A1 19-036 HP
A5 19-015 HG
A4 19-016 HG
A6 19-013 HG
A1 19-036 HP

ENABLE1

D(MS) C B A(LS)
AR 19-032
1 OUT OF 10
DECODER
9 8 7 6 5 4 3 2 1 0
NC-11 NC-10 O9 O7 O6 O5 O4 O3 O2 O1

105-0 PARO
(TP) GRD

P5
R1 1K
R2 1K

INHIA 4S1, 5A1
LRIA 1A1
WIA 1H1
INHOA 1A9
LROA
WOA 1L1
EROA 1A5
ERWI3 R1 2A1
ERWI3N1 2H1
ERWI3P0 2H1
ERWI3N0 2M1

SENSE AUX CIRCUITS

P5
R356 470
P2 10K
R250 1950
CW
C85 15PF
A42 DUAL SINGLE SHOT 19-042
1H1
LROA
P5 R252 1K
(N.C.) 127-1 WRTO
C114 15PF
R251 4.7K P5
(TP) STB R249 1K
STBO
STBA1 4S6
STBB1 5A6
STBC1 4S8
STBD1 5A8

4B4 P15
R242 1K
R243 1K
R245 10K
P5
20-020
Q86
DR58
D259
R244 340
P1 1K
CW
Q88
Q87
R246 47
R247 47
R248 4.7K
C84 2.2MFD
SEE NOTE 2
(TP) VT
129-1 EXVT
N15 N8

TEMP A 128-1
TH1
TEMP B 227-1

4S7, 5A7
N16
R172 100 5W
R178 100 5W
C89 15MFD
D257
N15
4C4, N16

P5
A1 A2 A5 A6 A41 A18 A13 A21 A26 A32 A27 A44 A49 A56 A63 A70 A46 A51 A58 A65 A72 A74 A33 A36 A38 A40 (I.C. REF DESIG)
C1 C2 C124 C127 C128 C14 C11 C24 C27 C31 C29 C86 C87 C88 C89 C90 C115 C117 C119 C121 C123 C125 C131 C53 C55 C57
ALL CAPACITORS THIS ROW: 33 MFD

P5
A1 A2 A3 A4 A6 A5 A41 A18 A13 A7 A12 A20 A21 A24 A32 A27 A46 A51 A58 A65 A72 A70 A63 A56 A49 A94 (I.C. REF DESIG)
ALL CAPACITORS THIS ROW: .001 MFD
C3 C4 C5 C6 C7 C8 C113 C13 C2 C9 C10 C17 C25 C26 C30 C28 C116 C118 C120 C122 C124 C93 C101 C99 C97 C95

DECOUPLING

N6
A68 A55 A62 A69 (IC REF DESIG)
C91 C92 C93 C94
ALL CAPACITORS THIS ROW : 33 MFD

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-344 OR 35-436
2. C84 ON THE 35-436 BOARD IS A 15MFD CAP.

REVISIONS
REMOVED J28-1 CONN DESS. FROM LOC 55
ADDED NOTE 2
BY km 1621 DATE 1/19/73 RO4

REV.	DESCRIPTION	APPD
1&2. 1	REVISED PER LAB PROTOTYPE D.DWORZAK 3 MAY 71	

	NAME	DATE
DRAWN	D. DWORZAK	
TITLE		
DRAFT		
CHK		
ENGR		
DIR ENG		

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TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY
TASK NO. 03070
DWG NO. 02-211 R07 D08
SHEET OF 3-8

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SENSE-INHIBIT BITS9-16

1MHIA 352

STBA1 353

VT 336

N6 3N8

STBC1 354

NOTES

REV.	DESCRIPTION	APPVD	NAME	TITLE	DATE
ISS. 1	REVISED PER LAB PROTOTYPE. D.DWORZAK 4MAY71		R. F. CERO	DRAFT	
				CHK	
				ENGR	
				DIR ENG	

TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

TASK NO. 03070 DWG NO. 02-211R07 D08 SHEET OF 4-8

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SENSE-INHIBIT BITS 0-8

INHIA

STBB1

STBD1

NG

BIT 8 BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0

NOTES

REV.	DESCRIPTION	APPVD
ISS. 1	REVISED PER LAB PROTOTYPE. D.DWORZAK 4 MAY 71	

	NAME	DATE
	R. F. CERO	
TITLE		
DRAFT		
CHK		
ENGR		
DIR ENG		

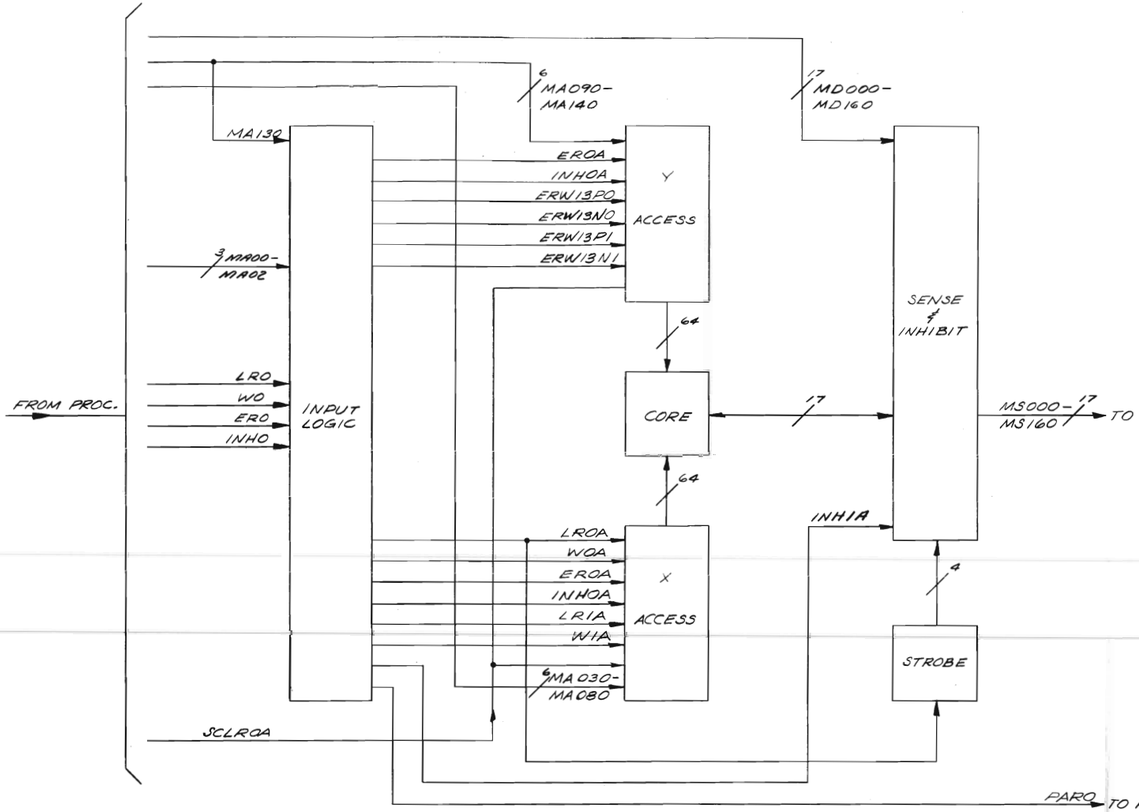
TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

ASM NO. 03070 SHEET OF 5-8

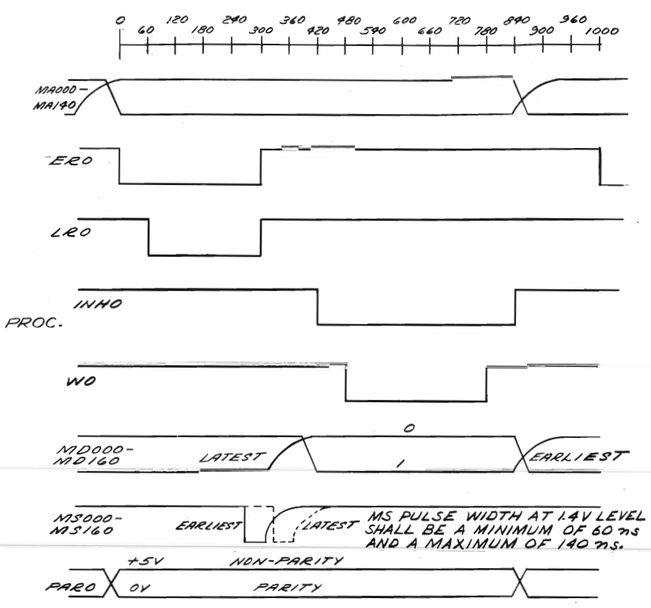
DWG NO. 02-211R07 D08

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BLOCK DIAGRAM



TIMING



TEST POINTS	LOCATION
NXC	1R1
PXC	1G1
NYC	2R1
PYC	2G1
GRD	3A6
LROA	1G2
STB	3L3
VT	3S6

BACK PANEL MAP

CONN	CONN. POS. MOTHER BD. VERT. POS.	SERIES 5 MEMORY HORIZONTAL POS. 1	2
1	41	P5	GND
	40	GND	GND
	39	P15	P15
	38	N15	N15
	37	MD150	MD160
	36	MD130	MD140
	35	MD110	MD120
	34	MD090	MD100
	33	MD070	MD080
	32	MD050	MD060
	31	MD030	MD040
	30	MD010	MD020
	29	EXVT	MD000
	28	TEMP A	
	27	WRTO	TEMP B
	26		
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10		MS000
	09	MS010	MS020
	08	MS030	MS040
	07	MS050	MS060
	06	MS070	MS080
	05	MS090	MS100
	04	MS110	MS120
	03	MS130	MS140
	02	MS150	MS160
	01	GND	GND
	00	P5	GND
0	41	P5	GND
	40	GND	GND
	39		
	38		
	37		
	36		
	35		
	34		
	33	MA130	MA140
	32	MA110	MA120
	31	MA090	MA100
	30	MA070	MA080
	29	MA050	MA060
	28		
	27	SCLR OA	
	26		
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10	MA 030	MA040
	09	MA 020	MA021
	08	MA 01	MA02
	07	MA 010	MA011
	06	MA000	MA001
	05	PARO	MA00
	04	INH O	ERO
	03	WO	LRO
	02	P15	N15
	01	GND	GND
	00	P5	GND

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NOTES

REVISIONS

REVISED. VT MNEM FROM CONN 22B4 BACK PANEL MAP.					
BY	DATE	APPD			
DW	1/6/71	DWK	1/5/73	ROB	

REV.	DESCRIPTION	APPD
ISS. 1	REVISED PER LAB PROTOTYPE D.DWORZAK 4 MAY 71	

	NAME	DATE
DRAFT	D.DWORZAK	
CHK		
ENGR		
DIR ENG		

TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

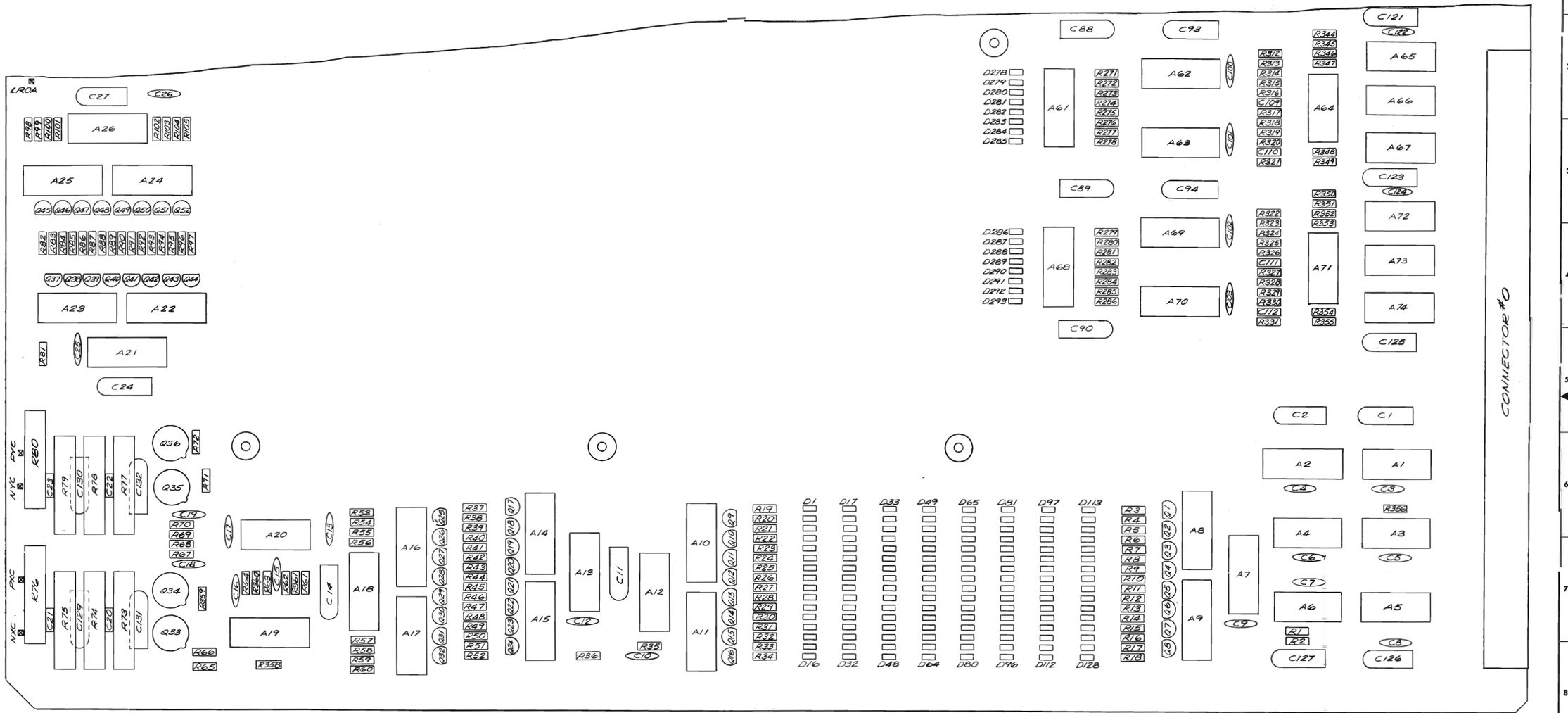
TASK NO. 03070

DWG NO. 02-211R07 D08

SHEET OF 6-8

© R & W REPROGRAPHICS 40004-4

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COMPONENT	REFERENCE DESIGNATION
THERMISTOR	TH1
I.C.	A1 THRU A74
CAP.	C1 THRU 58, 60, 62, 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84 THRU 132
RES	R1 THRU R361
TRANS	Q1 THRU Q88
DIODE	D1 THRU D293
POT.	P1 & P2

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NOTES
1. THIS COMPONENT LOCATOR APPLIES ONLY TO THE 35-344 BOARD.

REVISIONS

ADDED NOTE 1	EM	HM	621	11/15/72	E04

REV.	DESCRIPTION	APPVD
ISS. 1	REVISED PER LAB PROTOTYPE. R358 THRU R361 WERE NOT SPECIFIED. D. DWORZAK 4 MAY 71	

	NAME	TITLE	DATE
	D. DWORZAK	DRAFT	
		CHK	
		ENGR	
		DIR ENG	

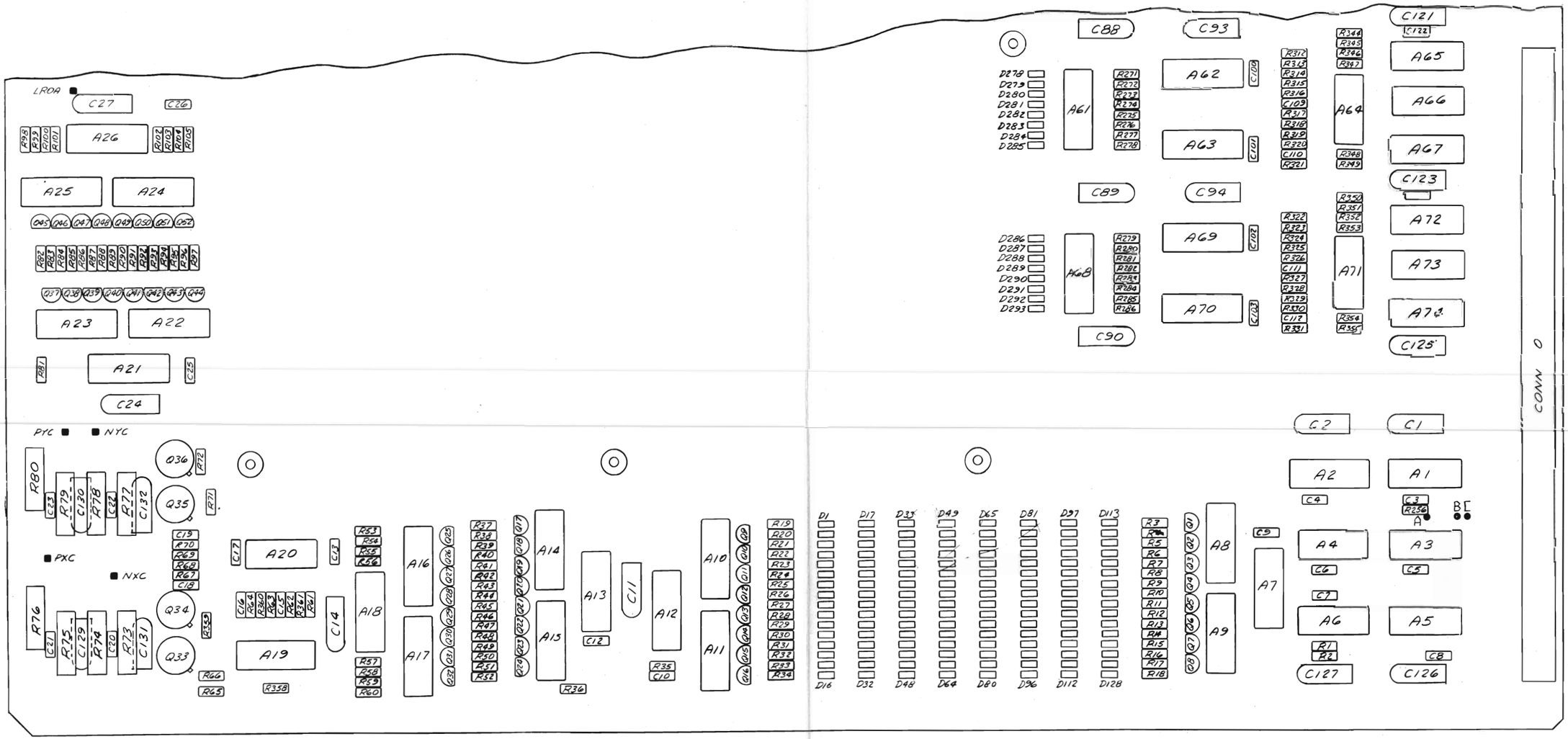
TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

TASK NO. 03070 SHEET OF 7-8

DWG NO. 02-211R07 D08

D & W REPROGRAPHICS 4006S-4

INTERDATA®



NOTES:
1. THIS COMPONENT LOCATOR APPLIES ONLY TO THE 35-436 BOARD.

COMPONENT	REFERENCE DESIGNATION
THERMISTOR	TH1
I. C.	A1 THRU A74
CAP.	C1 THRU C58, 60, 62, 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84 THRU C132
RES.	R1 THRU R361
TRANS	Q1 THRU Q88
DIODE	D1 THRU D293
POT.	P1 AND P2

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NAME: W. ZILLGER
TITLE: DRAFT
DATE: 7-31-72

TITLE: FUNCTIONAL SCHEMATIC
SERIES 5 MEMORY
03024
02-211 R07 D08 7A-8

INTERDATA®

P1
VT
P2
STB
GRD

C31 A32 C30 R158
A31 A30
A33 A34 A35 A36 A37 A38 A39 A40
+C51 +C53 +C55 +C57
Q61 Q62 Q63 Q64 Q65 Q66 Q67 Q68
Q69 Q70 Q71 Q72 Q73 Q74 Q75 Q76 Q77 Q78 Q79 Q80 Q81 Q82 Q83 Q84 Q85
D241 D256 D225 D240 D209 D224 D193 D208 D177 D192 D161 D176 D145 D160 D129 D144
A29 A28
A27
C29 C28

C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49
R139 R140 R141 R142 R143 R144 R145 R146 R357 R147 R148 R149 R150 R151 R152 R153 R154 R155 R156 R157 R158 R159 R160 R161 R162 R163 R164 R165 R166 R167 R168 R169 R170 R171 R172 R173 R257

C84 Q86 Q87 Q88 D258 D259 R242 R243 R244 R245 R246 R247 R248

TH1
C128 A41 C113 A42
R249 R250 C85 C114 R251 R252

A43 A44 A45 A46 A47 A48 A49 A50 A51 A52 A53 A54 A55 A56 A57 A58 A59 A60
C86 C91 C87 C92 C88 C97 C89 C98 C90 C99
D260 D261 D262 D263 D264 D265 D266 D267 D268 D269 D270 D271 D272 D273 D274 D275 D276 D277
R233 R234 R235 R236 R237 R238 R239 R240 R241 R253 R254 R255 R256 R257 R258 R259 R260 R261 R262 R263 R264 R265 R266 R267 R268 R269 R270
C104 C105 C106 C107 C108 R287 R288 R289 R290 R291 R292 R293 R294 R295 R296 R297 R298 R299 R300 R301 R302 R303 R304 R305 R306 R307 R308 R309 R310 R311
C115 C116 C117 C118 C119 C120 R332 R333 R334 R335 R336 R337 R338 R339 R340 R341 R342 R343

NOTES
1. THIS COMPONENT LOCATOR APPLIES ONLY TO 7NE35-3AA BOARD.

REVISIONS
ADDED NOTE 1
BY HA | DATE 12/27/71 | APPD BY

REV.	DESCRIPTION	APPVD.
ISS. 1	REVISED PER LAB PROTOTYPE. D. DWORZAK 4 MAY 71	

	NAME	DATE
DRAFT	D. DWORZAK	
CHK		
ENGR		
DIR ENG		

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TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY
TASK NO. 03070
DWG NO. 02-211R07 DP5
SHEET 5 OF 5

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INTERDATA®

P1
VT
P2
STB
GND

C32 R139 R140 C33 R141 R142 C34 R143 R144 C35 R145 R146 C36 R357 R147 C37 R148 R149 C38 R150 R151 C39 R152 R153 C40 R154 R155 C41 R156 R157 C42 R158 R159 C43 R160 R161 C44 R162 R163 C45 R164 R165 C46 R166 R167 C47 R168 R169 C48 R170 R171 C49 R172 R173 D257

Q86 D258 D259 R245 R246 R247 R248 R243 R244 Q87 Q88

C31 A32 C30 R138 A31 A30

Q61 Q62 Q63 Q64 Q65 Q66 Q67 Q68

R198 R184 R180 R176 A33 A34 C51 C50 R174 R175 C52 R178 R179 C53 R182 R183 C54 R186 R187 C55 R190 R191 C56 R194 R195 C57 R198 R199 C58 R202 R203 C59 R206 R207 C60 R210 R211 C61 R214 R215 C62 R218 R219 C63 R222 R223 C64 R226 R227 C65 R230 R231 C66 R234 R235 C67 R238 R239 R240

R206 R200 R196 R192 A35 A36 C52

R220 R216 R212 R208 A37 A38 C55

R236 R232 R228 R224 A39 A40 C57

Q69 Q70 Q71 Q72 Q73 Q74 Q75 Q76 Q77 Q78 Q79 Q80 Q81 Q82 Q83 Q84 Q85

R177 R181 R185 R189 R193 R197 R201 R205 R209 R213 R217 R221 R225 R229 R233 R237

R241 A43 R253 R254 D260 D261

TH1 C128 R249 R250 C85 A41 C113 A42 C114 R251 R252

C84 A45 C115 C116 A46

A44 C95

R287 R288 R289 R292 R291 C104

C117 C118

C86 C91 A48 C96 A49 C97

R290 R293 R294 R295 R296 C105 R297 R298 R299 R300 C106 R301 A50 R332 R333 R334 R335 R334 R337 A51 A52 A53

D262 D263 D264 D265 D266 D267 D268 D269 A47 R255 R256 R257 R258 R259 R260 R261 R262

C87 C92 A55 C98 A56 C99

R302 R303 R304 R305 R306 C107 R307 R308 R309 R310 C108 R311 A57 R338 R339 R340 R341 R342 R343 C119 C120 A58 A59 A60

D270 D271 D272 D273 D274 D275 D276 D277 A54 R263 R264 R265 R266 R267 R268 R269 R270

A29 A28 A27 C28 C29

CONN 1

D1 D256 D225 D240 D209 D224 D193 D208 D177 D192 D161 D176 D145 D160 D129 D144

NOTES:
1. THIS COMPONENT LOCATOR APPLIES ONLY TO THE 35-436 BOARD.

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION
SER. 5 MEM. 35-437 R00

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NAME	TITLE	DATE
W. ZILLGER	DRAFT	7-31-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
SERIES 5 MEMORY

TAB NO 03024
DWG NO 02-211 R07 D08
SHEET OF 8 8

BRUNING 44 231 16042

INTERDATA®

REVISIONS			
REVISED SHTS 4 & 7			
BG	JEH	2114	R01
REVISED SHTS 2 & 7			
PE	JEH	2132	6-6-74 R02
REVISED SHTS 3 & 4, 7			
GMB	EN	2197	6-19-74 R03

DATA LINES 08-15

PRIVATE DATA LINES 08-15

4 TO 1 MULTIPLEXOR

4 TO 1 MULTIPLEXOR

NOTES 1. PREFERRED ADDRESS X'F0'.
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 MO2 SELECTOR CHANNEL.

SHEET INDEX — SHEET 1 2 3 4 5 6 7 — REV NO. 3 2 2 2 1 1 B

REVISION LEVEL OF SHEET 1 IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
R CERO	CHK	2-6-73
D FRANKENBERGER	ENGR	2-7-73
N. MASI	SYS TST	2-7-73
R.E. JONES	DIR ENG	

TITLE: NS SELECTOR CHANNEL

TASK NO. 03075 — DWG NO. 02-232MXR8D08 — SHEET OF 1-7

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BRUNING 44.231.15043

INTERDATA

GOR1

J5 DR1

111-0 D000 — H2 PD001 — 112 19-036 HP — 114 19-015 HG — 111 19-043 OC — DA000 — 74 19-003 G — 96 19-015 HG — 81 19-036 HP — R31 330 — PD0000 (111-1 — 47 19-015 HG — 52 19-003 G — PDR000 GA2 — PD0001 A2

211-0 D010 — H3 PD011 — 112 19-036 HP — 114 19-015 HG — 111 19-043 OC — DA010 — 74 19-003 G — 95 19-015 HG — 81 19-036 HP — R32 330 — PD0010 (211-1 — 47 19-015 HG — 52 19-003 G — PDR010 GA3 — PD0011 A2

112-0 D020 — H4 PD021 — 112 19-036 HP — 114 19-015 HG — 111 19-043 OC — DA020 — 74 19-003 G — 95 19-015 HG — 81 19-036 HP — R19 330 — PD0020 (112-1 — 69 19-015 HG — 52 19-003 G — PDR020 GA4 — PD0021 A3

212-0 D030 — H5 PD031 — 112 19-036 HP — 114 19-015 HG — 111 19-043 OC — DA030 — 74 19-003 G — 95 19-015 HG — 81 19-036 HP — R18 330 — PD0030 (212-1 — 69 19-015 HG — 52 19-003 G — PDR030 GA5 — PD0031 A4

113-0 D040 — HG PD041 — 101 19-036 HP — 114 19-015 HG — 100 19-043 OC — DA040 — 94 19-003 G — 95 19-015 HG — 80 19-036 HP — R20 330 — PD0040 (113-1 — 63 19-003 G — PDR040 GA6 — PD0041 A5

213-0 D050 — H7 PD051 — 101 19-036 HP — 114 19-015 HG — 100 19-043 OC — DA050 — 94 19-003 G — 95 19-015 HG — 80 19-036 HP — R22 330 — PD0050 (213-1 — 63 19-003 G — PDR050 GA7 — PD0051 A6

114-0 D060 — H8 PD061 — 101 19-036 HP — 70 19-015 HG — 100 19-043 OC — DA060 — 94 19-003 G — 95 19-015 HG — 80 19-036 HP — R23 330 — PD0060 (114-1 — 63 19-003 G — PDR060 GA8 — PD0061 A7

214-0 D070 — H8 PD071 — 101 19-036 HP — 70 19-015 HG — 100 19-043 OC — DA070 — 94 19-003 G — 84 19-015 HG — 80 19-036 HP — R21 330 — PD0070 (214-1 — 69 19-015 HG — 63 19-003 G — PDR070 GA9 — PD0071 A8

1K3 DB001 — 1K4 DB011 — 1K5 DB021 — 1K6 DB031 — 1K6 DB041 — 1K7 DB051 — 1K8 DB061 — 1K9 DB071

1D2 CLG1 — 1E2 DLGO — A9 PHWI

1J1 BSYI — 1E2,F9 PHWI — 3K6,4H7 WTOA — 38 19-002 G — UDBHO — 84 19-015 HG

DATA LINES 00-07

PRIVATE DATA LINES 00-07

P5 — R65 1K — DS J-K 72 19-014 DC 6J3

3A5 DARGI — 4M9, 3K2 CLUSO — 93 19-003 G

LOAD/UNLOAD SEQUENCER

82 19-004 G — 83 19-032 — INPUTS A B C D — OUTPUTS 0 1 2 3 4 5 6 7 8 9 — 1 OF 10 DECODER

01 NC — 02 NC — 03 NC — 04 NC — 05 LARHO 5AB — R55 470 P5 — 06 LARLO 5AB — R56 470 P5 — 07 84 19-015 HG LFRH1 5D1 — R54 470 P5 — 09 84 19-015 HG LFRL1 5D5 — R47 470 P5 — 10 UAARHO 1F8 — R46 470 P5 — 11 UAARLO 1F8 — R45 470 P5

4D8 DAI — 73 19-002 G — DAGO — DAGO 5J8

B1,IM2,4D7 DRI — 1C3 BSYO — 73 19-002 G — DRGO

4H4 SELO — 4D8 CMDI — 73 19-002 G — CMGO

133 19-001 G — 64 19-021 — 10 SYNIO 4F5 — C21 470 PF

IM2,4D6 SRI — 71 19-003 G — SRGO — IF7 — 82 19-004 G — SRG1 1M1

TPA — 1A2 ADI — SCLROA 3A4, 4L5

1E9 ADRSIA — 1G5 SGADO — 93 19-003 G — 85 19-036 HP — ADDRESS FF

D12 — D13 — 1B9 ATSYNO — 82 19-004 G — SGADI 3A4

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NOTES
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AREA B1: ADDED, 93H. AREA A8: A101-13, DLG1, WAS CONN TO DLG1 @ 1A3 2132 4-16-74

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: NS SELECTOR CHANNEL

TASK NO. 03075 — DWG NO. 02-232M01REV08 — SHEET 2-7

© D & W REPROGRAPHICS 42056-4

INTERDATA®

CIRCUIT NOTES

MAP FOR EDX (END OF DATA XFER)

	WTO	WTI	
MCH0	000 SSX	100 SSX	(EVEN) AAR15O
	001 RBA	101 SREQ, SSX, LDB	(ODD) AAR151
MCH1	011 CBSY	111 SREQ, LDB	
	010 CBSY	110 SREQ, LDB	(EVEN) AAR15O

MAP FOR EMX (END MEM. XFER)

	WTO	WTI
MCH0	SREQ, SSX, LDB	RBA
MCH1	SREQ, SSX, LDB	RBA

MAP FOR EBS (END BSY SET)

WTO	WTI
SREQ	SSX

BUFFER ACTIVE FF

BUSY FF

MUX/SELCH FF

WRITE FF

STATUS REQ FF

DATA XFER FF

ONE SHOT

BRANCH GATES

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 MO2 SELECTOR CHANNEL.

REVISIONS
CHANGED: LDRD FROM 71-05 TO 71-11 WAS FROM 71-05 TO 71-09
EM 2197 VM 6-19-74 E02

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NAME	TITLE	DATE
W ZILLGER	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO. 03075 DWG NO. 02-2321MN/E02D08 SHEET OF 3-7

INTERDATA®

REVISIONS			
LOC G6 ADDED R72, C61			
B/C VIEW 2114	VM	7-MAR-74	ROT
REMOVED: CONN. BET. 17-08 & 13-15. ADDED "CDRO" TO "L" - X			
G/M VIEW 2197	VM	6-19-74	ROZ

P5
R49 180
R67 100
223-1 PATNO
C57 470 PF
76 19-004 G
88 19-021 P
ATNO 223-0
1A2, A5 MSCO
87 19-016 HG
109 19-004 G
C60 470 PF
R71 100
122-0 RACKO
R64 680
76 19-004 G
93 19-003 G
85 19-036 HP
1M1 ACKI
3J3 SATNO
86 19-045 DC
NC
A2 MSCO
R61 1K P5 PTACKO 222-1
R60 1K P5 TACKO 222-0
C56 100PF
27 19-003 G
R57 1K P5 ATSYNO 1B9
96 19-015 HG
137-0 ACTO
17 19-057 SG
238-0 ENO
R70 100
C59 100PF
AEQ1
03 19-003 G
32 19-055 SG
77 19-055 SG
3A3 SCLR1
D7 CLOT1
2J5,S4 SELO
126-1 SCLRO
126-0
H1 ENO
104-0 INHO
R72 100
C61 100PF
NC
INH1
CDRO S2
REQUEST FF
SCLR0A 2M7
NC R40 10K P5
62 19-042
3M7 P5R
CDR1
NC
P5R 3F1
TP(I)
SELECT FF
SEL1
TACO 237-0
R58 1K P5 CDRO 6G9, K5
97 19-036 HP
WTI 1J, 3E9
30 19-036
WRTOA 110-1
A03 19-003 G
A41 19-044 HGO
R68 470 P5
14 19-016 HG
TP(F)
ENMDW1 6R1
R62 470 P5
SELO H4
53 19-017 HG
TP(J)
ENMSI 6A1
R59 470 P5
SREQO 3S4
REQO 239-0
REQI H2
TP(G)
ENMDR1 6R1
R3 470 P5
TP(K)
15 19-036 HP
R29 10K P5
43 19-042
ENX1 3K5
5R5 SELIA
2A9 WTOA
3H1 BACT1
5R9 SELI
42 19-016 HG
5J8, 3K8 SINHO
AAR15I
01 19-024 HA
16 19-015 HG
R36 1K P5
3E8 ENG1
760 HF DC
LDB1A 3S7
ALDB1 3A8
CLUS0 2K2
3G4 MSC1
3A7 PSYNO
123-1
R4 180 P5
123 19-015 HG
3A2 PSYN1
79 19-021 P
SYNO 255
123-0
119-0 SR0
102 19-004 G
IM2,2J6 SR1
PSR0 3H6
119-1
R44 1K P5
121-0 CL070
H4 CL071
PCL070 121-1
R43 1K P5
120-0 DR0
IM2,2J5 DR1
90 19-021 P
PDR0 3H5
120-1
R51 1K P5
221-0 DA0
2J4 DA1
PDA0 3H5
221-1
R50 1K P5
220-0 CMD0
2J5 CMD1
PCMD0 220-1
R52 1K P5
C34 100PF
C33 47PF
PADR0 219-1
R53 1K P5
219-0 ADR0
ADRSIA 1E9
1D2 CLG1

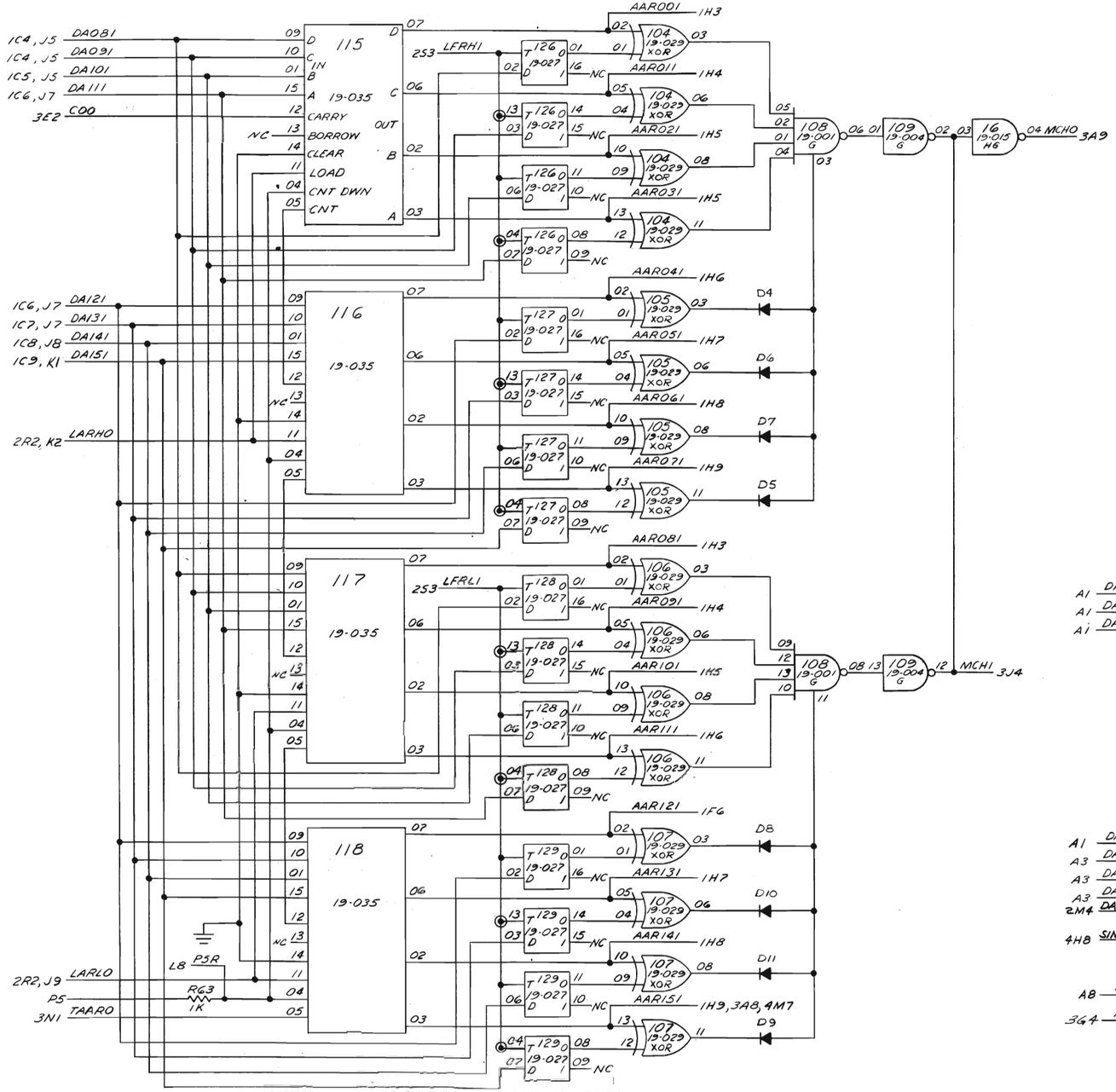
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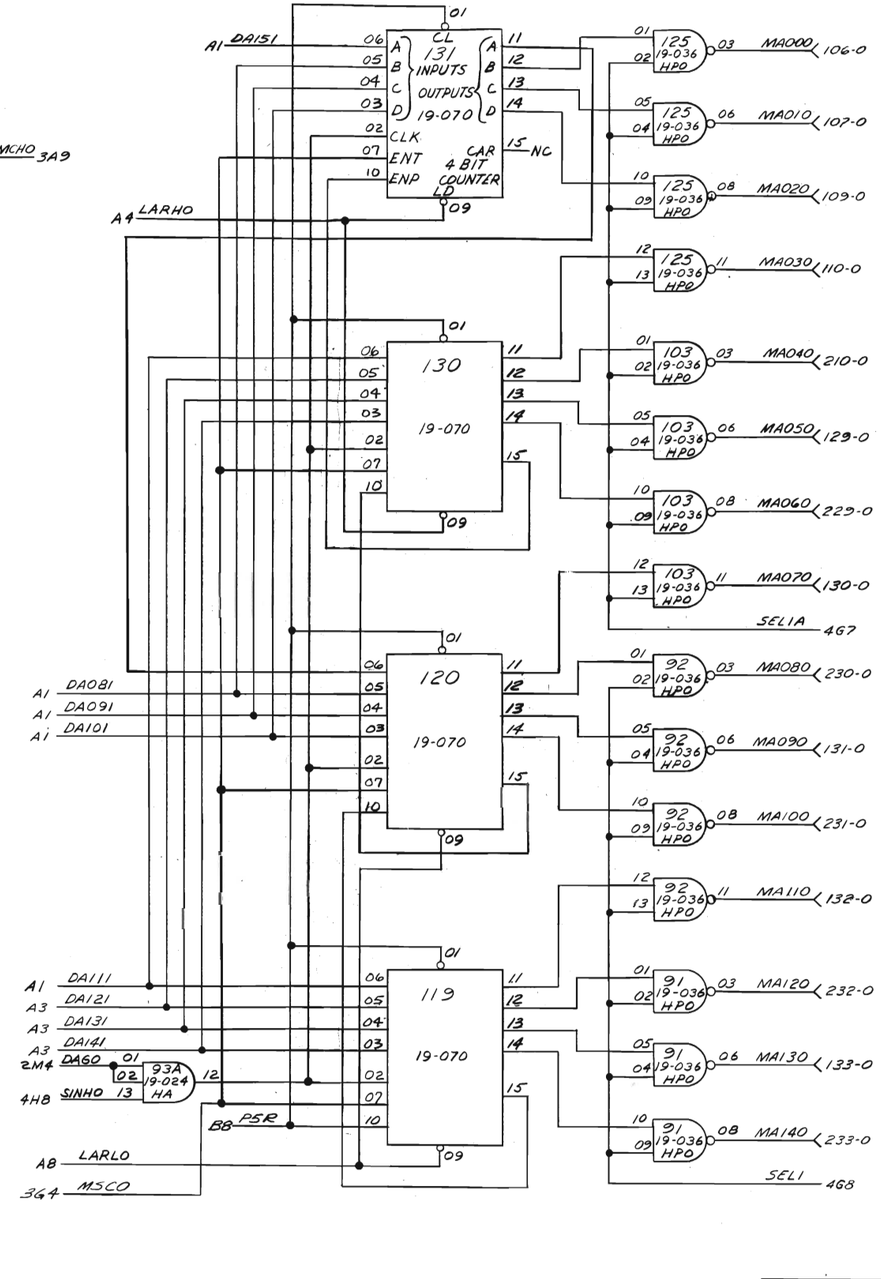
NOTES
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NAME	TITLE	DATE
N. ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: NS SELECTOR CHANNEL
TASK NO. 03075
DWG NO. 02-232M01 Rev D08
SHEET OF 4-7

BRUNING 44 231 15043





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NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: SELECTOR CHANNEL

TASK NO. 03075 | DWG NO. 02-232M01/R01D08 | SHEET OF 5-7

BRUNING 44231 15043

DATA REG HIGH

DATA BUFFER

DATA REG LOW

DATA BUFFER

4R4,H1 ENMS1

210-1 MS000 01 — 58 19-015 HG — 02 — 01 — 6 19-016 HG — 03 — 02 — D S J 7 19-045 K 0 DC — 04 — 01 — 16 — 03 — 15 — 14 NC

1H3,H2 PD081 — 01 — 5 19-043 OC — 03 — 01 — 4 19-015 HG — 02

1H2 PHWOA — 02

2H1 PDR000

109-1 MS010 03 — 58 19-015 HG — 04 — 04 — 6 19-016 HG — 06 — 05 — D S J 7 19-045 K 0 DC — 09 — 06 — 12 — 08 — 11 — 10 NC

1H4,H3 PD091 — 04 — 5 19-043 OC — 06 — 03 — 4 19-015 HG — 04

2H2 PDR010

209-1 MS020 05 — 58 19-015 HG — 06 — 09 — 6 19-016 HG — 08 — 10 — D S J 8 19-045 K 0 DC — 04 — 01 — 16 — 03 — 15 — 14 NC

1H4,H4 PD101 — 09 — 5 19-043 OC — 08 — 05 — 4 19-015 HG — 06

2H3 PDR020

108-1 MS030 09 — 58 19-015 HG — 08 — 12 — 6 19-016 HG — 11 — 13 — D S J 8 19-045 K 0 DC — 09 — 06 — 12 — 08 — 11 — 10 NC

1H5,H5 PD111 — 12 — 5 19-043 OC — 11 — 09 — 4 19-015 HG — 08

2H4 PDR030

208-1 MS040 11 — 58 19-015 HG — 10 — 01 — 19 19-016 HG — 03 — 02 — D S J 20 19-045 K 0 DC — 04 — 01 — 16 — 03 — 15 — 14 NC

1H6,H6 PD121 — 01 — 18 19-043 OC — 03 — 11 — 4 19-015 HG — 10

2H5 PDR040

107-1 MS050 13 — 58 19-015 HG — 12 — 04 — 19 19-016 HG — 06 — 05 — D S J 20 19-045 K 0 DC — 09 — 06 — 12 — 08 — 11 — 10 NC

1H7,H7 PD131 — 04 — 18 19-043 OC — 06 — 13 — 4 19-015 HG — 12

2H6 PDR050

207-1 MS060 01 — 59 19-015 HG — 02 — 09 — 19 19-016 HG — 08 — 10 — D S J 21 19-045 K 0 DC — 04 — 01 — 16 — 03 — 15 — 14 NC

1H7,H8 PD141 — 03 — 18 19-043 OC — 08 — 01 — 17 19-057 SG — 02

2H7 PDR060

106-1 MS070 03 — 59 19-015 HG — 04 — 12 — 19 19-016 HG — 11 — 13 — D S J 21 19-045 K 0 DC — 09 — 06 — 12 — 08 — 11 — 10 NC

1H8,H9 PD151 — 12 — 18 19-043 OC — 11 — 03 — 17 19-057 SG — 04

2H8 PDR070

3G8 LDRH0

3G9 LDRH1 — 01 — 54 19-036 HP — 03 — 02 — R7 470Ω — P5

D 9 0 19-027 T 1 — 02 — 01 — NC — 16

D 9 0 19-027 T 1 — 03 — 14 — NC — 13 — 15

D 9 0 19-027 T 1 — 06 — 11 — NC — 10

D 9 0 19-027 T 1 — 07 — 08 — NC — 04 — 09

D 22 0 19-027 T 1 — 02 — 01 — NC — 16

D 22 0 19-027 T 1 — 03 — 14 — NC — 13 — 15

D 22 0 19-027 T 1 — 06 — 11 — NC — 10

D 22 0 19-027 T 1 — 07 — 08 — NC — 04 — 09

MD000 (229-1) — 02 — 01 — 24 19-036 HP — 03 — DB001 1K3

MD010 (130-1) — 05 — 04 — 24 19-036 HP — 06 — DB011 1K4

MD020 (230-1) — 10 — 09 — 24 19-036 HP — 08 — DB021 1K5

MD030 (131-1) — 13 — 12 — 24 19-036 HP — 11 — DB031 1K5

MD040 (231-1) — 02 — 01 — 23 19-036 HP — 03 — DB041 1K6

MD050 (132-1) — 05 — 04 — 23 19-036 HP — 06 — DB051 1K7

MD060 (232-1) — 10 — 09 — 23 19-036 HP — 08 — DB061 1K8

MD070 (133-1) — 13 — 12 — 23 19-036 HP — 11 — DB071 1K9

LDB1 R9,3S7

CDR0 R9,4R2

A1 ENMS1

206-1 MS080 05 — 59 19-015 HG — 06 — 02 — 01 — 57 19-016 HG — 03

A1 PD081 — 11 — 47 19-015 HG — 10

105-1 MS090 09 — 59 19-015 HG — 08 — 05 — 57 19-016 HG — 06

A2 PD091 — 13 — 47 19-015 HG — 12

205-1 MS100 11 — 59 19-015 HG — 10 — 10 — 57 19-016 HG — 08

A3 PD101 — 13 — 65 19-015 HG — 12

104-1 MS110 13 — 59 19-015 HG — 12 — 13 — 57 19-016 HG — 11

A4 PD111 — 11 — 65 19-015 HG — 10

204-1 MS120 01 — 70 19-015 HG — 02 — 02 — 68 19-016 HG — 03

A5 PD121 — 09 — 65 19-015 HG — 08

3A1 PDR120

103-1 MS130 03 — 70 19-015 HG — 04 — 05 — 68 19-016 HG — 06

AG PD131 — 05 — 65 19-015 HG — 06

3A1 PDR130

203-1 MS140 05 — 70 19-015 HG — 06 — 10 — 68 19-016 HG — 08

A7 PD141 — 03 — 65 19-015 HG — 04

3A1 PDR140

102-1 MS150 09 — 70 19-015 HG — 08 — 13 — 68 19-016 HG — 11

AB PD151 — 01 — 65 19-015 HG — 02

3A1 PDR150

3J9 LDRL0 — 04 — 54 19-036 HP — 06 — R35 470Ω — P5

D S J 1 56 19-045 K 0 DC — 02 — 04 — 01 — 16 — 03 — 15 — 14 NC

D S J 1 56 19-045 K 0 DC — 07 — 11 — 09 — 06 — 12 — 08 — 10 NC

D S J 1 55 19-045 K 0 DC — 02 — 04 — 01 — 16 — 03 — 15 — 14 NC

D S J 1 55 19-045 K 0 DC — 07 — 11 — 09 — 06 — 12 — 08 — 10 NC

D S J 1 67 19-045 K 0 DC — 02 — 04 — 01 — 16 — 03 — 15 — 14 NC

D S J 1 67 19-045 K 0 DC — 07 — 11 — 09 — 06 — 12 — 08 — 10 NC

D S J 1 66 19-045 K 0 DC — 02 — 04 — 01 — 16 — 03 — 15 — 14 NC

D S J 1 66 19-045 K 0 DC — 07 — 11 — 09 — 06 — 12 — 08 — 10 NC

D 44 0 19-027 T 1 — 02 — 01 — NC — 16

D 44 0 19-027 T 1 — 03 — 14 — NC — 13 — 15

D 44 0 19-027 T 1 — 06 — 11 — NC — 10

D 44 0 19-027 T 1 — 07 — 08 — NC — 04 — 09

D 33 0 19-027 T 1 — 02 — 01 — NC — 16

D 33 0 19-027 T 1 — 03 — 14 — NC — 13 — 15

D 33 0 19-027 T 1 — 06 — 11 — NC — 10

D 33 0 19-027 T 1 — 07 — 08 — NC — 04 — 09

ENMDR1 4RG

ENMDW1 4R3

MD080 (233-1) — 01 — 02 — 10 19-036 HP — 03 — DB081 1K3

MD090 (134-1) — 04 — 05 — 10 19-036 HP — 06 — DB091 1K4

MD100 (234-1) — 09 — 10 — 10 19-036 HP — 08 — DB101 1K6

MD110 (135-1) — 12 — 13 — 10 19-036 HP — 11 — DB111 1K6

MD120 (235-1) — 01 — 02 — 11 19-036 HP — 03 — DB121 1K6

MD130 (136-1) — 04 — 05 — 11 19-036 HP — 06 — DB131 1K7

MD140 (236-1) — 09 — 10 — 11 19-036 HP — 08 — DB141 1K8

MD150 (137-1) — 12 — 13 — 11 19-036 HP — 11 — DB151 1K9

LDB1 G9

CDR0 G8

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NOTES:
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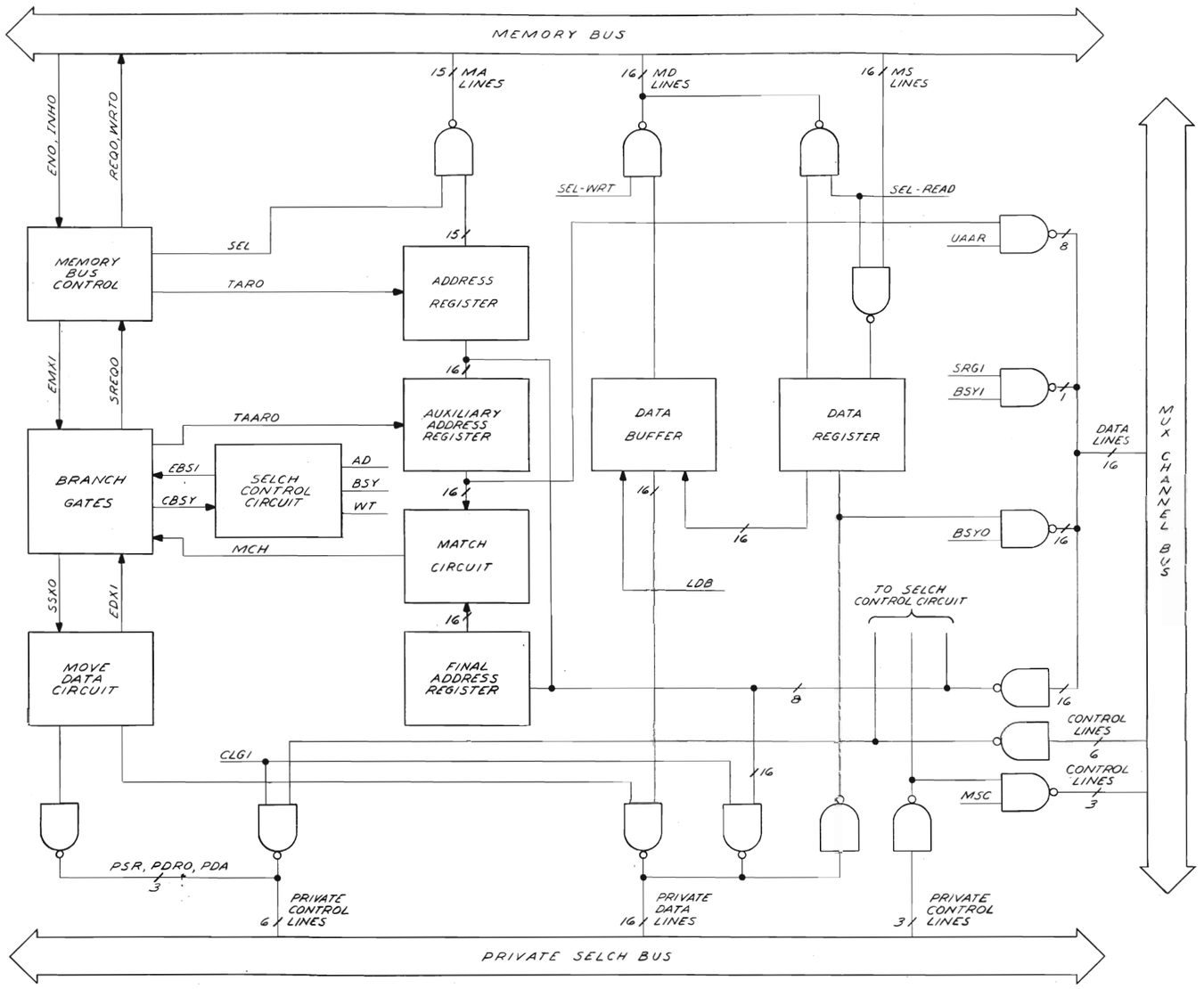
NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: N5 SELECTOR CHANNEL

TASK NO. 03075 — SHEET OF 6 - 7

DWG NO. 02-232M01R01D08

BRUNING 44-231 15043



BACK PANEL PIN INDEX			
MNEM	LOC.	MNEM.	LOC.
ACTO	4H1	MD130	GR6
ADRSO	4B8	MD140	GA7
ATNO	4F1	MD150	GR8
CLO70	4B6	MS000	GA1
CMDO	4B8	MS010	GA2
DO00	2A1	MS020	GA3
DO10	2A2	MS030	GA4
DO20	2A3	MS040	GA5
DO30	2A4	MS050	GA6
DO40	2A5	MS060	GA7
DO50	2A6	MS070	GA8
DO60	2A7	MS080	GH1
DO70	2A8	MS090	GH2
DO80	1A3	MS100	GH3
DO90	1A4	MS110	GH4
DI00	1A5	MS120	GH5
DI10	1A6	MS130	GH6
DI20	1A6	MS140	GH7
DI30	1A7	MS150	GH8
DI40	1A8	PADRSO	4F8
DI50	1A8	PATNO	4B1
DAO	4B7	PCLO70	4F6
DRO	4B7	PCMDO	4F8
ENO	4H1	PDO00	2F1
HWO	1D1	PDO10	2F2
INHO	4H5	PDO20	2F3
MAO00	5R1	PDO30	2F4
MAO10	5R1	PDO40	2F5
MAO20	5R2	PDO50	2F6
MAO30	5R2	PDO60	2F7
MAO40	5R3	PDO70	2F8
MAO50	5R3	PDO80	1R4
MAO60	5R4	PDO90	1R4
MAO70	5R4	PDI00	1R5
MAO80	5R5	PDI10	1R6
MAO90	5RG	PDI20	1R7
MAI00	5R6	PDI30	1R7
MAI10	5R7	PDI40	1R8
MAI20	5R7	PDI50	1R9
MAI30	5R8	PDAO	4F7
MAI40	5R8	PDRO	4F8
MDO00	6G1	PHWO	1A1
MDO10	6G2	PSRO	4F6
MDO20	6G3	PSYNO	4B5
MDO30	6G4	PTACKO	4F2
MDO40	6G5	RACKO	4B3
MDO50	6G6	REQO	4R5
MDO60	6G7	SCLRO	6H4
MDO70	6G8	SRO	4B6
MDO80	6R1	SYNO	4F5
MDO90	6R2	TACKO	6H3
MDI00	6R3	TACO	4R1
MDI10	6R4	WRTOA	4R3
MDI20	6R5		

TEST POINT INDEX		
DESIG	MNEM	LOC.
A	ADI	2L6
B	WTI	3G5
C	SXI	3G6
D	MSCO	3G4
E	BSYO	3G3
F	ENMDRI	4S3
G	REQI	4S5
H	DXI	3G7
I	SELI	4L3
J	ENMSI	4S4
K	ENMDRI	4S6

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION

NS SELCH	35-391 M02 R03

BACK PANEL MAP			
ROW 1	ROW 2	TERM NO.	CONN.
P5	GND	41	1
GND	GND	40	
		39	
		38	
MD150		37	
MD130	MD140	36	
MD110	MD120	35	
MD090	MD100	34	
MD070	MD080	33	
MD050	MD060	32	
MD030	MD040	31	
MD010	MD020	30	
	MD000	29	
		28	
		27	
SCLRO	PHWO	26	
		25	
		24	
PSYNO	PATNO	23	
	PTACKO	22	
PCLO70	PDAO	21	
PDRO	PCMDO	20	
PSRO	PADRSO	19	
PDI40	PDI50	18	
PDI20	PDI30	17	
PDI00	PDI10	16	
PDO80	PDO90	15	
PDO60	PDO70	14	
PDO40	PDO50	13	
PDO20	PDO30	12	
PDO00	PDO10	11	
WRTOA	MS000	10	
MS010	MS020	09	
MS030	MS040	08	
MS050	MS060	07	
MS070	MS080	06	
MS090	MS100	05	
MS110	MS120	04	
MS130	MS140	03	
MS150		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	0
GND	GND	40	
	REQO	39	
	ENO	38	
ATCO	TACO	37	
		36	
		35	
		34	
MA130	MA140	33	
MA110	MA120	32	
MA090	MA100	31	
MA070	MA080	30	
MA050	MA060	29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
CLO70	DAO	21	
DRO	CMDO	20	
SRO	ADRSO	19	
DI40	DI50	18	
DI20	DI30	17	
DI00	DI10	16	
DO80	DO90	15	
DO60	DO70	14	
DO40	DO50	13	
DO20	DO30	12	
DO00	DO10	11	
MA030	MA040	10	
MA020		09	
		08	
MA010		07	
MA000		06	
		05	
INHO		04	
		03	
		02	
GND	GND	01	
P5	P5	00	

NOTES

REVISIONS		
IN SUPP INFO 35-392 M02 WAS R00	2 WH 2/32 WH 4-16-74	E02
- WH 2/14 WH 3/14/74 R01	AREA M9: LEV LEV OF 35-391 M02 WAS R02	
IN SUPP INFO 35-392 M02 WAS R01	WH WH 2/97 WH 6/28/74	E03

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-13-71
	CHK	
	ENGR	
	MFR ENG	

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TITLE: N.S SELECTOR CHANNEL

TASK NO. 03075 | SHEET OF 7-7

FUNC NO. 02-232 M01 R03 E03

BRUNING 44231 15043

INTERDATA®

SHTS 1 & 2 CHG'D IC No. A24, A25 & A28 WAS 19-015 HG. A26 WAS 19-016 HG. PIN 01 OF A27 WAS N.C. ADDED P26 TO A19 PIN 04 & 05

PM	PE	1483	MM	7/7/72	ECN

CHANGED: SHT 1 LOC A1-A5 IC A30 & 31 WAS 19-016 HG

ADDED: SHT 1 LOC M9, C1 & R27

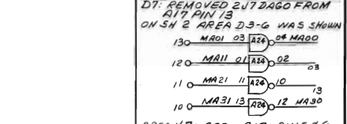
PM	PE	1507	MM	7/24/72	R02

CHG. SHT 1 LOC J7 ADD-10 WAS DGND TO A02-12 NON COMM TO A02-15

PM	MM	1616	MM	10/9/72	R03

DT: REMOVED 2J7 DAGO FROM A17 PIN 13

ON SH 2 AREA D3-G WAS SHOWN



AREA N7: ADD A13 PIN 5 & 6 AREA K7: A19 PIN 5 WAS IFB DAGO

TCP	PM	1904 1863	MM	9-21-73	R04

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NOTES: 1. PREFERRED ADDRESS X'AE'

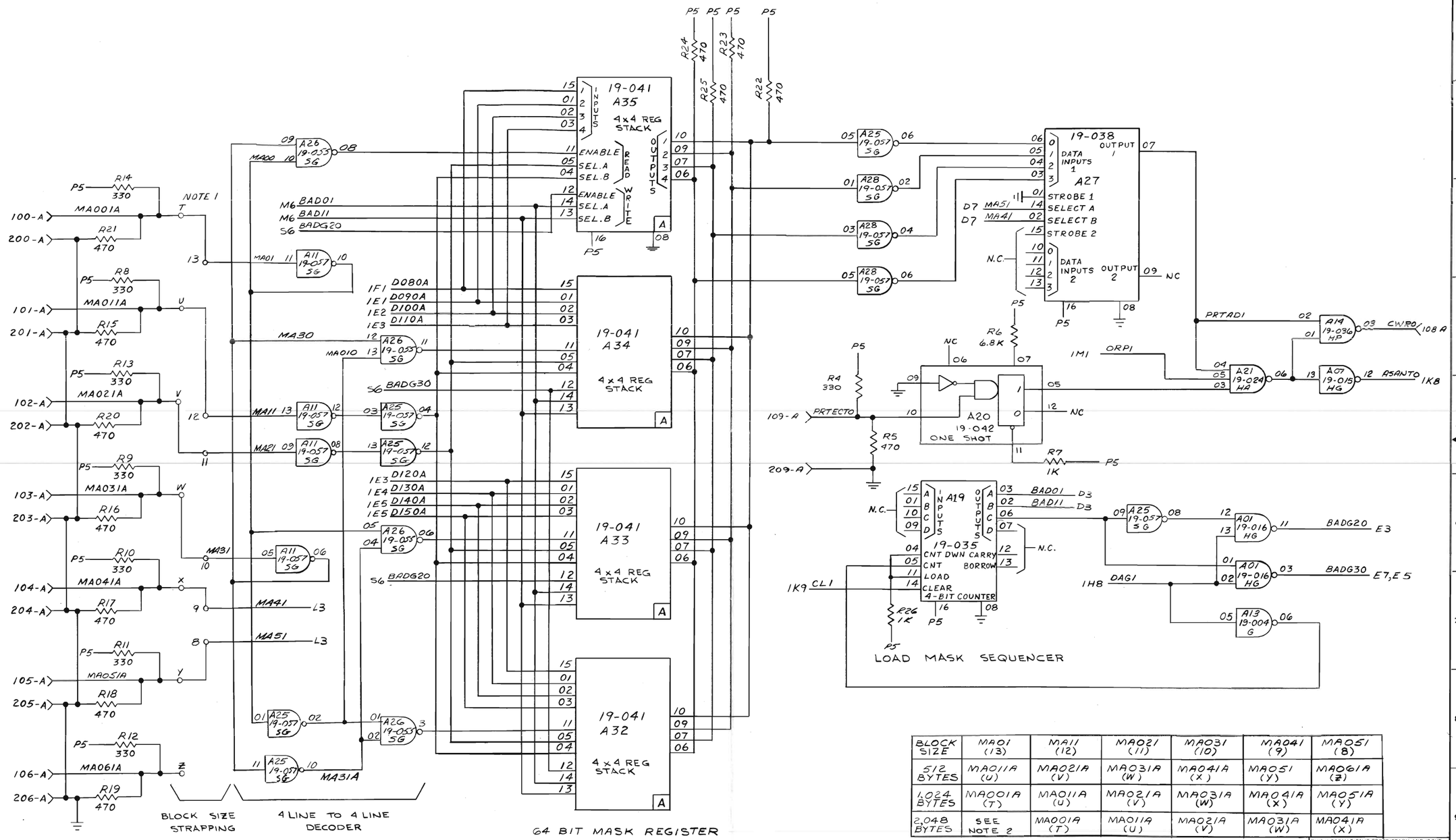
NAME	TITLE	DATE
L. VALENTY	DRAFT	9-10-71
G.J. HOMEFIELD	CHK	1-7-72
D. FRANKENBERGER	ENGR	1-14-72
D.W. YOUNG	SYS	1-14-72
R.E. JONES	DIR ENG	1-17-72

TITLE FUNCTIONAL SCHEMATIC NS -MEMORY PROTECT

TASK NO. 03123 DWG NO. 02-2361A04D08 SHEET OF 1 - 3

D. D & W REPROGRAPHICS 40059-4

INTERDATA®



BLOCK SIZE	MA01 (13)	MA11 (12)	MA021 (11)	MA031 (10)	MA041 (9)	MA051 (8)
512 BYTES	MA011A (U)	MA021A (V)	MA031A (W)	MA041A (X)	MA051 (Y)	MA061A (Z)
1,024 BYTES	MA001A (T)	MA011A (U)	MA021A (V)	MA031A (W)	MA041A (X)	MA051A (Y)
2,048 BYTES	SEE NOTE 2	MA001A (T)	MA011A (U)	MA021A (V)	MA031A (W)	MA041A (X)

TABLE 1. BLOCK SIZE STRAPPING

NOTES: 1. STRAPPED FOR 1K BYTE BLOCKS
2. FOR THE 2K BYTE OPTION MA01 (13) MUST BE TIED TO GROUND

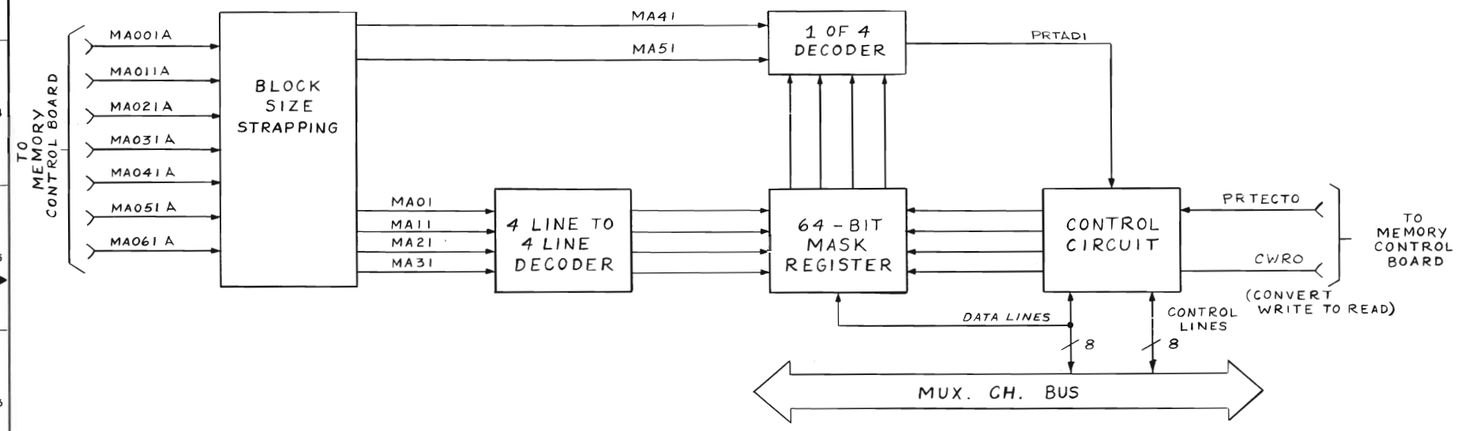
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NAME	TITLE	DATE
L. VALENTY	DRAFT	9-14-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
NS - MEMORY PROTECT

TASK NO. 03123
DWG NO. 02-286,R04D08
SHEET 2 OF 3

D D & W REPROGRAPHICS 40058-4



BLOCK DIAGRAM

HORIZ. POS	VERTICAL POSITION 1	2
00		GND
01	MA001A	GND
02	MA011A	GND
03	MA021A	GND
04	MA031A	GND
05	MA041A	GND
06	MA051A	GND
07	MA061A	GND
08	CWRO	GND
09	PROTECTO	GND

CABLE MAP

HORIZ. POS	VERTICAL POSITION 1	2
00		GND
01	P5	GND
02		
03		
04		
05		
06		
07		
08		
09		
10		
11		
12		
13		
14		
15	D080	D090
16	D100	D110
17	D120	D130
18	D140	D150
19	SR0	ADR50
20	DR0	CMD0
21	CLOT0	DA0
22	RACK0	TACK0
23	SYN0	ATN0
24		
25	SCLR0	HW0
26		
27		
28		
29		
30		
31		
32		
33		
34		
35		
36		
37		
38		
39	GND	GND
40	GND	GND
41	P5	GND

BACK PANEL MAP

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NOTES

NAME	TITLE	DATE
L.VALENTY	DRAFT	9-14-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
NS - MEMORY PROTECT

TASK NO. 03123
DWG NO. 02-236 RD008

SHEET 3 OF 3

INTERDATA

REVISIONS (CONTINUED)								
ADDED: AT 138 & 139								
DB1-C3, I/O-213-3 & I/O-214-3								
EM	83	1367	V4	8	4-6-71	R04		
SHT 1 LOC C6 DEL.								
TERM 10 & 11. 28 & 29 DEL.								
TERM 23 & 24 SHOW								
CONN DB1-C3 & C4 AS T.P.								

REVISIONS								
ORIGINAL ISSUE WAS R01								
ADDED 3 RESISTORS,								
7 DIODES, AND 1 GATE								
LV	UF	1109	V2	8	4-7-71	R02		
ADDED GND TO I/O-100-3								
LOC S9								
A	WH	22						

ADDED: IC P 19-004 & CONN. TERM 02 TO 05 SW21-SHT 1 LOC C3 ON SHT 2 ADDED IC A 19-021 LOC C6 REMOVED: IC P 19-004 LOC C6

LOC C5 SW21 PIN NO'S WERE CHANGED TO CONFORM WITH NEW SWITCH CONFIG. SEE 2J3

LOC B8 & C8 REMOVED UNUSED GATES

LOC/C5 REMOVED CONN FROM SW21-02 TO SW21-03

CONN I/O-213-3 & I/O 214-3 AS T.P. LOC N7

MNEM. SRGO WAS SRGO LOC E7 ADDED C3-C7. SHT2 LOC H-L7

PWR'L UP RESIS.

RUN1 N9, 285, 2D2
RUN0 N9, 2D5
SNGL 2D5, 2D2 (SINGLE)
SNGO 2B5, 2D5
ESWCO N7
ESWOO N8
INIT N8
INITO N8
SW03 SW02 SW01 SW00
SW04 SW05 SW06 SW07 SW08 SW09 SW10 SW11
SW12 SW13 SW14 SW15 SW16 SW17 SW18 SW19
SW21
01W 05W 09W
OFF ON LOCK
CONT2
CONT1
POFFO
TO NB CONTROL RELAY
R10 1K
R6 1K
R8 1K
R4 1K
R3 1K
R9 1K
R7 1K
P5
2B3, 2B5, 2C2, 2D3, 2E5
2F5
RORO RAWO RINO RSWO R010 R230 R450 R670 R890 RAB0 RCD0 REF0
2E8
D01 D11 D21 D31 D41 D51 D61 D71 D06 D11 D21 D31 D41 D51 D61 D71
LDO LCO LBO LAO SNIO SCOO WAITI SRGO ESNCO ESNOO INITO POFFO CONT1 CONT2 SSGL1 INIT1 RUN1 RUN0 SND
2K7
C2 C3 D2 C7, D6 D6 D6 1H4 D2 B2 B2
DB1-C1 DB1-C2 DB1-C3 DB1-C4
I/O-106-3 I/O-215-3 I/O-214-3
NC
LP5 POWER WAITI
LGND TO ALL LAMP DRIVE POWER GATES
P5
GND TO ALL GATES EXCEPT LAMP DRIVERS
C1 2.2 MF
C2 2.2 MF
C3 1000PF
C4 1000PF
C5 1000PF
C6 1000PF
C7 1000PF
DISPLAY 1
DISPLAY 2

NOTES

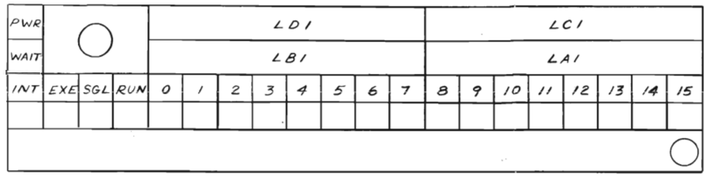
NAME	TITLE	DATE
N TERNUNE	DRAFT	10 AUG 71
R F CERO	CHK	10 AUG 71
B.W. SATHMARY	ENGR	2 JUNE 71
M. FUCHS	Q C	2 JUNE 71
R. JONES	DIR ENG	2 JUNE 71

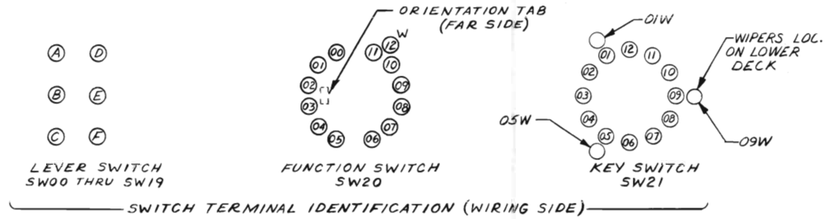
TITLE SCHEMATIC DISPLAY PANEL (CNS 1)

SIZE B | CODE 23116 | DWG NO 29-651209008 | SHEET 1 OF 2

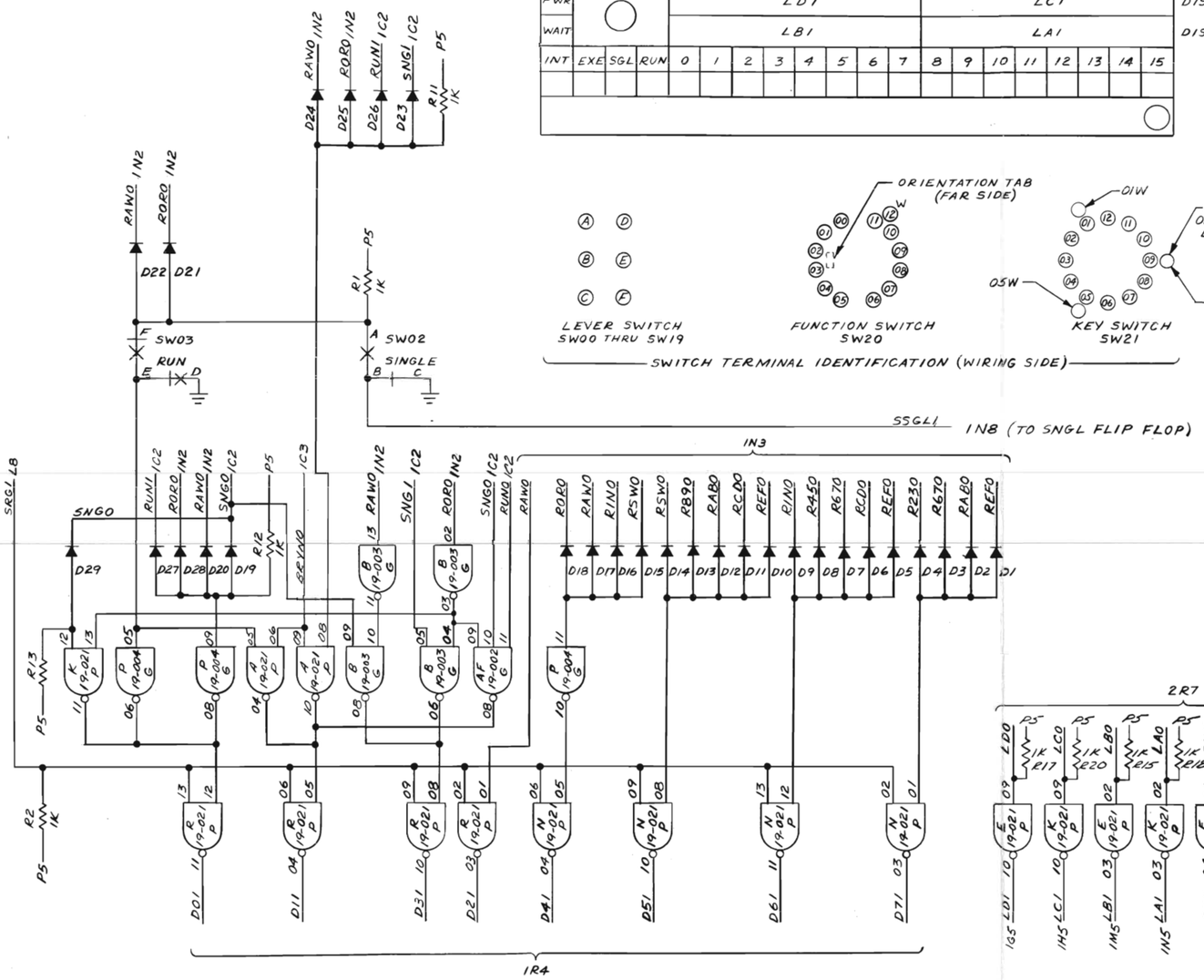
INTERDATA®

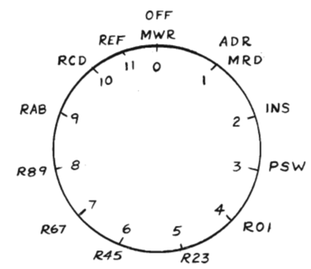
FRONT PANEL LAYOUT





STATUS												
RUN	OFF WRT RORO	ADRS RD RAWO	SINGLE	MODE	0	1	2	3	4	5	6	7
0	0	0	0	HALT	1	1	0	0	X	X	X	X
0	0	0	1	HALT	1	1	0	0	X	X	X	X
0	0	1	0	ADR	0	0	1	1	0	0	0	0
0	0	1	1	MRD	0	0	1	0	0	0	0	0
0	1	0	0	HALT	1	1	0	0	0	0	0	0
0	1	0	1	MWR	0	0	0	1	0	0	0	0
0	1	1	0									
0	1	1	1									
1	0	0	0	RUN	1	0	0	0	X	X	X	X
1	0	0	1	VAR	0	1	0	0	X	X	X	X
1	0	1	0	ADR	0	0	1	1	0	0	0	0
1	0	1	1	MRD	0	0	1	0	0	0	0	0
1	1	0	0	RUN	1	0	0	0	0	0	0	0
1	1	0	1	MWR	0	0	0	1	0	0	0	0
1	1	1	0									
1	1	1	1									
				OFF					0	0	0	0
				INS					0	0	1	0
				PSW					0	1	0	0
				0/1					1	0	0	0
				2/3					1	0	0	1
				4/5					1	0	1	0
				6/7					1	0	1	1
				8/9					1	1	0	0
				A/B					1	1	0	1
				C/D					1	1	1	0
				E/F					1	1	1	1





FRONT VIEW ROTARY

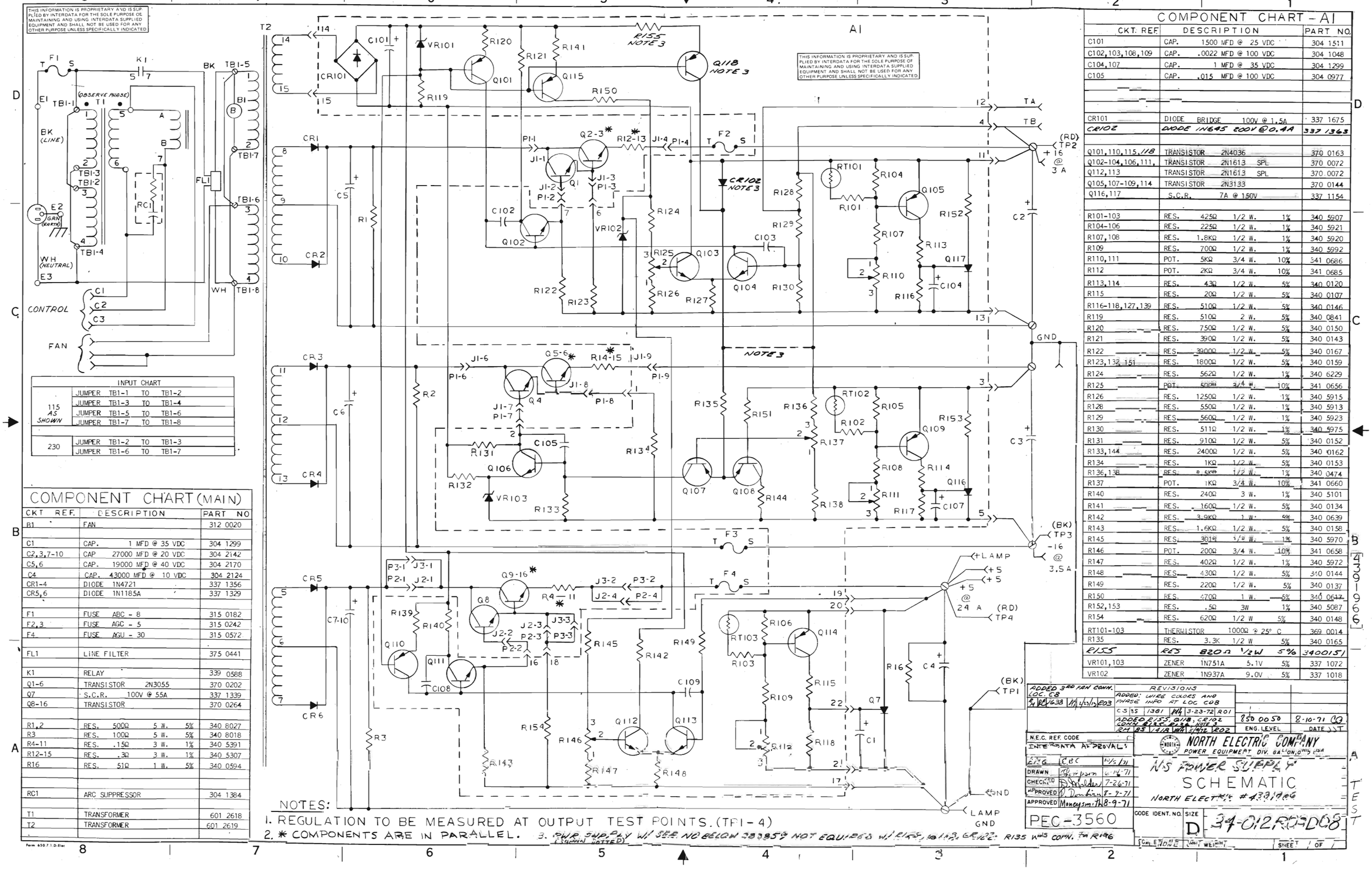
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NOTES

NAME	TITLE	DATE	TITLE SCHEMATIC
L. VALENTY	DRAFT	28JUL71	DISPLAY PANEL (NS1)
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03116 SHEET OF 2-2
			DWG NO. 09-051R09D08

BIRLNING 44-231 15043

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INPUT CHART				
115 AS SHOWN	JUMPER	TB1-1	TO	TB1-2
	JUMPER	TB1-3	TO	TB1-4
	JUMPER	TB1-5	TO	TB1-6
	JUMPER	TB1-7	TO	TB1-8
230	JUMPER	TB1-2	TO	TB1-3
	JUMPER	TB1-6	TO	TB1-7

COMPONENT CHART (MAIN)

CKT REF.	DESCRIPTION	PART NO
B1	FAN	312 0020
C1	CAP. 1 MFD @ 35 VDC	304 1299
C2,3,7-10	CAP 27000 MFD @ 20 VDC	304 2142
C5,6	CAP. 19000 MFD @ 40 VDC	304 2170
C4	CAP. 43000 MFD @ 10 VDC	304 2124
CR1-4	DIODE 1N4721	337 1356
CR5,6	DIODE 1N1185A	337 1329
F1	FUSE ABC - 8	315 0182
F2,3	FUSE AGC - 5	315 0242
F4	FUSE AGU - 30	315 0572
FL1	LINE FILTER	375 0441
K1	RELAY	339 0588
Q1-6	TRANSISTOR 2N3055	370 0202
Q7	S.C.R. 100V @ 55A	337 1339
Q8-16	TRANSISTOR	370 0264
R1,2	RES. 500Ω 5 W. 5%	340 8027
R3	RES. 100Ω 5 W. 5%	340 8018
R4-11	RES. .15Ω 3 W. 1%	340 5391
R12-15	RES. .3Ω 3 W. 1%	340 5307
R16	RES. 51Ω 1 W. 5%	340 0594
RC1	ARC SUPPRESSOR	304 1384
T1	TRANSFORMER	601 2618
T2	TRANSFORMER	601 2619

COMPONENT CHART - A1

CKT. REF.	DESCRIPTION	PART NO.
C101	CAP. 1500 MFD @ 25 VDC	304 1511
C102,103,108,109	CAP. .0022 MFD @ 100 VDC	304 1048
C104,107	CAP. 1 MFD @ 35 VDC	304 1299
C105	CAP. .015 MFD @ 100 VDC	304 0977
CR101	DIODE BRIDGE 100V @ 1.5A	337 1675
CR102	DIODE IN645 200V @0.4A	337 1363
Q101,110,115,118	TRANSISTOR 2N4036	370 0163
Q102-104,106,111,	TRANSISTOR 2N1613 SPL	370 0072
Q112,113	TRANSISTOR 2N1613 SPL	370 0072
Q105,107-109,114	TRANSISTOR 2N3133	370 0144
Q116,117	S.C.R. 7A @ 150V	337 1154
R101-103	RES. 425Ω 1/2 W. 1%	340 5907
R104-106	RES. 225Ω 1/2 W. 1%	340 5921
R107,108	RES. 1.8KΩ 1/2 W. 1%	340 5920
R109	RES. 700Ω 1/2 W. 1%	340 5992
R110,111	POT. 5KΩ 3/4 W. 10%	341 0686
R112	POT. 2KΩ 3/4 W. 10%	341 0685
R113,114	RES. 43Ω 1/2 W. 5%	340 0120
R115	RES. 20Ω 1/2 W. 5%	340 0107
R116-118,127,139	RES. 510Ω 1/2 W. 5%	340 0146
R119	RES. 510Ω 2 W. 5%	340 0841
R120	RES. 750Ω 1/2 W. 5%	340 0150
R121	RES. 390Ω 1/2 W. 5%	340 0143
R122	RES. 3900Ω 1/2 W. 5%	340 0167
R123,132,151	RES. 1800Ω 1/2 W. 5%	340 0159
R124	RES. 562Ω 1/2 W. 1%	340 6229
R125	POT. 500Ω 3/4 W. 10%	341 0656
R126	RES. 1250Ω 1/2 W. 1%	340 5915
R128	RES. 550Ω 1/2 W. 1%	340 5913
R129	RES. 560Ω 1/2 W. 1%	340 5923
R130	RES. 511Ω 1/2 W. 1%	340 5975
R131	RES. 910Ω 1/2 W. 5%	340 0152
R133,144	RES. 2400Ω 1/2 W. 5%	340 0162
R134	RES. 1KΩ 1/2 W. 5%	340 0153
R136,138	RES. 2.5KΩ 1/2 W. 1%	340 0474
R137	POT. 1KΩ 3/4 W. 10%	341 0660
R140	RES. 240Ω 3 W. 1%	340 5101
R141	RES. 160Ω 1/2 W. 5%	340 0134
R142	RES. 3.9KΩ 1 W. 5%	340 0639
R143	RES. 1.6KΩ 1/2 W. 5%	340 0158
R145	RES. 301Ω 1/2 W. 1%	340 5970
R146	POT. 200Ω 3/4 W. 10%	341 0658
R147	RES. 402Ω 1/2 W. 1%	340 5972
R148	RES. 430Ω 1/2 W. 5%	340 0144
R149	RES. 220Ω 1/2 W. 5%	340 0137
R150	RES. 470Ω 1 W. 5%	340 0647
R152,153	RES. .5Ω 3W 1%	340 5087
R154	RES. 620Ω 1/2 W 5%	340 0148
RT101-103	THERMISTOR 1000Ω @ 25° C	369 0014
R135	RES. 3.3K 1/2 W 5%	340 0165
R155	RES 820Ω 1/2W 5%	340015[illegible]
VR101,103	ZENER 1N751A 5.1V 5%	337 1072
VR102	ZENER 1N937A 9.0V 5%	337 1018

NOTES:
1. REGULATION TO BE MEASURED AT OUTPUT TEST POINTS. (TP1-4)
2. * COMPONENTS ARE IN PARALLEL.
3. PWR SUPPLY W/ SER NO BELOW 383853 NOT EQUIPPED W/ R155, 1W 1%, CR102. R135 WAS COMM. FOR R196 (SHOWN NOTED)

REVISIONS				
ADDED 3RD FAN CONN. LOC. C8				
ADDED: WIRE COLORS AND PHASE INFO AT LOC C8	C-3	35	1381	3-23-72 R01
ADDED R155, Q118, CR102 CONN. [illegible] NOTE 3	850 0050		8-10-71 CG	
[illegible]	ENG. LEVEL		DATE	

N.E.C. REF. CODE		
INTERDATA APPROVAL:		
ENG.	CEC	11/5/71
DRAWN	[illegible]	6-14-71
CHECKED	[illegible]	7-26-71
APPROVED	[illegible]	8-9-71
APPROVED	Monaysmith	8-9-71
PEC-3560		

NORTH ELECTRIC COMPANY
POWER EQUIPMENT DIV. GALION, OHIO USA

NS POWER SUPPLY
SCHEMATIC
NORTH ELECTRIC #439966

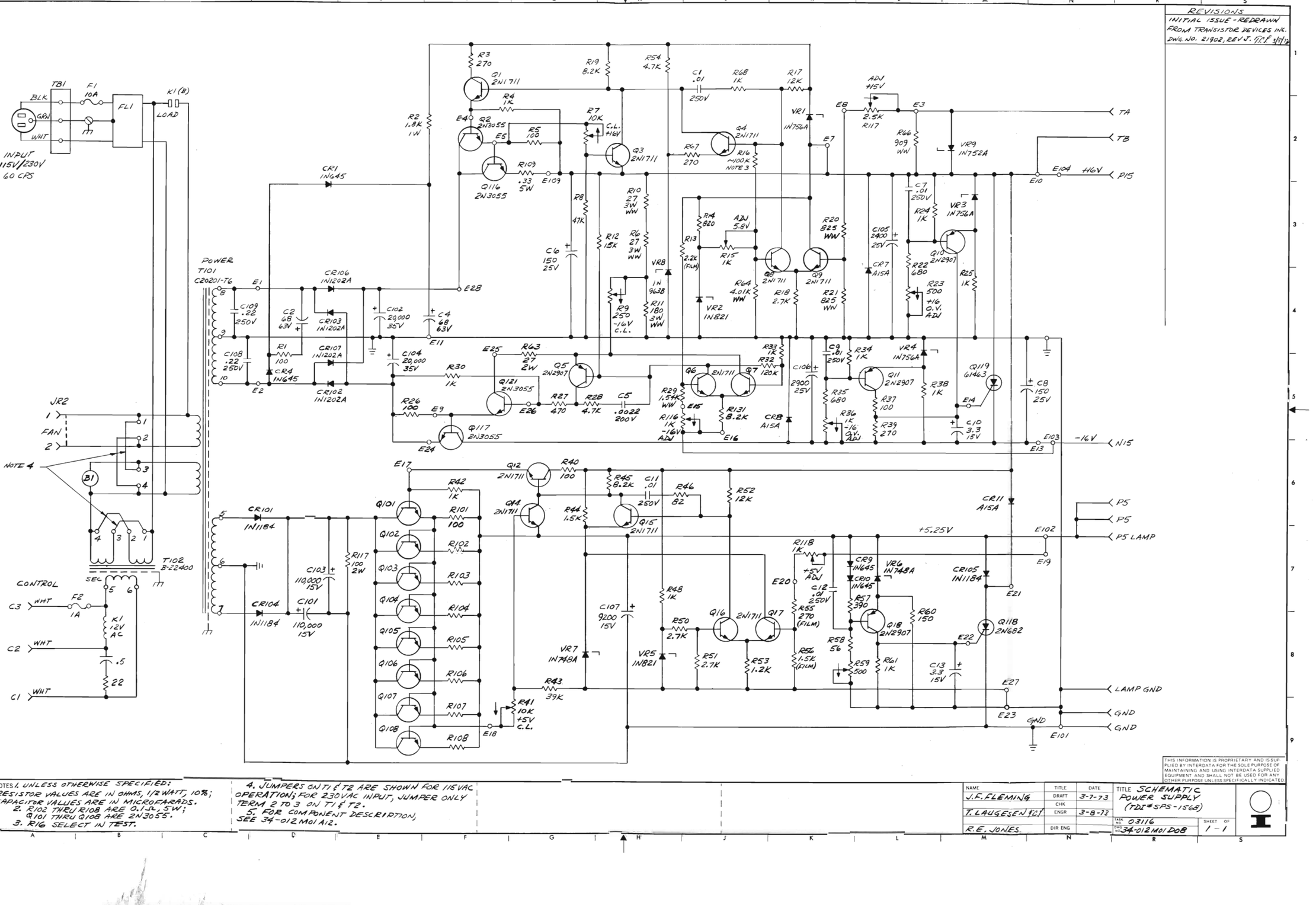
CODE IDENT. NO.	SIZE	34-012R03D08
	D	
SCALE NONE	WEIGHT	SHEET 1 OF 1

439-966

TEST

INTERDATA®

REVISIONS
INITIAL ISSUE - REDRAWN FROM TRANSISTOR DEVICES INC. DWG. NO. 21902, REV J. T.L.F. 3/8/73



NOTES 1. UNLESS OTHERWISE SPECIFIED: RESISTOR VALUES ARE IN OHMS, 1/2 WATT, 10%; CAPACITOR VALUES ARE IN MICROFARADS.
2. R102 THRU R108 ARE 0.1Ω, 5W; Q101 THRU Q108 ARE 2N3055.
3. R16 SELECT IN TEST.
4. JUMPERS ON T1 & T2 ARE SHOWN FOR 115VAC OPERATION; FOR 230VAC INPUT, JUMPER ONLY TERM 2 TO 3 ON T1 & T2.
5. FOR COMPONENT DESCRIPTION, SEE 34-012 M01 A12.

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NAME	TITLE	DATE
J.F. FLEMING	DRAFT	3-7-73
T. LAUGESEN T.C.F.	CHK	3-8-73
R.E. JONES	ENGR	
	DIR ENG	

TITLE SCHEMATIC POWER SUPPLY (TDI # SPS-1568)

TASK NO. 03116 DWG NO. 34-012 M01 D08 SHEET OF 1-1

BRUNING 44-231 16042

INTERDATA®

35-453
P.C. ASSY

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV [illegible]	4/13/73
	PROD [illegible]	5/10/73

REVISED CIRCUITRY					
W2	VCK	3030-001	BS	6-27-73	R01
ADDED RV1 (24-050)					
W2	VCK	3030-004	BS	7-18-73	R02
RELEASED FOR PRODUCTION					
MFG. ENG. [illegible] DATE 10-10-73					
R11 & R12 WERE 5.1Ω					
W2	VCK	3030-005	VG	10-23-73	R03
R66 WAS 1/2 W. (02)					
W2	MH	2026	VG	12-20-73	R04
R11 & R12 WERE 2.4Ω. ADDED C36 & GND SYMBOL. ADDED LEADS TO TB1-8,9. ADDED (2) STRAP OPTION JUMPERS.					
W2	MH	2032 2026	VG	1-17-74	R05
REVISED P.S. FAN & K1 RELAY AREA E1 & D6					
SM	MH	2209	VG	6-18-74	R06

NOTES 1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS-1/4W; CAPACITOR VALUES ARE IN MICROFARADS.

R73 T4
C38 RT2
CR26 RV1
Q13
F6
L3

NAME	TITLE	DATE
J.F. FLEMING	DRAFT	10-25-72
W. ZILLGER	CHK	1-26-73
T. LAUGESEN [illegible]	ENGR	3/9/73
L. PEZZI	MGR	[illegible] 3/13/73
	DIR ENG	

TITLE SCHEMATIC SWITCHING REGULATED POWER SUPPLY

TASK NO. 03020 SHEET OF

DWG NO. 34-017 R06 DOS 1 1

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BRUNING 44231 16042

INTERDATA®

35-510
P.C. ASSY

REVISIONS			
PRE PRODUCTION APPROVAL	INIT.	DATE	
	DEV	12/20/72	
	PROD		
ADDED RBZ RESISTOR			
WE VLA 3051-001	VGA	12-14-73	R01
RGG WAS 1/2 W (D2)			
WE DEH 2026	MA	2-20-73	R02
ADDED C36 & GND SYMBOL. ADDED LEADS TO TB1-8,9. ADDED (2) STRAP OPTION JUMPERS.			
WE DEH 2031	VMA	1-17-74	R03

NOTES 1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS-YAW, CAPACITOR VALUES ARE IN MICRO-FARADS.

RBZ T4
C40 RT2
23026 RV1
Q15
FG
L3

NAME	TITLE	DATE
P. EDWARDS	DRAFT	10-1-73
W. ZILLGER	CHK	
T. LANGE-STN	ENGR	
N. MASI	TEST	
L. PEZZI		

TITLE: SCHEMATIC SWITCHING REGULATED POWER SUPPLY

TASK NO. 03051 DWG NO. 34-020R03D09 SHEET OF 1-1

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BRUNING 44-231 16042

NOTES:

1. WHEN POWERING TWO CHASSIS FROM ONE POWER SUPPLY USE JUMPERS #17-182 F03, F04, F05, F06 & FAN JUMPER #17-181 1 REQ'D PER DETAIL A
2. WHEN CONNECTING TWO 34-012 POWER SUPPLIES IN PARALLEL USE JUMPER 17-182 PER DETAIL B.
3. ADJACENT CHASSIS MUST USE GROUND JUMPERS #17-0176 F00 AS STATED BELOW
   a. ADJACENT 15 IN. CHASSIS TO USE 4 JUMPERS
   b. CHASSIS ADJACENT TO 10 IN CHASSIS TO USE 3 JUMPERS.

CONN RETAINING BAR REF #14-312 A02

15 INCH CHASSIS

10 INCH CHASSIS

SEE NOTE 3

JUMPER 17-182 F03
JUMPER 17-182 F04
JUMPER 17-182 F05
JUMPER 17-182 F06

REF JUMPER #17-181

CONN RETAINING BNR 14-309 A02 REF

DETAIL A
(SEE NOTE 1)

REF. JUMPERS #17-182

DETAIL B
(SEE NOTE 2)

REAR VIEW

NOTES

AREA C & K. JUMPERS SHOWN ON TERM C2 WAS ON C3. SHT 2 AREA #3 17-166 WAS 17-167. AREA L12 DELETED NOTE FOR CABLE 8.	BW	BW	03116-45	1/31/72	155.
AREA J THRU N-14. DELETED RETAINING BAR 14-309 A02	BW	BW	03116-47	1/31/72	R01
NOTE 2 READ WHEN CONNECTING POWER SUPPLIES IN PARALLEL USE JUMPER 17-182 PER DETAIL B SHT. 3 WAS NOT SPECIFIED	PE	RBC	03116-76	4-19-72	R02
CHANGED SHT. 1 TO SHOW COPPER BACK PANEL, DELETED OLD SHT. 2, NEW SHT. 2 WAS SHT. 3. ADDED SHTS. 3 & 4 FOR REF SEE 01-051R02C12 (VOID)	DB		03038-004	MB	3-7-73	R03
LOC GH 67 ADDED JUMPER IDENT, NOTE 1 WAS.. #17-182 4 REQD & FAN--, SHT 3: LOC 4E ADD NOTE FOR RACKO/TACKO PRIORITY. LOC 4M & 4N ADDED NOTE FOR USE OF 17-166 & 17-214 CABLES. LOC 9J CONNECTOR (10" EXP. CHASS.) WAS IN SLOT 5. ADDED NOTE 1. SHT 4: LOC D15 ADD CONNECTOR (15" EXPAN CHASSIS) IN PHANTOM. ADDED NOTE PERTAINING TO PHANTOM CONNECTOR	PE	WAH	2075	MB	2-15-74	R04

	NAME	TITLE	DATE
DRAWN	G. Wellly	MTG	2-1 JAN 72
CHECKED	G. WELLY	ENGR	
ENG APPR.	M. FUCHS	ENGR	
MFG APPR.	R. E. JONES	Q. C.	
RELEASED		DIR ENG	

TITLE: CABLE INFORMATION #3

DOCUMENT NO. 01-051R02C12 REV

SIZE D

SHEET 1 OF 4

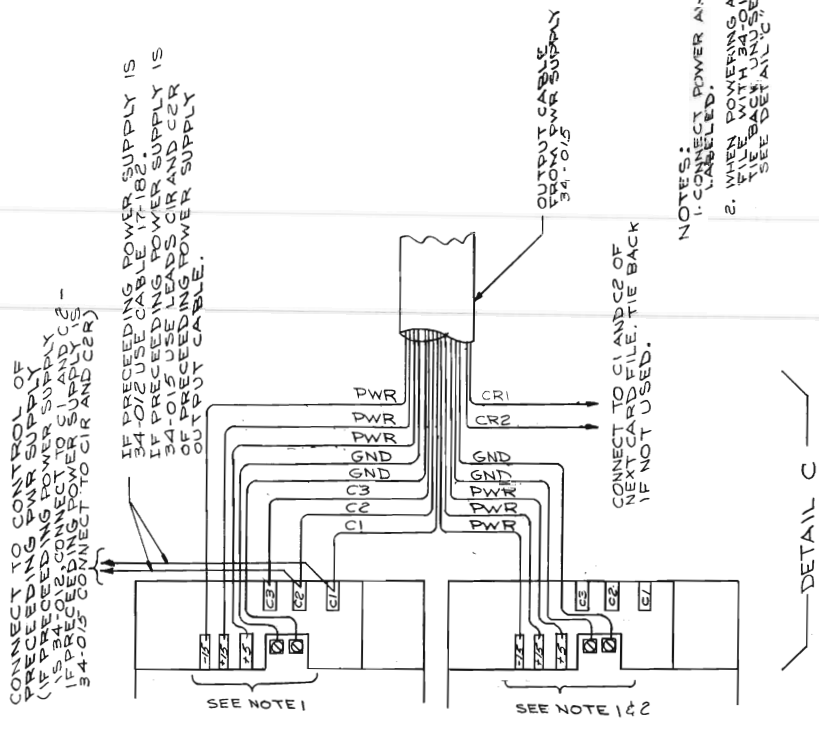
RELEASED TO PRODUCTION
MFG. APPR. [illegible] DATE 2/15/74

DWG. APPR. [illegible] DATE 1/31/72

INTERDATA

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NOTES:
1. CONNECT POWER AND GROUND AS LABELED.
2. WHEN POWERING A SINGLE CARD FILE WITH 34-016 POWER SUPPLY USE 34-016 CABLES. SEE DETAIL C.

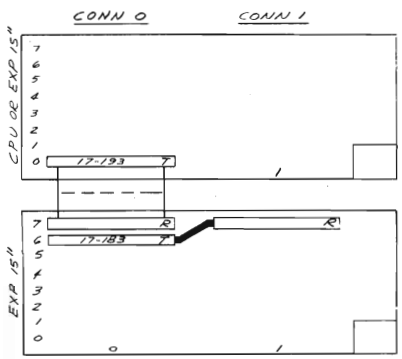


DETAIL C

NOTES	NAME	TITLE	DATE

TITLE CABLE INFORMATION NS
TASK NO. 03116
DWG NO. 21-051R04C12
SHEET 2 OF 4

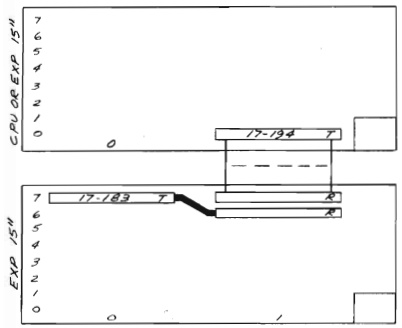
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CABLE : 17-183 & 17-193

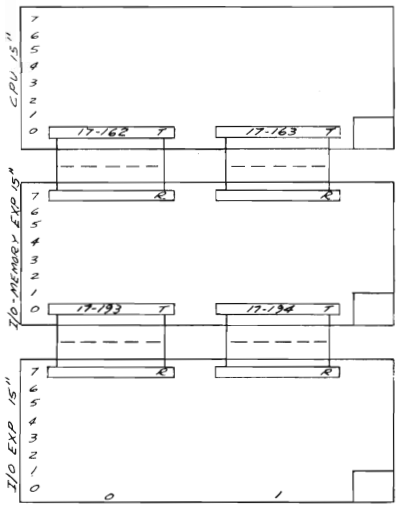
17-183 CABLE IS USED TO CONNECT CONN 0, AND CONN 1 OF THE SAME CHASSIS, IN ORDER TO REGENERATE EITHER THE MUX BUS OR THE BUFFERED OR SELCH BUS. IT USES TWISTED PAIR AND CONTAINS ONLY THE I/O BUS. IT DOES NOT HAVE RACKO/TACKO INCORPORATED.

USED ON:
MOD 80 CPU CHASSIS
UNIVERSAL EXPAN. CHASSIS



CABLE : 17-183 & 17-194

THIS IS A TYPICAL CONFIGURATION USING A 17-183 & 17-194 TO MAKE BOTH CONNECTORS OF A SINGLE CHASSIS THE SAME I/O BUS. THIS CONFIGURATION IS VALID ON THE MOD 80 ONLY IF THE CPU CHASSIS CONTAINS A BUS BUFFER OR SELCH.



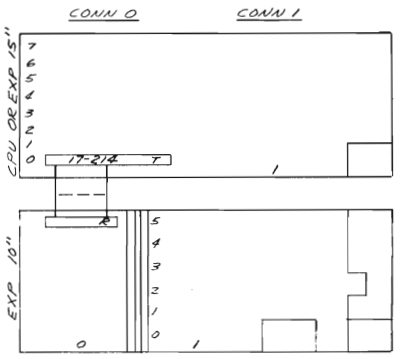
CABLE : 17-162 & 17-163

THESE CABLES ARE USED TO BRING THE I/O BUS AND MEM BUS TO THE ADJACENT CHASSIS. THEY USE TWISTED PAIR AND ARE NOT BUNDLED. THEY CAN ONLY BE USED TO CONNECT THE CPU CHASSIS TO THE FIRST EXPANSION CHASSIS. MUST BE USED IN CONJUNCTION WITH 17-183 ON MOD 80.
17-163 - SEE NOTE 1

USED ON: MOD 70, MOD 74, MOD 80, & UNIVERSAL EXPAN.

CABLE : 17-193 & 17-194

THESE CABLES ARE USED TO CONNECT THE I/O BUS ONLY TO THE ADJACENT "S" EXPANSION CHASSIS. THE 17-193 CABLE IS USED ON CONN 0 AND THE 17-194 HANDLES CONN 1. THEY USE TWISTED PAIR AND ARE NOT BUNDLED.
17-194 MODIFIED - SEE NOTE 1
USED ON:
MOD 70
MOD 74
MOD 80
UNIVERSAL EXPAN.

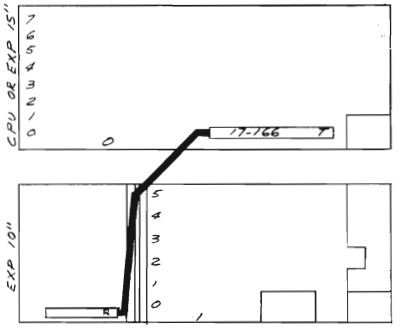


CABLE : 17-214

THIS CABLE IS USED TO CONNECT THE I/O BUS AS IT APPEARS ON CONN 0 TO AN ADJACENT 10" EXPAN CHASSIS. IT IS TWISTED PAIR AND IS NOT BUNDLED. THIS CABLE CONTAINS THE I/O BUS ONLY. D BUS BITS, D080-D150 ARE THE ONLY ONES CARRIED THRU WITH THIS CABLE. (BITS D080-D070 ARE TERMINATED ON THE "S" CONNECTOR END)

USED ON: MOD 70, MOD 74, MOD 80, UNIVER. EXPAN. CHASSIS, & 10" EXPAN. CHASSIS

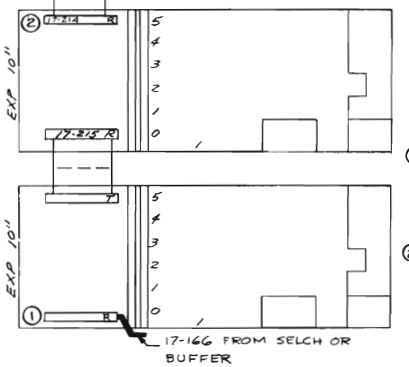
TO MAINTAIN THE BOTTOM TO TOP RACK/TACK PRIORITY ON A 10" EXPAN. CHASSIS, RACKO IS WIRED TO UNUSED PIN 119-0500 IN 10" END OF CABLE & THE 10" CHASSIS CAN BE WIRED FROM 119-0500 TO 114-000.



CABLE : 17-166

THIS CABLE CONTAINS THE I/O BUS, D BUS BITS 8-15, ONLY. IT IS USED TO CONNECT A BUS BUFFER, OR SELCH TO A 10" EXPAN. CHASSIS. THE LENGTH OF THIS CABLE IS 36" WITH DATA LINES AND CONTROL LINES BUNDLED SEPERATELY. DUE TO ITS LENGTH IT MUST BE DRIVEN BY A BUS BUFFER OR SELCH.

USED ON:
MOD 70
MOD 74
MOD 80
UNIVERSAL EXPAN.
10" EXPAN.



CABLE : 17-215

THIS CABLE IS USED TO CONNECT TWO ADJACENT 10" EXPAN. CHASSIS. IT CONTAINS BITS D080-D150 OF THE I/O BUS ONLY. IT IS TWISTED PAIR AND NOT BUNDLED.

① NORMALLY USED WHEN A 17-166 FROM A SELCH OR BUS BUFFER IS DRIVING SLOT 0 OF THE BOTTOM CHASSIS. NO SPECIAL RACK/TACK WIRES NEEDED.

② OR WHEN A 17-214 FROM THE PROCESSOR CHASSIS IS DRIVING SLOT 5 OF THE UPPER CHASSIS, THE "T" END OF THE 17-215 CABLE SHOULD BE ON THE UPPER CHASSIS

USED ON:
10" EXPAN. ONLY

NOTES:
1. ON THE RECEIVE END OF THE 17-163 OR 17-194 CABLES A STRAP IS INSTALLED IN THE FACTORY. THIS STRAP MUST BE OUT UNLESS THE CABLE IS BEING USED TO JUMPER A PRIVATE I/O BUS (SELCH OR BUS BUFFER) TO THE I CONNECTOR ONLY OF THE FIRST EXPANSION CHASSIS. THIS STRAP JUMPERS PIN 222-0001 OF THE CPU CHASSIS TO 122-0701 OF THE FIRST EXPAN. CHASSIS. IF THE 17-163 OR 17-194 IS BEING USED TO EXTEND A SELCH OR BUS BUFFER THE FOLLOWING WIRING CHANGES SHOULD BE MADE TO THE EXPAN. CHASSIS: REMOVE 134-0700 TO 122-0701 & 122-0001 TO 122-0700, ADD 134-0700 TO 122-0001 & 122-0701 TO 122-0700.

NAME	TITLE	DATE	TITLE
			CABLE INFORMATION
			N.S
			SIZE C 03065 DWG NO. 70-000504 REV C2
			SHEET 5 OF 6

INTERDATA

INTERDATA

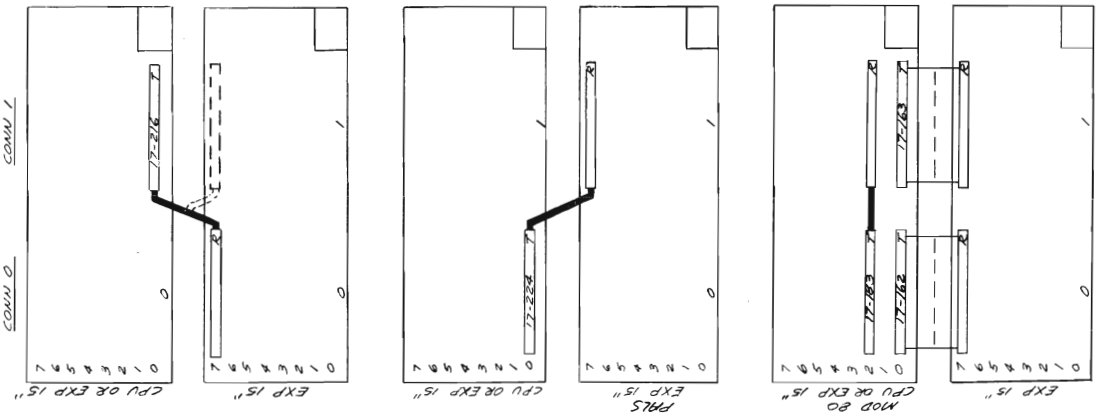
CABLE: 17-216
THIS CABLE IS USED TO CONNECT THE I/O BUS ONLY FROM A 15" CHASSIS TO A 15" CHASSIS. IT MUST BE DRIVEN BY A SELCH OR 36" BUS BUFFER. THIS CABLE IS 36" LONG AND USES TWISTED PAIR WITH THE DATA LINES BUNDLED SEPERATELY CONTROL LINES BUNDLED SEPERATELY IT CAN BE CONNECTED TO THE 0 OR 1 SIDE ON THE SECOND CHASSIS.

USED ON:
MOD 70
MOD 74
MOD 80
15" EXPAN.

CABLE: 17-224
THIS CABLE IS THE SAME AS THE 17-183 EXCEPT FOR THE ADDITION OF RACKO/TACKO. ITS PRIMARY USE IS WITH THE PALS CHASSIS. IT CONTAINS THE I/O BUS COMPLETE WITH RACKO/TACKO ONLY.

USED ON:
MOD 70
MOD 74
MOD 80
PALS EXPAN. CHASSIS

CABLE: 17-162, 17-163, 17-183
THIS EXAMPLE SHOWS THE TYPICAL CONFIGURATION OF THE MOD 80. THE 17-183 CABLE IS INSTALLED ON SLOT 2 CONN 0 TO CONN 1 IN THE STANDARD CPU CHASSIS. IF A SELECTOR CHANNEL OR BUS BUFFER IS INSTALLED IN THE CPU CHASSIS THE 17-183 CABLE MUST BE REMOVED.



NOTES	NAME	TITLE	DATE	TITLE: CABLE INFORMATION N/S
				TASK NO. 03095 SHEET 4 OF 4
				DWG. NO. 01-051R04 C12

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15.380 REF.

14.880 REF.

C51 C52 C53 C54

C48 C47 C46 C45

GRD

NS SELCH 25-367 APP SIDE

48 11 JUMPERS

49

10

2

7

6

1

5

46 INSTALL APPARATUS SIDE (42 PLACES)

A A

SEE NOTE 2

SEE NOTE 3

45

3

9

.530 MAX.

.062 REF.

.125 MAX.

8

PARTIAL VIEW A-A

NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE ITEM 44.
2. STIFFENER BAR (ITEM 3) TO BE SOLDERED TO GROUND BUS AT 2 END POINTS AND CENTER POINT.
3. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

COMPONENT	REF. DESIGNATION
CAPACITOR	C1-21 & 23-60
RESISTOR	R1-36, 38-65 & 67-71
DIODE	D1 THRU D18
I C	A01 THRU A136 & 93A

LAST STRAP NO. 15 (5)

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SCALE 2:1

NAME	TITLE	DATE
R. F. CERO	DRAFT	1-13-73
R. F. CERO	CHECK	1-16-73
D. FRANCISCO	ENGR	2-7-73
H. ROSS	QC	2-7-73
R. E. JONES	MFG MGR	2-7-73

ASSEMBLY N.S. SELECTOR CHANNEL

03075 SHEET

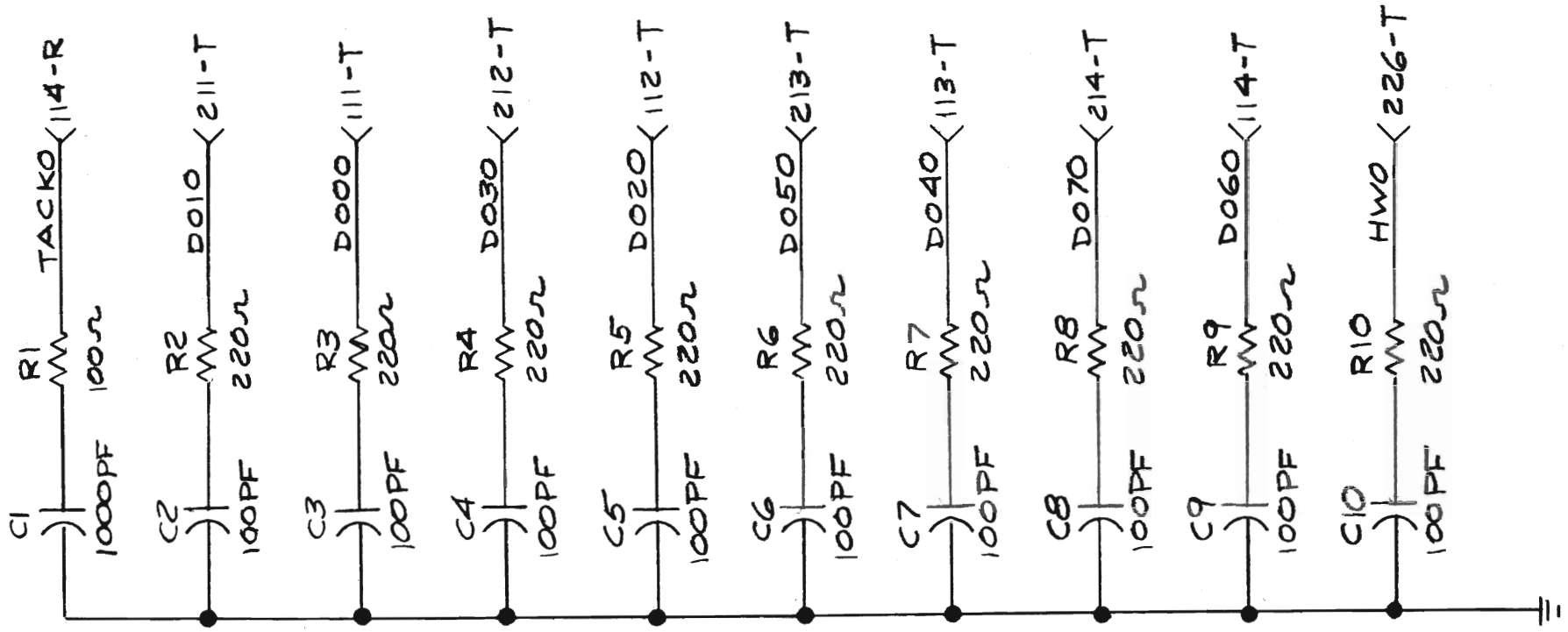
32-351/MOD 2

REVISIONS
ADDED R72 CLN
CHANGED ZIF/WIREWRAP
ADDED STRAPS 14 & 15
CHANGE PA LAYOUT
SEE DOCUMENTS
ADDED: STRAPS 14 & 15

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NOTES

NAME	TITLE	DATE
K.LAFFERTY	DRAFT	9-11-73
H.MATTER	CHK	
H. ROSS	Q.C	3-11-74
D. BOPP	SYS TST	3-12-74
D.FRANKENBERGER	MGR	3-8-74

TITLE FUNCTIONAL SCHEMATIC
FIELD 1 OF A 15" CHASSIS
TO FIELD 0 OF A 10"
CHASSIS

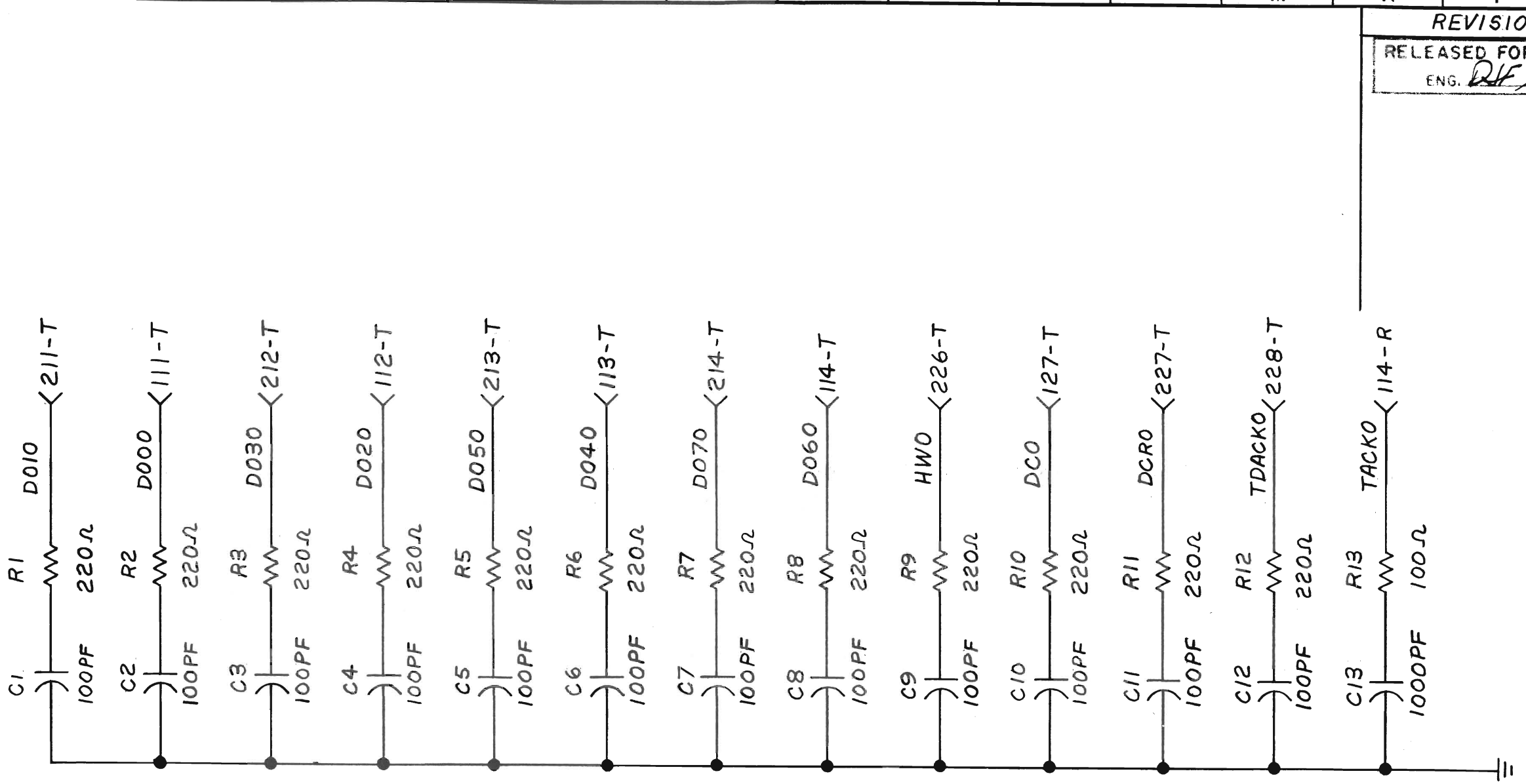
TASK NO. 03095 SHEET OF 1-1

DWG NO. 12-166 B08

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RELEASED FOR PRODUCTION ENG. DLF 4/4 DATE 3-12-74



NOTES

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	9-10-73
H. MATTER	CHK	
H. BOSS	Q.C.	3-11-74
D. BOPP	SYS TEST	3-12-74
D. FRANKENBERGER	MGR	3-8-74

TITLE FUNCTIONAL SCHEMATIC FIELD 0 OF A 15" CHASSIS TO FIELD 0 OF A 10" CHASSIS

TASK NO. 03095

DWG. NO. 17-214 B08

SHEET 1 OF 1

D & W REPROGRAPHICS 40055-2

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STAPLE

STAPLE

Publication Number 29-619

16-BIT EXTENDED SELECTOR CHANNEL (ESELCH) INSTALLATION AND MAINTENANCE MANUAL

INTERDATA®
A UNIT OF
PERKIN-ELMER DATA SYSTEMS
2 Crescent Place, Oceanport, New Jersey 07757 • (201) 229-4040

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September 1977

FOREWORD

This manual provides the necessary information required for the user to install and maintain the 16-Bit Extended Selector Channel (ESELCH). The ESELCH is a Direct Memory Access (DMA) port which can provide block data transfer between a device controller and memory, independent of the processor. The ESELCH can access up to four 64KB blocks of memory for a total of 256KB of memory. It can also operate with only one 64KB block of memory.

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Functional Schematic Drawing, Extended Selector Channel (ESELCH) 35-661D08

Assembly Drawing, Extended Selector Channel (ESELCH) 35-661E03

CHAPTER 1
16-BIT EXTENDED SELECTOR CHANNEL (ESELCH) INSTALLATION

1.1 INTRODUCTION

This chapter provides general information for the installation of the 02-530 Extended Selector Channel (ESELCH) in any INTERDATA Processor System. For installation requirements for specific processors refer to the appropriate processor maintenance manual. The ESELCH is complete on one 35-661 printed circuit board. The processor determines whether the ESELCH is used to access 64KB of memory or up to four 64KB memory segments (256KB maximum) of memory.

1.2 PHYSICAL CHARACTERISTICS

Dimensions: 15-3/8 by 14-7/8".

Weight: 2-1/2 pounds maximum.

1.3 INSTALLATION

The ESELCH may be installed in any even numbered universal expansion slot (i.e., 0, 2, 4, or 6), in the Central Processor Unit (CPU), or in the first Memory I/O Expansion Chassis. See Figure 1-1.

When installing the ESELCH on the 8/16E Processor, the XMAXX memory address bits must be strapped to their respective back panel pin connections to provide the 18-bit address required to access the extended memory, that is:

XMA 140 connects to back panel Pin 208-0.
XMA 150 connects to back panel pin 108-0.

Refer to Functional Schematic 35-661D08 for further information.

NOTE

Connecting the XMAXX memory address bits when the ESELCH is installed on a system limited to 64KB of memory may cause an OR tie of back panel signals resulting in the inability to access memory.

An ESELCH may only be installed in Slots 0, 1, or 2 of a Model 80/85 CPU chassis. Cutting the Multiplexor Bus is not necessary.

When used with the Model 80 or 85, the following options must be exercised:

1. Remove the jumper labeled J located between IC 14 and IC 15.

2. Change the jumper, above IC 53, from (L to X) to (L to 2).

1.3.1 Back Panel Wiring

Multiplexor Channel Bus

At installation, it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the ESELCH and the next higher numbered slot on the One (1) connector only. The RACK0/TACK0 daisy-chain wiring on the back panel is rerouted according to Figure 1.1. The lower numbered card slots in the chassis become part of the private ESELCH I/O Bus on the One (1) connector only.

For the convenience of cutting the Multiplexor Bus, the connections between every other slot are made using top wire wraps. (This refers to interconnections between back panels of Twin Chassis only.) This allows cutting the bus by lifting the top wraps when the ESELCH is installed in the 0 slot. Refer to Figure 1.1 A during the following example.

To install an ESELCH in Slot 4:

1. Remove all wires on Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2. (See back panel map in 35-661 D08 Sheet 1A.)

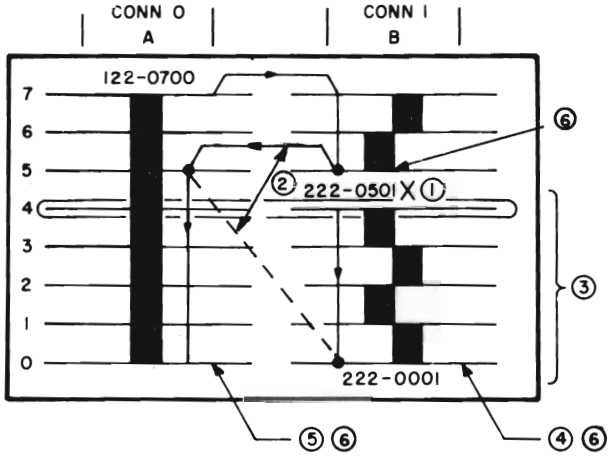
2. Remove the wire between 222-0001 and 122-0700.

3. Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the Zero (0) and One (1) connectors of Slot 4.

4. Connect 122-0700 to 222-0501.

5. Install the ESELCH into Slot 4 of the chassis. The private ESELCH Bus now appears on the Connector One (1) side of Slots 4, 3, 2, 1, and 0. All slots on the Connector Zero (0) side and Slots 7, 6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.

To install an ESELCH in even numbered slots of the lower expansion back panel, a similar procedure is followed. See Figure 1-1B.

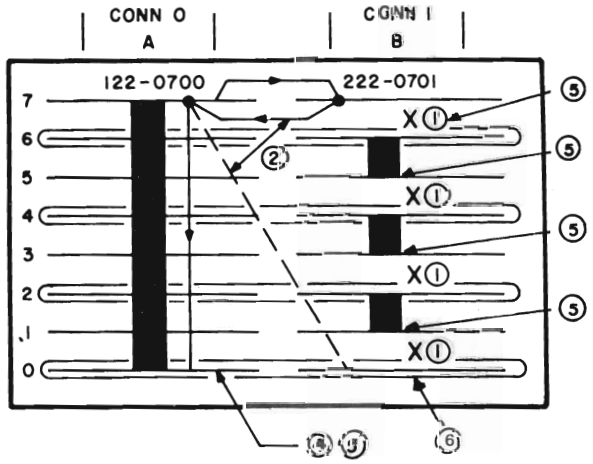


NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A AND B REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.

TO INSTALL AN EXTENDED SELECTOR CHANNEL IN SLOT 4 OF THE CPU BACK PANEL (UPPER).

1. CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.
2. JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.
3. THIS SECTION BECOMES THE PRIVATE EXTENDED SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE, AND SLOTS 7, 6 AND 5 ON CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.
4. IF REQUIRED, EXTEND THE EXTENDED SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.
5. EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.
6. INSTALL 35-433 I/O TERMINATOR

Figure 1-1. A Back Panel Modifications



TO INSTALL 4 EXTENDED SELECTOR CHANNELS (IN SLOTS 6, 4, 2 AND 0) EXPANSION BACK PANEL (LOWER).

1. CUT THE MULTIPLEXOR BUS IN FOUR PLACES.
2. JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.
3. EACH SELCH, EXCEPT THE ONE IN SLOT 0, HAS ONE SLOT AVAILABLE ON ITS PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3 AND 5 ON CONNECTOR ONE (CONN.1) SIDE.
4. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.
5. INSTALL 35-433 I/O TERMINATOR
6. EXTENDED SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

Figure 1-1. B Back Panel Modifications

ACT0/TAC0

The ACT0/TAC0 jumper between Pins 137-0 and 237-0 must be removed from the slot used by the ESELCH controller. If the Extended Selector Channel is not the first Direct Memory Access (DMA) channel on the Memory Bus, Jumper K on the ESELCH controller must be removed. On the Model 6/16 and 8/16E semi-memory systems, memory is the first Direct memory Access (DMA) device (refresh). For these machines, the K jumper must be removed on all Selector Channels.

NOTE

On installations with Multiple ESELCH's, remove the Enable (EN0) and the Inhibit (INH0) filters on all but the last ESELCH. (Remove R70, R72, C72, C59, and C61.)

1.3.2 Cabling

The cabling required for the ESELCH depends on the systems' physical configuration. When the private ESELCH I/O Bus does not extend outside the chassis, no cabling is required. When the private ESELCH I/O Bus must be extended to another chassis, a number of cable configurations can be used. See Figure 1-2. Care should be taken to minimize bus lengths.

1.4 ADDRESS STRAPPING

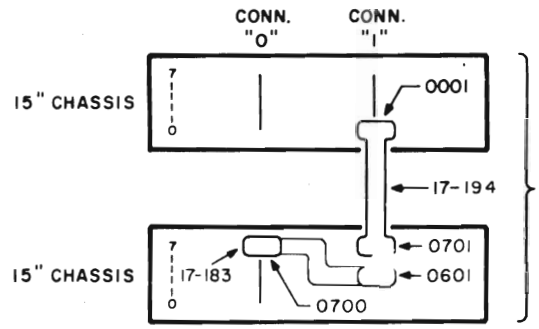
The preferred address of the Extended Selector Channel is X'F0'. The controller is strapped for this address at the factory. To change the address refer to Functional Schematic 35-661D08. The number and letter designations shown on the schematic refer to the designations on the apparatus side of the ESELCH controller board.

1.5 BUS TERMINATION

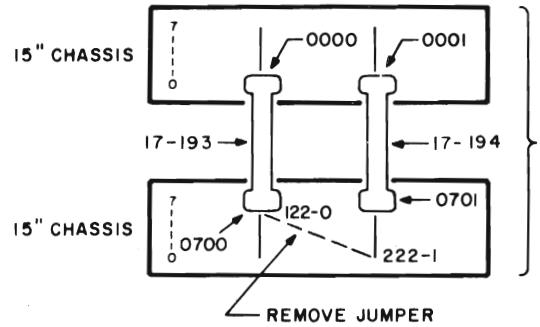
The private ESELCH Bus is terminated by installing a 35-433, 15" Bus Terminator, on the back panel, at the last slot where the bus exists on any configuration where the private ESELCH Bus extends more than four slots.

1.6 INSTALLATION CHECKS

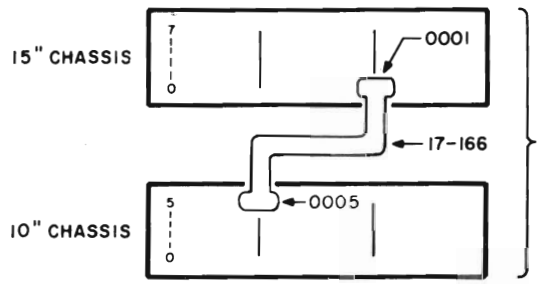
Perform the installation check by running the 16-Bit Extended Selector Channel (ESELCH) Test Program, 06-222 according to the test program description.



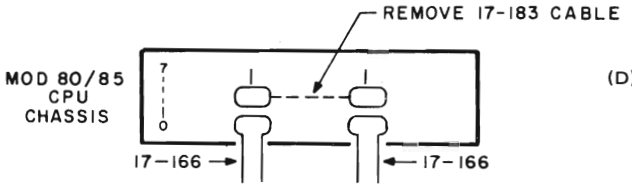
(A) CONNECTS TWO ADJACENT 15" CHASSIS. THE PRIVATE ESELCH BUS APPEARS AT BOTH CONNECTORS 0 AND 1 OF THE LOWER CHASSIS. NOTE THE DATA CHANNEL DOES NOT APPEAR IN THE LOWER CHASSIS.



(B) USED TO CONNECT TWO ADJACENT 15" CHASSIS. THE MULTIPLEXOR BUS APPEARS AT CONNECTOR 0, AND THE ESELCH BUS APPEARS AT CONNECTOR 1. WHEN USING THIS CONFIGURATION, THE RACKO/TACKO JUMPER FROM 122-0, SLOT 7, TO 222-1, SLOT 0, MUST BE REMOVED FROM THE LOWER CHASSIS.



(C) CONNECTS THE PRIVATE ESELCH BUS TO A 10" CHASSIS ONE OR TWO CHASSIS AWAY.



(D) CONNECTS THE PRIVATE ESELCH BUS AND THE MULTIPLEXOR BUS TO A 10" CHASSIS, ONE OR TWO CHASSIS AWAY.

Figure 1-2. Cabling

CHAPTER 2
16-BIT EXTENDED SELECTOR CHANNEL (ESELCH) OPERATION

2.1 INTRODUCTION

The 02-530 Extended Selector Channel (ESELCH) is a Direct Memory Access (DMA) port which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the processor. The processor sets up the device controller, loads the ESELCH with the starting and final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO and Block Boundary Command. The ESELCH then handles the transfer without further direction by the processor.

The Extended Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The ESELCH provides the drivers and receivers for the private ESELCH I/O Bus. This bus originates at Connector One (1) of the ESELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private ESELCH I/O Bus can be extended to other chassis. For installation information, refer to ESELCH Installation (Paragraph 1.3) and the installation information pertaining to the processor in use.

2.2 SCOPE

This chapter describes the operation of the ESELCH in its various modes; Set Up, Memory Read, Memory Write, and Termination. Where necessary, this chapter references the Multiplexor Channel Bus and Memory Bus operations.

2.3 BLOCK DIAGRAM ANALYSIS

See the ESELCH block diagram on Sheet 1A of Functional Schematic 35-661D08 and the ESELCH Flow Chart, Figure 2-1, during the following analysis. Before initiating a data transfer via the ESELCH, the device controller and the ESELCH must be set up. The set up procedure is implemented by the processor via the Multiplexor Bus (MPX-Bus). When the ESELCH is in the idle mode, the MPX-Bus is tied directly to the private ESELCH I/O Bus through the ESELCH. This allows the processor to communicate directly with any device on the private ESELCH I/O Bus.

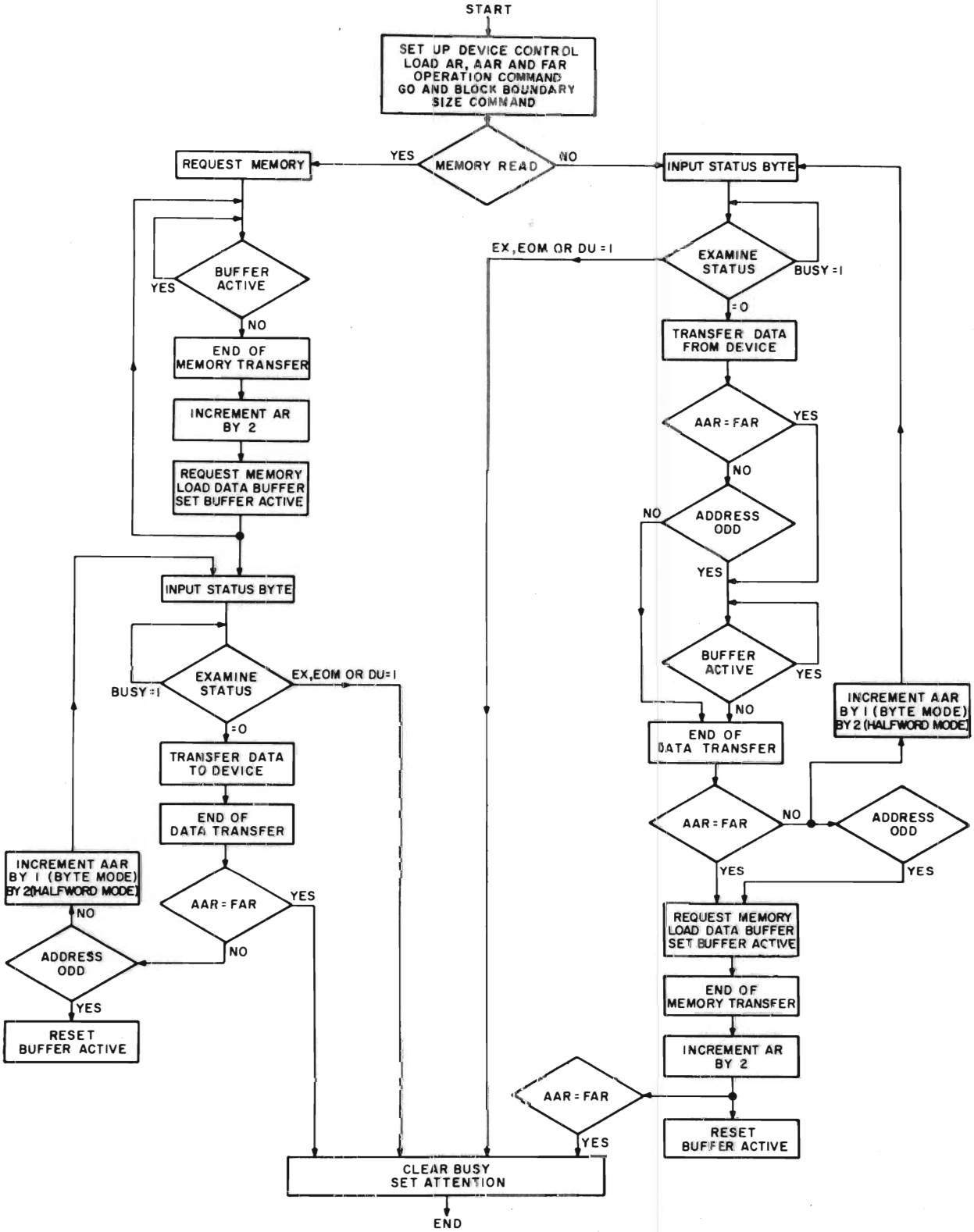


Figure 2-1. ESELCH Flow Chart

To prepare the ESELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines (D080:150) by four consecutive Data Availables (DAs) from the processor. The first two Data Availables simultaneously load the AR and AAR, which are 16-bit incrementing registers. The AR is incremented, by two, after each halfword is transferred to/from memory, and the AAR is incremented, by one, with each byte transferred to/from the device. Data transfer is terminated when the AAR is equal to the FAR or when the AAR increments past its maximum value, X'FFFF'. This feature is independent of the block boundary setting.

Data transfer begins by the processor issuing a GO and Block Boundary Command to the ESELCH. At the same time, information pertaining to the addressed memory segment (one of four 64KB blocks of memory) is transferred from the ESELCH and loaded into the designated memory segment (Block Boundary). Transfer to/from the device is now independent of the processor. The GO Command prevents communication between the processor and any device on the private ESELCH I/O Bus until the present transfer is terminated and the ESELCH is addressed.

Data transfer is controlled in the Move Data circuit by inspection of the four least significant bits of the Status Byte presented by the active device on the private ESELCH I/O Bus. When any one of the three least significant bits is set (EX, EOM, or DU), the transfer is terminated. Bit 12 (Busy) regulates the rate of data transfer. In the Memory Read mode, the actual data transfer begins with a memory request, REQ0 active, as soon as a GO and Block Boundary Command is issued. When the memory request is serviced by the processor, the ESELCH Memory Bus control circuit activates Select (SEL), which gates the contents of the Address Register (AR) onto the Memory Address Bus, and gates a halfword of data from memory into the Data Register (DR). At the termination of the memory transfer, the data is loaded from the DR to the Data Buffer (DB) and the AR is incremented.

NOTE

> Unless the ESELCH has dropped REQ0 in time to remain selected during the next memory cycle, the ESELCH is deselected by the rising edge of Inhibit (INH0) after the halfword has been transferred.

Once the DB is loaded, the data transfer to the device over the Private Data Lines (PD000:150) is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and the contents of the Final Address Register, or until the transfer is aborted due to a device status error condition.

In the Memory Write mode, the data transfer sequence described previously for Memory Read mode is reversed. That is, two bytes of data are loaded into the DR from the device, prior to a memory request, and the data flow is from the device to the DR, DR to the DB, and finally into memory.

The Branch Gate and the Move Data circuits control the flow of data between memory and the device. The Branch Gate supervises the overall data flow, while the Move Data circuit generates the control between the ESELCH and the active device on the private ESELCH I/O Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the ESELCH Busy flip-flop, which is presented to the program as Bit 12 of the ESELCH Status Byte.

Table 2-1 shows the Extended Selector Channel Status and Command Byte Data.

TABLE 2-1. EXTENDED SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP		XMA 140	XMA 150

BSY — When this bit is set, a one shot generates the End of Busy Set pulse (EBS1) to start the appropriate ESELCH operation. When this bit is cleared, an interrupt is generated.

READ — This command, Bit 10, sets the Memory Write (WT) flip-flop. The controller on the private ESELCH I/O Bus is set up for a device Read operation.

GO — This command, Bit 11, clears the Multiplexor ESELCH Control (MSC) flip-flop and sets the BSY flip-flop to initiate the Data Transfer mode.

STOP — This command, Bit 12, from the processor clears the BSY flip-flop and initializes the Load/Unload Sequencer. During the Data Transfer mode, execution of the command is delayed until the end of a memory cycle, if one is in progress.

XMA14
XMA15 — The combination (active = 1, inactive = 0) of Command Bits 14 and 15 (XMA140 and XMA150) define the 64KB memory segment where the Write or Read operation is to occur. See Table 2.2.

TABLE 2-2. COMMAND BITS 14 AND 15

XMA		MEMORY SEGMENT	MEMORY ADDRESS
140	150		
0	0	0	X`00000´ to X`0FFFF´
0	1	1	X`10000´ to X`1FFFF´
1	0	2	X`20000´ to X`2FFFF´
1	1	3	X`30000´ to X`3FFFF´

XMA140 and XMA150 must be specified in the same command byte that commands the ESELCH to perform a Write or Read and GO operation.

XMA140 and XMA150 must be reset when a Stop command (Bit 12 set) is issued to the ESELCH.

2.4 FUNCTIONAL DIAGRAM ANALYSIS

2.4.1 Introduction

This section relates to Functional Schematic 35-661 D08, Sheets 1 through 6. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example, D080 is Data Line Number 8 (D08). The last character (0) indicates that when D080 is active, the line is at a logical Zero level.

2.4.2 ESELCH Control Circuit

In the Idle mode, the ESELCH Address (2M8), Busy (3F3), and Multiplexor-ESELCH control (MSC) (3F4) flip-flops are reset, and the private ESELCH I/O Bus is tied directly to the Multiplexor Bus. This allows the processor to communicate, via the Multiplexor Bus, with any device on the private ESELCH I/O Bus.

To communicate with the ESELCH, it must first be addressed. The ESELCH Address (X`F0´ preferred) is placed on the Data Lines (D080:150) (1A3-8) and the Address control line is activated (ADRS0) (4B8). The ESELCH Address is decoded by the four input NAND gate (1F4) and the Address flip-flop is set (2M8). The set output from the Address flip-flop (AD1) (2J7), when active, prevents the control signals on the MPX-Bus from passing onto the private ESELCH I/O Bus by holding the Control Line Gate inactive (CLG1) (1B2). The capacitors in area 4D8 delay the propagation of the Private Address control line (PADRS0) (4F9) to the private ESELCH I/O Bus, so that when the ESELCH is being addressed, PADRS0 does not become active. This delay allows the ESELCH to be addressed without resetting the Address flip-flop of the active device on the private ESELCH I/O Bus.

The simultaneous loading of the Address Register (AR) and Auxiliary Address Register (AAR), and the loading of the Final Address Register (FAR) is accomplished by four consecutive Data Availables (DAs) from the processor. The Load/Unload Sequence (2L2) controls the loading of these registers (AR, AAR, and FAR) and the unloading of the AAR. The sequencer is set to its initial state by the termination of the last data transfer, a Stop Command, or a System Clear (SCLR0) (4M5); so, the first DA, through the Data Available Gate (DAG0) (2L4), activates Load Address Register High (LARH0) (2S2).

LARH0 gates the Data Lines (DA08I:15I) (Sheet 1) into the eight most significant bits of the AR and AAR. The rising edge of the first and each successive Data Available Gate (DAG0) (2L4) increments the sequencer and allows the next DA to activate the next load line. The second DA loads the eight least significant bits of these registers. The third and fourth DAs then load the Final Address Register in the same order. The contents of the AAR may be inspected, via the program, by issuing two Data Requests to the ESELCH whenever the Load/Unload Sequencer is in its initial state. (e.g., Upon termination of an ESELCH transfer, sequencer initialized, the FAR may be inspected to determine if the entire block of data has been transferred.)

If a Memory Write operation is desired, an Output Command with Bit 10 set must be issued to set the Write flip-flop (3F5). Since the Write flip-flop is reset by the Data Available/Request Gate (DARG1) (2L5) whenever a DA or Data Request is sent to the ESELCH (set up procedure), no command is necessary to initiate a Memory Read operation.

Data transfer commences with a GO and Block Boundary Command from the processor, which is an Output Command with Bit 11 set. The GO and Block Boundary Command sets the Busy (3F3) and MSC (3F4) flip-flops. The setting of the Busy flip-flop causes an End of Busy Set pulse (EBS1) (3H4) to be generated. This pulse is generated from the falling edge of BSY0 (3F3) and it is used by the Branch Gate circuit to initiate the transfer cycle. The Busy latch circuit remains set until the Extended Selector Channel detects the termination of transfer and its state is presented to the program via Bit 12 of the Sense Status Byte.

The MSC flip-flop is reset by SCLR0A or by addressing the ESELCH, Set Gate active (SGAD1) (2L9), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the Extended Selector Channel.

Information is steered from the ESELCH to the Data Lines (D080:150) (Sheet 1) and the Private Data Lines (PD080:150) (Sheet 1) by the proper gating of four each, four-to-one line multiplexors (Sheet 1). For example, with the ESELCH idle and Busy reset, all Data Lines are tied directly to the Private Data Lines in both directions.

2.4.3 Memory Bus Control Circuit

Memory Bus Control timing relationships are shown in Figure 2-2. An ESELCH request for memory is started by activating Set Request (SREQ0) (3S4). SREQ0 is activated by the Branch Gate circuit (3M8) when either the ESELCH has received a halfword of data from the device or, in the Memory Read mode, whenever the Memory Data Register is available to accept the next halfword.

SREQ0 is applied to the direct set input of the Request flip-flop (REQ) (4L5) which sets the flip-flop and sends REQ0 to the processor. When REQ0 is received, the processor generates Enable (EN0). EN0, on the first DMA device, is jumpered to Accept (ACT0) which generates the daisy-chain priority loop through all DMAs in the system. The daisy-chain begins at the highest priority DMA as EN0, and propagates to the lower priority DMAs as Transmit Accept (TAC0) until it is captured by the first DMA requesting a memory cycle. When the REQ flip-flop is set and ACT0 (EN0) is active, the ACT0/TAC0 contention circuit (4H2) blocks the propagation of TAC0 and provides highs on the J input to the SEL flip-flop and the K input to the REQ flip-flop. Thus, on the rising edge of EN0, the Select flip-flop becomes set and the Request flip-flop is reset. When the ESELCH REQ flip-flop is reset and ACT0 (EN0) is active, the ACT0 signal is propagated as TAC0 to the DMA with a lower priority.

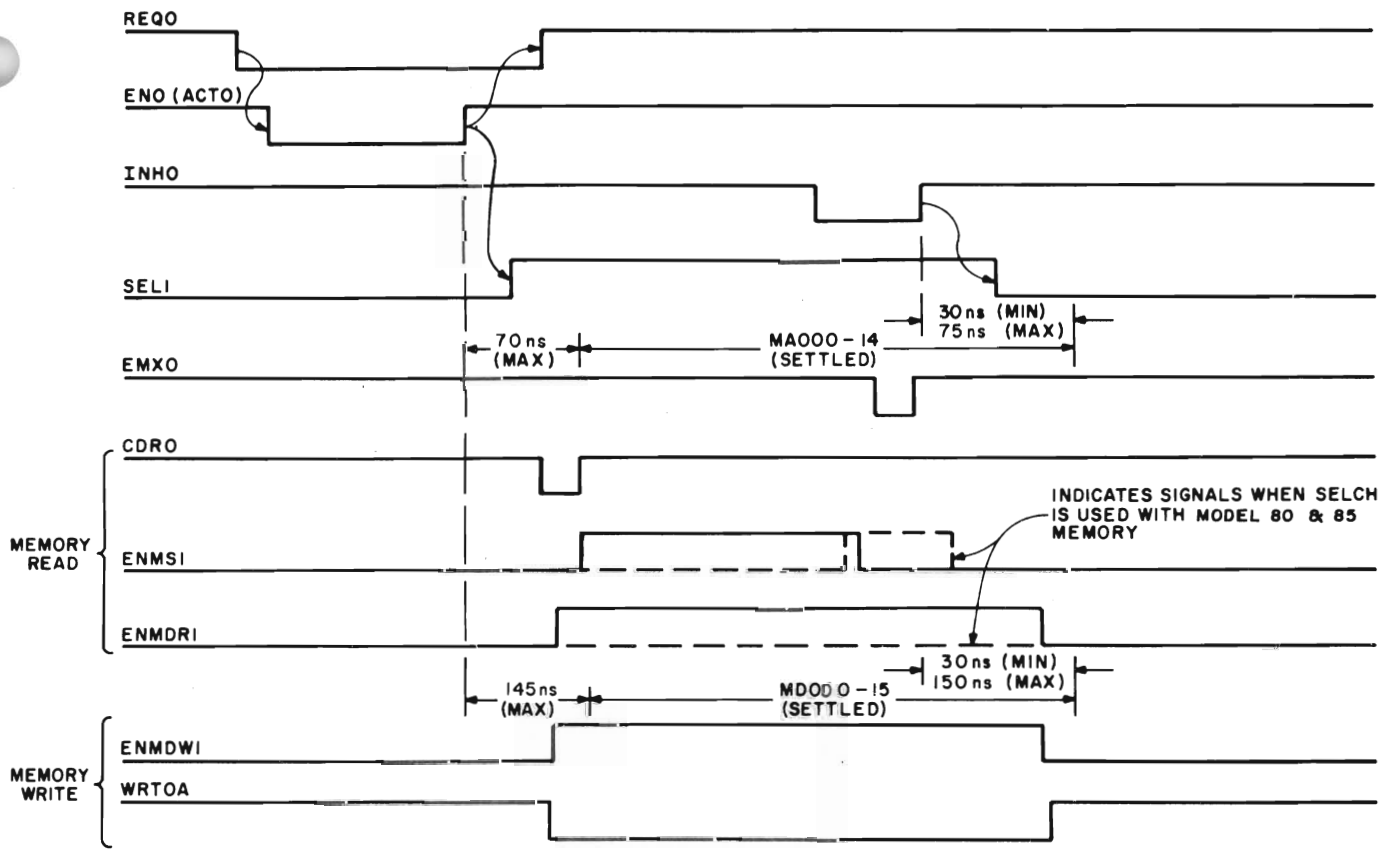


Figure 2-2. Memory Bus Control Timing Diagram

The trailing edge of Inhibit (INH0) (4H5), from the processor, indicates the end of the memory cycle. This edge, unless the ESELCH has dropped REQ0 in time to remain selected during the next cycle, causes the SEL flip-flop to reset. The End of Memory Transfer (EMX0) (4M7) is used by the Branch Gate circuit to indicate the end of the memory transfer. The Address Register is toggled by the AND function SEL1 and INH1 and the Load Data Buffer (LDB) (3S7) is enabled.

In the Memory Read mode, the Memory Data Register (MDR) is cleared by Clear Data Register (CDR0) (4R2) which is generated by the trailing edge of REQ1. Memory Write (WT0A) (3F5) is ANDed with SEL1 to form Enable Memory Data Read (ENMDR1) (4R6), which gates the contents of the MDR onto the Memory Data Lines (MD000:150) (Sheet 6) for the restore portion of the memory cycle. (This function is disabled when using solid-state memory.) The contents of the memory location accessed is gated to the direct set inputs of the MDR by Enable Memory Strobe (ENMS1) (4R4). This function is WT·SEL·CDR0 for use with core memory and WT·SEL·INH when using solid-state memory (4R4).

When writing to memory, the contents of the Data Buffer is gated onto the Memory Data Lines (MD000:150) (Sheet 6) by Enable Memory Data Write (ENMDW1) (4R3). A Memory Write operation is indicated to the processor by activating WRT0A (4S3).

2.4.4 Address Register and Auxiliary Address Register (AR) (AAR)

The Address Register (AR) and Auxiliary Address Register (AAR) (Sheet 5) each consist of four 4-bit counters. These registers are loaded simultaneously by the processor from the Data Lines (D080:150) (Sheet 1) under control of the Load/Unload Sequencer (see Section 2.4.2), with the block transfer starting address. The content of the AR (Sheet 5) is gated onto the Memory Address Lines (MA000:140) (Sheet 5) whenever the ESELCH is selected, SEL flip-flop set. The AR is incremented with each memory transfer by Select Inhibit (SINH0) (4K8). The AAR (Sheet 5) keeps track of the transfer between the ESELCH and the device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0) (3M1). In the halfword mode, TAAR0 is generated twice for each transfer. The outputs of the AAR are used by the Match circuit to determine the end of the data block. Its contents may be examined, via the program, by issuing two consecutive DRs to the ESELCH when the sequencer is initialized. In addition, AAR151 is used in the Byte Transfer mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the AAR (CO0) (5A1) terminates the transfer, clear Busy, when a transfer is attempted past the maximum memory address. This feature prevents 'wrap-around' in memory.

2.4.5 Final Address Register (FAR)

The Final Address Register (FAR) is implemented by four quad latches (Sheet 5.). This register, like AR and AAR, is loaded by the processor under control of the Load/Unload Sequencer. The outputs are used exclusively by the Match circuit to determine when the final address of the transfer is reached.

2.4.6 Memory Data Register and Data Buffer (MDR) (DR)

The Memory Data Register (MDR) (Sheet 6) is a 16-bit register composed of 16 edge-triggered JK flip-flops. In the Memory Read mode, the MDR is first cleared by Clear Data Register (CDR0) (4R2) and then direct set by each active bit on the Memory Strobed Data Lines (MS000:150) (Sheet 6). During a Memory Write, the data, present in double rail format at the J and K inputs to the MDR, is toggled into the flip-flops on the trailing edge of either Load Data Register High (LDRH0) (6A9) or Load Data Register Low (LDRL0) (6J9).

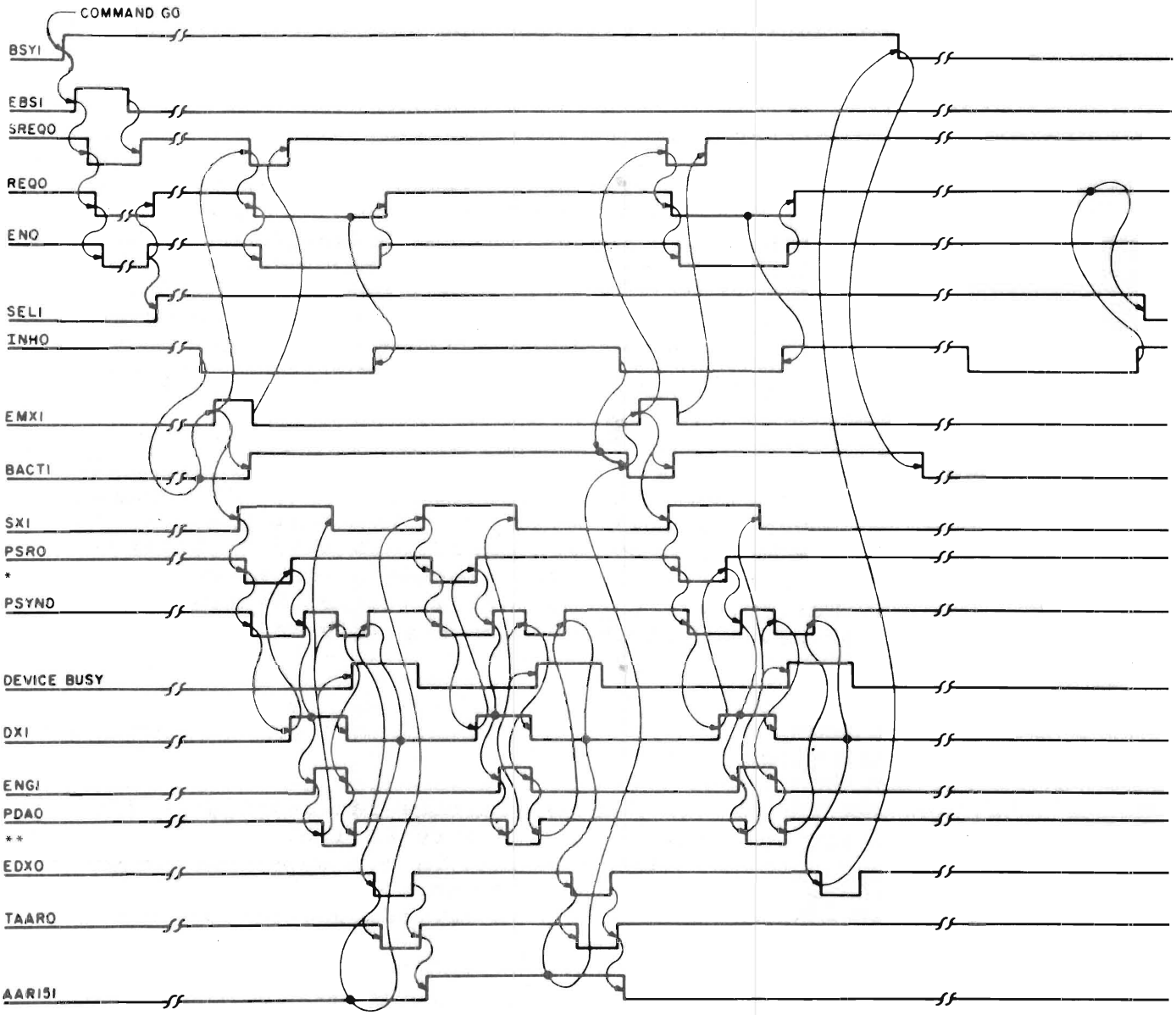
As soon as the MDR is loaded, if the Data Buffer (DB) is empty, as determined by the inactive state of the Buffer Active flip-flop (3H1), the MDR content is loaded into the DB (Sheet 6) by Load Data Buffer (LDB1) (3S7). Information present in the DB is, in turn, either written into memory via the Memory Data Lines (MD000:150) or sent to the device on the Private Data Lines (PD000:150).

2.4.7 Data Transfer Circuit

Refer to Figure 2-3 for Memory Read timing diagram and Figure 2-4 for Memory Write timing diagram. The Memory Read timing diagram shows the timing of a three byte transfer, in the Byte mode, of 2,000,000 bytes/second. Figure 2-4 shows a transfer of two halfwords, in the Halfword mode, to a slower device.

A GO and Block Boundary Command to the Extended Selector Channel sets the Busy flip-flop which generates the End of Busy Set pulse (EBS1) (3K8).

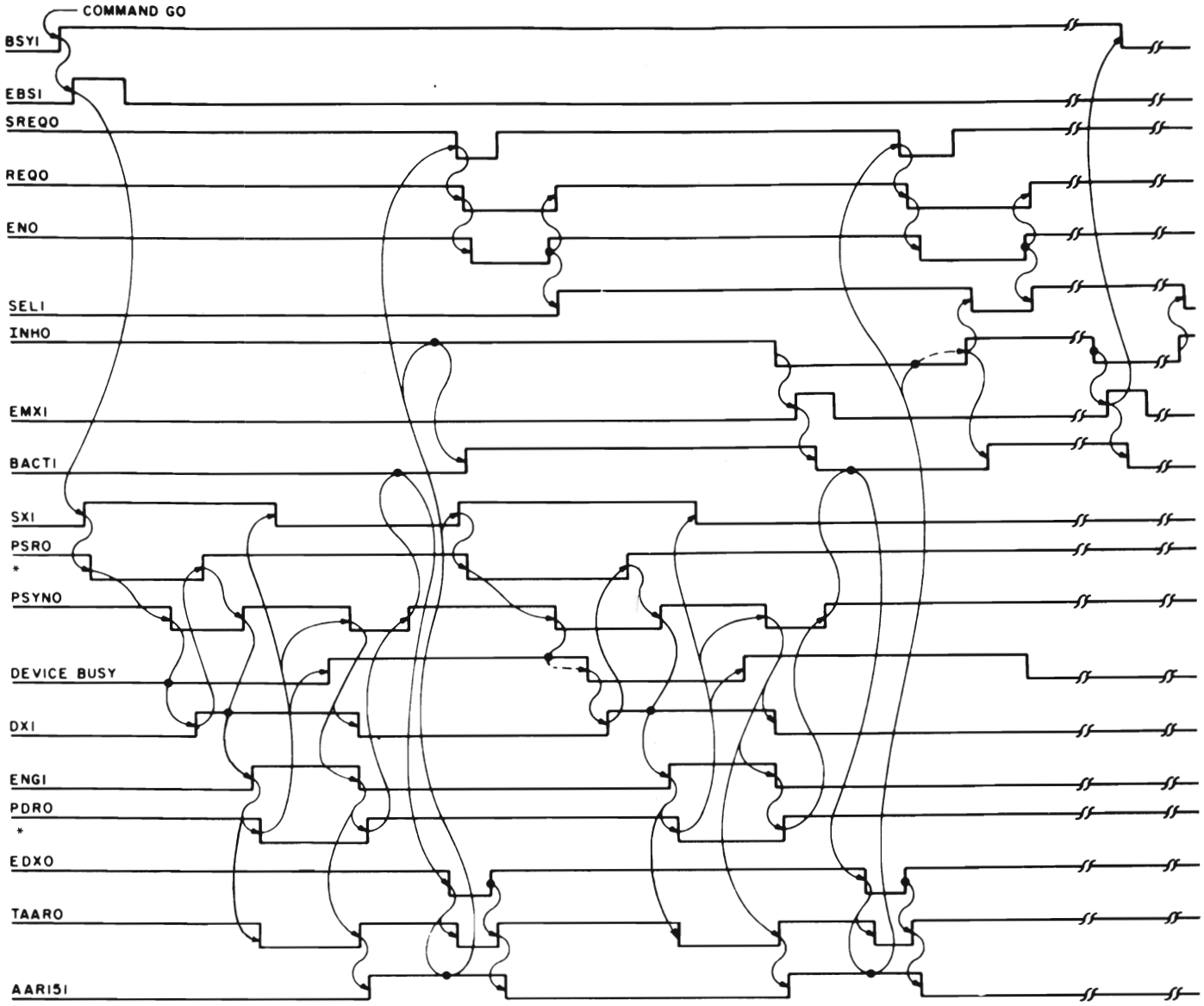
In the Memory Read mode, EBS1 is decoded by the Branch Gate circuit and SREQ0 is generated. Thus, a request for memory is initiated. When the halfword of data is present in the MDR, the End of Memory Transfer pulse (EMX1) (4R6) becomes active and the Branch Gate circuit once again requests memory and generates Set Status Transfer (SSX0) (3S5) and Load Data Buffer (LDB1) (3S7). These signals initiate the transfer to the device and load the Data Buffer (DB) respectively.



*Data must be settled prior to the device activating PSYN0 for the particular control line, and the data must remain active until PSYN0 is removed.

**The ESELCH will maintain data on the bus prior to activating the PDA0 control line, and keep it active until PSYN0 is returned from the active device.

Figure 2-3. Memory Read (Byte Mode)



*Data must be settled prior to the device activating PSYNO for the particular control line, and the data must remain active until PSYNO is removed.

Figure 2-4. Memory Write (Halfword I/O Mode)

SSX0 sets the Status Request flip-flop (SR) (3F6) which activates the Private Status Request control line (PSR0) (3G6) to the active device on the private ESELCH I/O Bus. This Status Request examines the four least significant bits of the Status Byte. If any of the three least significant bits (EX, EOM, or DU) is set, the transfer is terminated by resetting the Busy flip-flop (3F3). It is assumed that each of these status bits remain reset for the remainder of this discussion. With Bit 12 (Busy) of the Status Byte reset, the Data Transfer flip-flop becomes set (3F7). Data Transfer (DX0) (3E1) inhibits the generation of PSR0, which causes Private Sync (PSYN1) (4B4) from the device to become inactive. This enables Engage to go high (ENG1) (3D8), which allows the Private Data Available control line (PDA0) (3H5) to become active. The Private Data Available/Request signal (PDAR1) (3H5), generated whenever a Private Data Available (PDA0) or Private Data Request (PDR0) signal is active, then clears the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset, and ENG1 goes low, disabling PDA0. When the Sync is removed by the device, an 80 nanosecond End of Data Transfer pulse is generated (EDX0) (3J8), which increments the Auxiliary Address Register and uses the Branch Gate circuit to generate a function in accordance with the truth table for EDX on Sheet 3. This cycle continues until termination of the transfer is detected.

In the Memory Write mode, WT1 active (3F5), EBS1 is used to generate SSX0, and the Branch Gate circuit directs the loading of a halfword of data into DB before a memory request is made. The transfer of data from the device is the same as described in the Memory Read mode, except that ENG1 is used to generate the Private Data Request control line (PDR0) (3H5) rather than PDA0. Data from the device is loaded into the MDR on the trailing edge of either Load Data Register High (LDRH0) (2R2) or Load Data Register Low (LDRL0) (2R2), depending on which 8-bits are being loaded. In the Halfword Transfer mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (3H8) when the Buffer Active flip-flop is set (BACT1) (3H1), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0) (5J2). This prevents the reloading of the Data Buffer (DB) before the last halfword has been written into memory.

2.4.8 RACK0/TACK0 Contention Circuit

The Extended Selector Channel directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus (TACK0) and to devices on the private ESELCH I/O Bus (PTACK0). If the Extended Selector Channel Attention flip-flop (4B4) is set, the ESELCH captures the Receive Acknowledge signal (RACK0) (4B3), places its device address on the Data Lines and returns Sync to the processor, Attention Sync (ATSYN0) (4F4) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0) (4F2) or Transmit Acknowledge (TACK0) (4F3). Since devices on the private ESELCH I/O Bus have a higher interrupt priority than devices below the ESELCH on the MPX Bus, if the Private Attention Test line is active (PATN0) (4B1), PTACK0 is generated rather than TACK0. Note that when MSC0 is high (3F4), PATN0 is disabled so that a device on the private ESELCH I/O Bus may not interrupt the processor while the ESELCH is active.

2.5 MAINTENANCE, TROUBLE SHOOTING, AND TEST

Before attempting any maintenance or testing, insure that the necessary back panel modifications and ESELCH board option strapping have been made according to the Extended Selector Channel Installation. See Chapter 1.

To insure a 2 megabyte/second transfer rate in the Byte Transfer mode, limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0) to 30 nanoseconds. In addition, the device must be ready for the next byte of data, Busy Status bit reset, whenever a Status Request is made. Field testing of this device is contingent upon the user having the appropriate software and hardware available to exercise the Extended Selector Channel. There are no adjustments associated with this device. Do not install Terminator Board, 35-433, on the private ESELCH I/O Bus if a transfer rate of 2,000,000 Bytes/second is to be maintained in the Byte (8-bit) mode. The private ESELCH I/O Bus should be contained on a single 15-inch chassis if no terminators are used.

2.6 MNEMONICS

The following list provides a brief description of each mnemonic found in the ESELCH. The source of each signal on Functional Schematic 35-661 D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:151	Outputs of the Auxiliary Address Register	Sheet 5
ACT0	Accept - Request for memory accepted by processor	4H1
AD1	Address - Active when ESELCH is addressed	2K7
ADRS0	Address Control Line from MPX-Bus	4B8
AG081:151	Address Gated Lines - Output of Address Strap	Sheet 1
ATN0	Attention - Attention to Processor	4F1
ATSYN0	Attention Sync - Generated by an Acknowledge Attention from processor	4F4
BACT1	Buffer Active - Indicates that valid date is present in the Data Buffer (DB)	3H1
BSY1	Busy - Indicates a data transfer is in progress	3F3
CBSY0	Clear Busy - Terminates transfer when a match is detected	3M3
CDR0	Clear Data Register - Clears MDR prior to loading from MS000:150	4R2
CL070	Control Line 7 - Control Line from MPX-Bus	4B6
CLG1	Control Line Gate - Gates Private Control Lines	1C2
CLUS0	Clear Load/Unload Sequencer - Clears Sequencer	3S2
CMD0	Command Control Line from MPX-Bus	4B8
CMG1	Command Gated by AD1	2S7

MNEMONIC	MEANING	SCHEMATIC LOCATION
COO	Carry Out of the AAR - Prevents Memory Wrap-around	5A1
D000:150	Data Lines from MPX-Bus	Sheets 1 and 2
DA0	Data Available Control Line from MPX-Bus	4B7
DB001:151	Outputs of Data Buffer	Sheet 6
DLG0	Data Line Gate - Gates Data Lines and Private Data Lines	Sheet 1
DR0	Data Request Control Line from MPX-Bus	4B7
DRG0	Data Request Gated by AD1	2L5
DX1	Data Transfer flip-flop	3F8
EBS1	End of Busy Set - Signals the start of an ESELCH transfer	3J4
EDX1	End of Data Transfer - Signals the end of a device transfer	3J8
EMX1	End of Memory Transfer - Signals the end of a memory transfer	4R7
EN0	Enable from Memory Bus	4H2
ENG1	Engage - Gates either PDS0 or PDR0	3D8
ENMDR1	Enable Memory Data Register Read - Gates contents of MDR to MD000:150	4R6
ENMS1	Enable Memory Strobe - Gates contents of MS000:150 to MDR	4R4
HW0	Halfword Control Line from MPX-Bus	1D2
INH0	Inhibit from Memory Bus	4H5
LARH0	Load Address Register High - Loads AAR and AR, Bits 00:07	2R2

MNEMONIC	MEANING	SCHEMATIC LOCATION
LARL0	Load Address Register Low - Loads AAR and AR, Bits 08:15	2R2
LDBl	Load Data Buffer - Load contents of MDR to DB	3S2
LDRH0	Load Data Register High - Loads MDR Bits 00:07	3F8
LDRL0	Load Data Register Low - Loads MDR Bits 08:15	3H9
LFRH0	Load Final Address Register High -	2S3
LFRL0	Load Final Address Register Low - Loads FAR Bits 08:15	2S3
MA000:140	Memory Address Lines to Memory Bus	Sheet 5
MCHl	Match - Indicates a match between AAR and FAR	5J6
MD000:150	Memory Data Lines to Memory Bus	Sheet 6
MS000:150	Memory Strobed Data Lines from Memory Bus	Sheet 6
MSC0	Multiplexor ESELCH Control flip-flop	3F4
PADRS0	Private Address Control Line to ESELCH Bus	4F8
PATN0	Private Attention from ESELCH Bus	4Bl
PCL070	Private Control Line 7 to ESELCH Bus	4R6
PCMD0	Private Command Control Line to ESELCH Bus	4F8
PD000:150	Private Data Lines - ESELCH Bus	Sheet 1 Sheet 2
PDA0	Private Data Available Control Line from ESELCH Bus	3H5
PHW0	Private Halfword Control Line from ESELCH Bus	1Al

MNEMONIC	MEANING	SCHEMATIC LOCATION
PSR0	Private Status Request Control Line to ESELCH Bus	3H6
PSYN0	Private Sync from ESELCH Bus	4B5
PTACK0	Private Transmit Acknowledge to ESELCH Bus	4F2
RACK0	Receive Acknowledge from MPX-Bus	4B5
RBA0	Reset Buffer Active - Resets Buffer Active flip-flop	3M2
REQ0	Request - Request for memory cycle to Memory Bus	4R5
SCLR0	System Clear - Initialize Signal	4H4
SGAD1	Set Gate - Sets Address flip-flop	2L8
SR0	Status Request control line from MPX-Bus	4B6
SREQ0	Set Request - Initiates a request for memory	3S4
SSX0	Set Status Transfer - Sets the Status Request flip-flop	3S5
SX1	Status Transfer - Status Request flip-flop	3F6
SYN0	Sync to MPX-Bus	2S5
TAAR0	Toggle Auxiliary Address Register - Increments AAR	3M1
TAC0	Transmit Accept - To lower priority DMAs	4R1
TACK0	Transmit Acknowledge - To lower priority devices on MPX-Bus	4F3
TAR0	Toggle Address Register - Increments AR	4S7

MNEMONIC	MEANING	SCHEMATIC LOCATION
UAARH0	Unload Auxiliary Address Register High - Unloads AAR Bits 00:07	2R4
UAARL0	Unload Auxiliary Address Register Low - Unloads AAR Bits 08:15	2R4
WRT0A	Write to Memory Bus, when selected	4R3
WT1	Write flip-flop	3F5
XMA140 XMA150	Extended Memory Address Lines to Select the Applicable 64KB Memory Segment	2S8

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INTERDATA®

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	

RELEASED FOR PRODUCTION
MFG. ENG. DATE 5/27

R69 100 C58 470PF

226-1 PHWO — R28 180 P5 — 54 19-036 HP — 123 19-015 HG

P5 — R34 470 — 79 19-021 P — 03 HWO > 226-0

3F4,4A2,F2 MSCO — 85 19-036 HP — 06 CLG1 > 2C9,4B3

2J7 ADI — 85 19-036 HP — R48 1K — P5

PHWI > 2A9,3G9

3A2 SXI — 30 19-036 HP — 08 DLGO > N3,2E9

3A2 DXO — 10

2J5,3A6,M2 BSYO 02 — 64 19-021 P — 03 R42 1K — P5

B9 ATSYNO 04 — 42 19-016 HG — 06 ENDLI — 96 19-015 HG — 08

A2 MSCO 05 — F7

6A2 PHWOA — 78 19-003 G — 11

H9 AARI5I — 13

PHWI — 109 19-004 G — 08

2A9,3F3,F6 BSYI — 122 19-016 HG — 11 — 31 19-016 HG — 03

3F9 4R2 WTI — 12 — 13

3A9 AARI5O — 122 19-016 HG — 08 — 05 — 78 19-003 G — 06

2S6,F7 SRGI — 12 — 13 — 89 19-003 G — 11

4A4 ACKI — 09 — 89 19-003 G — 08

4F1 EACK1 — 10

C3 BSYO — 05 — 89 19-003 G — 06

2J6,4D6 SRI — 04

2J5,4D7 DRI — 01 — 02 — 89 19-003 G — 03

10 — 54 19-036 HP — 08 DLG1 > A3

09 — R30 1K — P5

R2 DLG1

K3 D081 — 136 19-036 HP — 03 — 135 19-016 HG — 03 — 134 19-015 HG — 02 DA08OA — 2 — A AG081 — H3

115-0 D080

K4 D091 — 136 19-036 HP — 06 — 135 19-016 HG — 06 — 134 19-015 HG — 04 DA09OA — 4 — B AG091 — H4

215-0 D090

K5 D101 — 136 19-036 HP — 08 — 135 19-016 HG — 08 — 134 19-015 HG — 06 DA10OA — 6 — C AG101 — H5

116-0 D100

K6 D111 — 136 19-036 HP — 11 — 135 19-016 HG — 11 — 134 19-015 HG — 08 DA11OA — 8 — D AG111 — H6

216-0 D110

K6 D121 — 113 19-036 HP — 03 — 124 19-016 HG — 03 — 134 19-015 HG — 10 DA12OA — 10 — E AG121 — H6 — DI4

117-0 D120

K7 D131 — 113 19-036 HP — 06 — 124 19-016 HG — 06 — 134 19-015 HG — 12 DA13OA — 12 — F AG131 — H7 — DI5

217-0 D130

K8 D141 — 113 19-036 HP — 08 — 124 19-016 HG — 08 — 123 19-015 HG — 12 DA14OA — 14 — G AG141 — H8 — DI7

118-0 D140

K9 D151 — 113 19-036 HP — 11 — 124 19-016 HG — 11 — 123 19-015 HG — 10 DA15OA — 16 — H AG151 — H9 — DI6

218-0 D150

2M7,4G4,F3,F2 ATSYNO — 2M9,5A3,K9 DA15I

2M7,5A3,K8 DA14I

3A4,5A1,K6 DA11I

3A5,5A1,K5 DA10I

3A3,5A3,K6 DA12I

5A3,K7 DA13I

5A1,K4 DA09I

5A1,K3 DA08I

NOTE 1

NOTE 2

133 19-001 G — 06 SGADO > 2J8

2J8,4F9 ADRS1A > DI8

DATA LINES 08-15

6A1,S3 PD08I — 5F1 AAR00I — 5F5 AAR08I — E4 AG08I — 06 — 07 DO8I > A3

6A2,S4 PD09I — 5F1 AAR01I — 5F5 AAR09I — E4 AG09I — 09 DO9I > A4

6A3,S5 PD10I — 5F2 AAR02I — 5F6 AAR10I — E5 AG10I — 07 DI0I > A5

6A4,S6 PD11I — 5F2 AAR03I — 5F6 AAR11I — E6 AG11I — 09 DI1I > A5

6A5,S6 PD12I — 5F3 AAR04I — E6 AG12I — 07 DI2I > AG

6A6,S7 PD13I — 5F3 AAR05I — 5F7 AAR13I — E7 AG13I — 09 DI3I > A7

6A7,S8 PD14I — 5F4 AAR06I — 5F8 AAR14I — E8 AG14I — 07 DI4I > A7

6A8,S9 PD15I — 5F4 AAR07I — 3A8,5F8,H2 AAR15I — E8 AG15I — 09 DI5I > A8

DATA INPUTS OUTPUT 132 STROBE 1 SELECT A SELECT B STROBE 2

DATA INPUTS 2 OUTPUT 19-038

121 / 110 / 99 — A — 19-038

4 TO 1 MULTIPLEXOR

P5 R66 1K

2C2,6G2 DB0 01 — 6R2 DA0 01 — C4 — 06 — 46 19-038 — 07 — DB0I > 2C2,6G2

2C3,6G3 DB0 11 — 6R3 DA0 91 — C4 — 09 — DB0I > 2C3,6G3

2C4,6G4 DB0 21 — 6R4 DA1 01 — C5 — 07 — 45 19-038 — DB0I > 2C4,6G4

2C5,6G5 DB0 31 — 6R5 DA1 11 — C6 — 09 — DB0I > 2C5,6G5

2C6,6G6 DB0 41 — 6R6 DA1 21 — C6 — 07 — 35 19-038 — DB0I > 2C6,6G6

2C6,6G7 DB0 51 — 6R7 DA1 31 — C7 — 09 — DB0I > 2C6,6G7

2C7,6G8 DB0 61 — 6R8 DA1 41 — C8 — 07 — 34 19-038 — DB0I > 2C7,6G8

2C8,6G9 DB0 71 — 6R9 DA1 51 — C9 — 09 — DB0I > 2C8,6G9

4 TO 1 MULTIPLEXOR

DLGO E2

48 19-036 HP — 03 — 47 19-015 HG — 02 PD08I > H3

P5 R17 330 — PD08O > 115-1

48 19-036 HP — 06 — 47 19-015 HG — 04 PD09I > H4

P5 R11 330 — PD09O > 215-1

48 19-036 HP — 08 — 36 19-015 HG — 12 PD10I > H4

P5 R15 330 — PD10O > 116-1

48 19-036 HP — 11 — 36 19-015 HG — 02 PD11I > H5

P5 R12 330 — PD11O > 216-1

37 19-036 HP — 03 — 36 19-015 HG — 06 PD12I > H6

P5 R13 330 — PD12O > 117-1

37 19-036 HP — 06 — 36 19-015 HG — 04 PD13I > H7

P5 R16 330 — PD13O > 217-1

37 19-036 HP — 08 — 36 19-015 HG — 10 PD14I > H8

P5 R5 330 — PD14O > 118-1

37 19-036 HP — 11 — 36 19-015 HG — 08 PD15I > H8

P5 R14 330 — PD15O > 218-1

PRIVATE DATA LINES 08-15

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NOTES 1. PREFERRED ADDRESS X'F0'
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-661.

SHEET INDEX	SHEET	1a	1	2	3	4	5	6
	REV NO.	0	0	0	0	0	0	0

REVISION LEVEL OF SHEET 1 IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

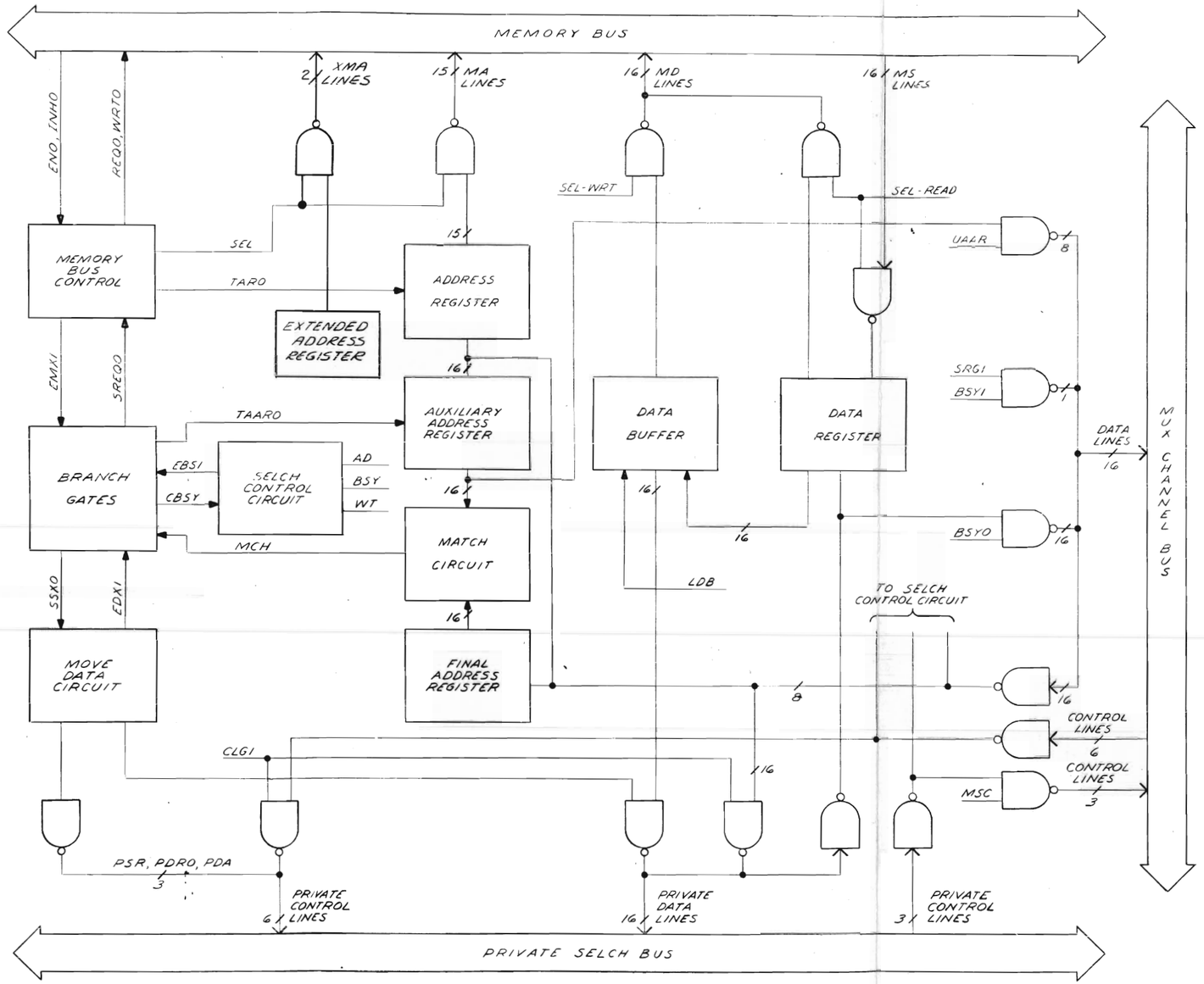
NAME	TITLE	DATE
G NELSON	DRAFT	5-27-77
B LIMPERT	CHK	7-9-77
G. HOWE	ENGR	7-7-77
R.A. WARNER		9-9-77
L FAJKANH	DIR ENG	9-9-77

TITLE: 16 BIT EXTENDED SELECTOR CHANNEL

TASK NO. 03882 — SHEET OF 1-6

DWG NO. 35-661 — DOB

RUNNING 49-231 15043



BACK PANEL PIN INDEX

MNEM	LOC.	MNEM.	LOC
ACTO	4H1	MD130	GR6
ADRSO	4B8	MD140	GR7
ATNO	4F1	MD150	GR8
CLO7O	4B6	MS000	GA1
CMDO	4B8	MS010	GA2
DO00	2A1	MS020	GA3
DO10	2A2	MS030	GA4
DO20	2A3	MS040	GA5
DO30	2A4	MS050	GA6
DO40	2A5	MS060	GA7
DO50	2A6	MS070	GA8
DO60	2A7	MS080	GH1
DO70	2A8	MS090	GH2
DO80	1A3	MS100	GH3
DO90	1A4	MS110	GH4
DO100	1A5	MS120	GH5
DO110	1A6	MS130	GH6
DO120	1A6	MS140	GH7
DO130	1A7	MS150	GH8
DO140	1A8	PADRSO	4F3
DO150	1A8	PATNO	4B1
DAO	4B2	PCLO7O	4F6
DRO	4B7	PCMDO	4F8
ENO	4H1	PDO00	1F1
HWO	1D1	PDO10	2F2
INHO	4H5	PDO20	2F3
MAO00	5R1	PDO30	2F4
MAO10	5R1	PDO40	2F5
MAO20	5R2	PDO50	2F6
MAO30	5R2	PDO60	2F7
MAO40	5R3	PDO70	2F8
MAO50	5R3	PDO80	1R4
MAO60	5R4	PDO90	1H4
MAO70	5R4	PDO100	1R5
MAO80	5R5	PDO110	1R6
MAO90	5R6	PDO120	1R7
MAO100	5R6	PDO130	1R7
MAO110	5R7	PDO140	1R8
MAO120	5R7	PDO150	1R9
MAO130	5R8	PDAO	4F2
MAO140	5R8	PDRO	4F8
MDO00	6G1	PHWO	1A1
MDO10	6G2	PSRO	4F6
MDO20	6G3	PSYNO	4B5
MDO30	6G4	PTACKO	4F2
MDO40	6G5	RACKO	4B3
MDO50	6G6	REQO	4R5
MDO60	6G7	SCLRO	4H4
MDO70	6G8	SRO	4B6
MDO80	6R1	SYNO	4F5
MDO90	6R2	TACKO	4H3
MDO100	6R3	TACO	4R1
MDO110	6R4	WRTOA	4R3
MDO120	6R5	XMAI30	25B
		XMAI40	25B

BACK PANEL MAP

ROW 1	ROW 2	TERM NO.	CONN
P5	GND	41	1
GND	GND	40	
		39	
		38	
MD150		37	
MD130	MD140	36	
MD110	MD120	35	
MD090	MD100	34	
MD070	MD080	33	
MD050	MD060	32	
MD030	MD040	31	
MD010	MD020	30	
	MD000	29	
		28	
		27	
SCLRO	PHWO	26	
		25	
		24	
PSYNO	PATNO	23	
	PTACKO	22	
PCLO7O	PDAO	21	
PDRO	PCMDO	20	
PSRO	PADRSO	19	
PDI40	PDI50	18	
PDI20	PDI30	17	
PDI00	PDI10	16	
PDO80	PDO90	15	
PDO60	PDO70	14	
PDO40	PDO50	13	
PDO20	PDO30	12	
PDO00	PDO10	11	
WRTOA	MS000	10	
MS010	MS020	09	
MS030	MS040	08	
MS050	MS060	07	
MS070	MS080	06	
MS090	MS100	05	
MS110	MS120	04	
MS130	MS140	03	
MS150		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	0
GND	GND	40	
	REQO	39	
	ENO	38	
ATCO	TACO	37	
		36	
		35	
		34	
MAI30	MAI40	33	
MAI10	MAI20	32	
MAO90	MAI00	31	
MAO70	MAO80	30	
MAO50	MAO60	29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
CLO7O	DAO	21	
DRO	CMDO	20	
SRO	ADRSO	19	
DI40	DI50	18	
DI20	DI30	17	
DI00	DI10	16	
DO80	DO90	15	
DO60	DO70	14	
DO40	DO50	13	
DO20	DO30	12	
DO00	DO10	11	
MAO30	MAO40	10	
MAO20		09	
XMAI50 *	XMAI40 *	08	
MAO10		07	
MAO00		06	
		05	
INHO		04	
		03	
		02	
GND	GND	01	
P5	GND	00	

TEST POINT INDEX

DESIG	MNEM	LOC.
A	ADI	2L6
B	WTI	3G5
C	SXI	3G6
D	MSCO	3G4
E	BSYO	3G3
F	ENMDWI	4S3
G	REQI	4S5
H	DXI	3G7
I	SELI	4L3
J	ENMSI	4S4
K	ENMDRI	4S6

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION

16BITESELCH	35-661

* CONNECT ONLY WHEN INSTALLED ON AN 8/16 E PROCESSOR

REV	0	0	0	0	0	0	0
SHEET NO	1A	1	2	3	4	5	6

NOTES

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NAME	TITLE	DATE
G. MELTON	DRAFT	5-16-77
W. LIMPERT	CHK	7/11/77
G. JUNGE	ENGR	
R.A. BARNER	Q.C.	
N. LEMUNDE	MGR. ENG	

TITLE: 16 BIT EXTENDED SELECTOR CHANNEL

TASK NO. 03882 | DWG NO. 35-661 | DOB | SHEET OF 1A-6

BRUNING 44231 15043

INTERDATA®

GOR1

15 DR1

DATA LINES 00-07

PRIVATE DATA LINES 00-07

LOAD/UNLOAD SEQUENCER

ADDRESS FF

19-032 I/O 10 DECODER

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-661.
2. WHEN THE 16 BIT EXTENDED SELCH IS INSTALLED ON AN 8/16 PROCESSOR CONNECT "W TO X" AND "Y TO Z".

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NAME	TITLE	DATE
G. MELTON	DRAFT	5-7-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: SELECTOR CHANNEL

TASK NO. 03883 | DWG NO. 35-661 D08 | SHEET OF 2-6

INTERDATA®

CIRCUIT NOTES

MAP FOR EDX (END OF DATA XFER)

	WTO	WTI	
MCHO	000 SSX	100 SSX	(EVEN) AAR150
	001 RBA	101 SREQ, SSX, LDB	(ODD) AAR151
MCHI	011 CBSY	111 SREQ, LDB	
	010 CBSY	110 SREQ, LDB	(EVEN) AAR150

MAP FOR EMX (END MEM. XFER)

	WTO	WTI
MCHO	SREQ, SSX, LDB	RBA
MCHI	SREQ, SSX, LDB	RBA

MAP FOR EBS (END BSY SET)

WTO	WTI
SREQ	SSX

BUFFER ACTIVE FF

BUSY FF

MUX/SELCH FF

WRITE FF

STATUS REQ FF

DATA XFER FF

ONE SHOT

1 OF 10 DECODER

BRANCH GATES

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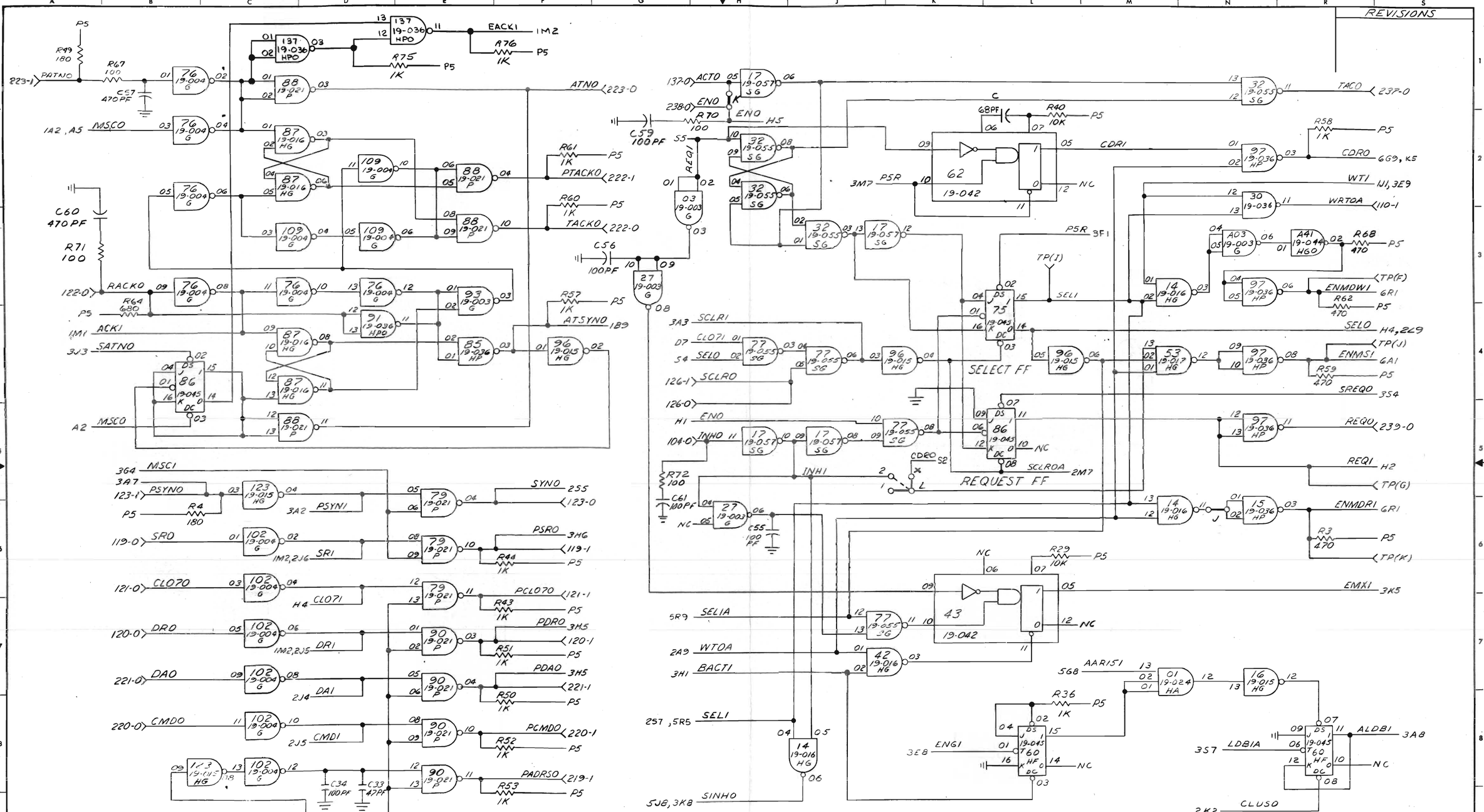
NAME	TITLE	DATE
G. MELTON	DRAFT	5-16-77
	CHK	
	ENGR	
	DIR ENG	

TITLE: 16 BIT EXTENDED SELECTOR CHANNEL

TASK NO. 03882
DWG NO. 35-661 D08
SHEET 3 OF 6

INTERDATA®

REVISIONS



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NAME	TITLE	DATE
G. MELTON	DRAFT	5-16-77
	CHK	
	ENGR	
	DIR ENG	

TITLE: 16 BIT EXTENDED SELECTOR CHANNEL

TASK NO. 03882 | DWG NO. 35-661 | DOB | SHEET OF 4-6

BRUNING 44 231 15043

INTERDATA®

IC4, J5 DA081
IC4, J5 DA091
IC5, J5 DA101
IC6, J7 DA111
3E2 COO

115 19-035: D, C, B, A, CARRY IN, BORROW OUT, CLEAR, LOAD, CNT DWN, CNT

253 LFRH1

AAR001 1H3 — 104 19-029 XOR
AAR011 1H4 — 104 19-029 XOR
AAR021 1H5 — 104 19-029 XOR
AAR031 1H5 — 104 19-029 XOR
AAR041 1H6 — 105 19-029 XOR
AAR051 1H7 — 105 19-029 XOR
AAR061 1H8 — 105 19-029 XOR
AAR071 1H9 — 105 19-029 XOR
AAR081 1H3 — 106 19-029 XOR
AAR021 1H4 — 106 19-029 XOR
AAR101 1H5 — 106 19-029 XOR
AAR111 1H6 — 106 19-029 XOR
AAR121 1F6 — 107 19-029 XOR
AAR131 1H7 — 107 19-029 XOR
AAR141 1H8 — 107 19-029 XOR
AAR151 1H3, 3A8, 4M7 — 107 19-029 XOR

T 126/127/128/129 19-027 D: NC

108 19-001 G → 109 19-004 G → 16 19-015 H6 → MCH0 3A9
108 19-001 G → 109 19-004 G → MCH1 3J4

116 19-035: IC6, J7 DA121; IC7, J7 DA131; IC8, J8 DA141; IC9, K1 DA151; 2R2, K2 LARH0
117 19-035: 253 LFRL1
118 19-035: L8 P5R; 2R2, J9 LARL0; P5; 3N1 TAARO; R63 1K

D4 D6 D7 D5 D8 D10 D11 D9

AUXILIARY ADDRESS REGISTER — FINAL ADDRESS REGISTER — MATCH CIRCUIT

A1 DA151
A4 LARH0

131 19-070 CAR 4 BIT COUNTER: CLK, ENP, ENT, LD
130 19-070
120 19-070
119 19-070

A1 DA081
A1 DA091
A1 DA101
A1 DA111
A3 DA121
A3 DA131
A3 DA141
A3 DAG0
2M4 93A 19-024 HA
4H8 SINH0
B8 P5R
AB LARL0
3G4 MSC0

125 19-036 HPO → MA000 106-0; MA010 107-0; MA020 109-0; MA030 110-0
103 19-036 HPO → MA040 212-0; MA050 129-0; MA060 229-0; MA070 130-0
92 19-036 HPO → MA080 230-0; MA090 131-0; MA100 231-0; MA110 132-0
91 19-036 HPO → MA120 232-0; MA130 133-0; MA140 233-0

SEL1 4G8
SELIA 4G1

ADDRESS REGISTER

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NAME	TITLE	DATE
G. MELTON	DRAFT	5-16-77
	CHK	
	ENGR	
	DIR ENG	

TITLE: 16 BIT EXTENDED SELECTOR CHANNEL
DATA 86 26
SHEET 5 - 6
35-661

BRUNING 44 231 15043

INTERDATA®

DATA REG HIGH

DATA BUFFER

DATA REG LOW

DATA BUFFER

ENMS1

MS000 210-1

PD081 1H3, N2

PHWOA 1H2

PDR000 2H1

MS010 109-1

PD091 1H4, H3

PDR010 2H2

MS020 209-1

PD101 1H4, H4

PDR020 2H3

MS030 108-1

PD111 1H5, H5

PDR030 2H4

MS040 208-1

PD121 1H6, H6

PDR040 2H5

MS050 107-1

PD131 1H7, H7

PDR050 2H6

MS060 207-1

PD141 1H7, H8

PDR060 2H7

MS070 106-1

PD151 1H8, H9

PDR070 2H8

LDAH0 3G8

LDAH1 3G9

R7 470Ω P5

MD000 229-1

DB001 1K3

MD010 230-1

DB011 1K4

MD020 230-1

DB021 1K5

MD030 131-1

DB031 1K5

MD040 231-1

DB041 1K6

MD050 132-1

DB051 1K7

MD060 232-1

DB061 1K8

MD070 133-1

DB071 1K9

LDB1 R9,3E7

CDR0 R9,4R2

ENMA S1 A1

MS080 206-1

PD081 A1

MS090 105-1

PD091 A2

MS100 205-1

PD101 A3

MS110 104-1

PD111 A4

MS120 204-1

PD121 A5

PDR120 3A1

MS130 103-1

PD131 A6

PDR130 3A1

MS140 203-1

PD141 A7

PDR140 3A1

MS150 102-1

PD151 A8

PDR150 3A1

LDRL0 3J9

R35 470Ω P5

ENMDR1 4R6

ENMDN1 4R3

MD080 233-1

DB081 1K3

MD090 234-1

DB091 1K4

MD100 234-1

DB101 1K5

MD110 135-1

DB111 1K6

MD120 235-1

DB121 1K6

MD130 136-1

DB131 1K7

MD140 236-1

DB141 1K8

MD150 137-1

DB151 1K9

LDB1 69

CDR0 R9

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NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-661-

NAME	TITLE	DATE
G. MELTON	DRAFT	5 NOV 74
	CHK	
	ENGR	
	DIR ENG	

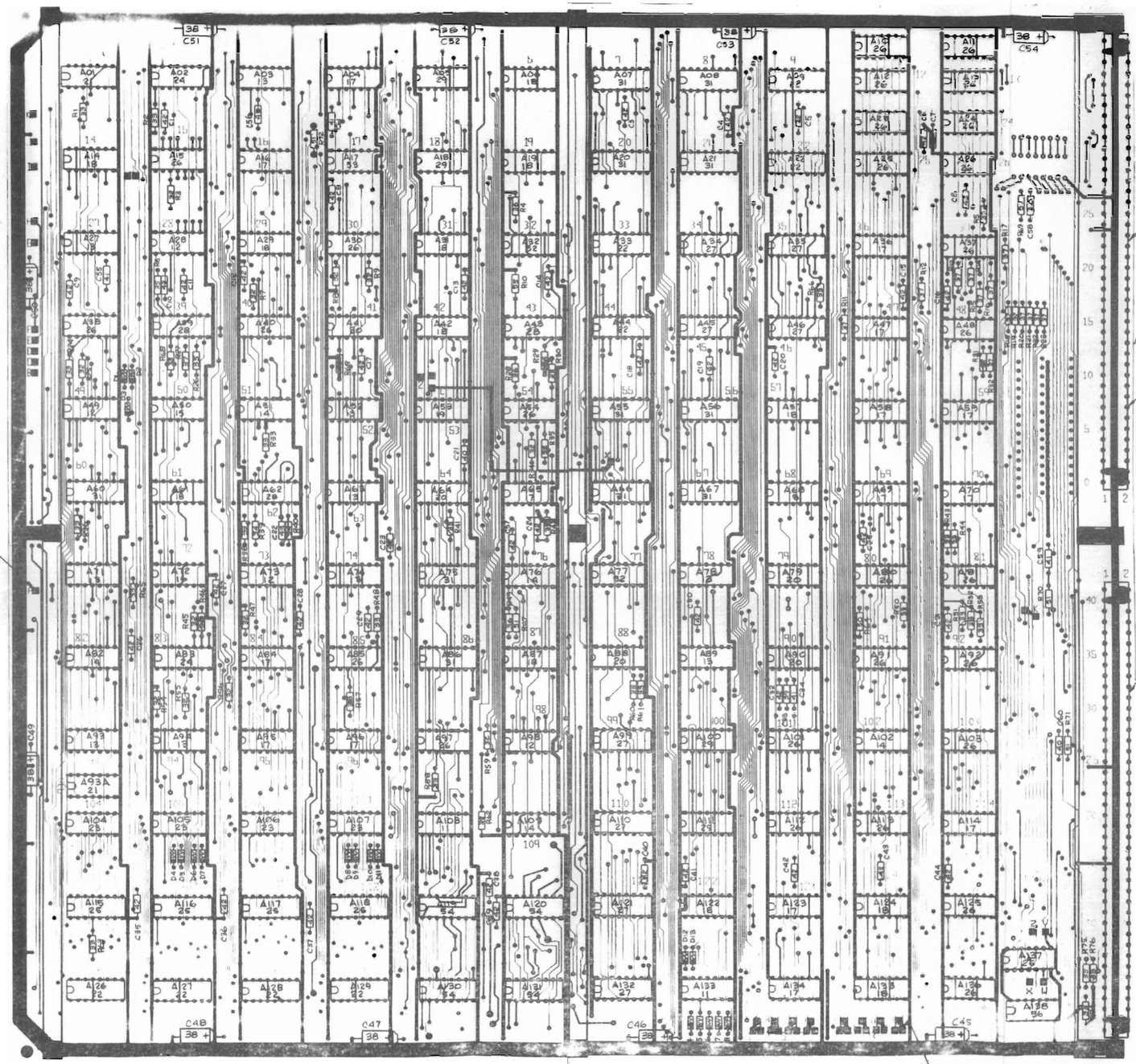
TITLE 16 BIT EXTENDED SELECTOR CHANNEL

TASK 03882 NO 85-661 DOC

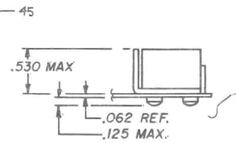
SHEET OF 6-6

BRUNING 44231 150-8

REVISIONS			
PRE PRODUCTION APPROVAL	REV	DATE	APPROVED
ZC 4137 WAS ITEM 68			
RELEASED FOR PRODUCTION			
MFG ENG		DATE	



NOTES:
1. FOR MOUNTING OF STANDARD HARDWARE SEE 16-642 DIA.
2. BEND LEADS CLOSEST TO THE EDGE OF BOARD INWARD PRIOR TO SOLDERING.
3. DIMENSIONS ARE IN INCHES.



PARTIAL VIEW A-A

COMPONENT	REF DESIGNATION
CAPACITOR	C1-21 & 23-60
RESISTOR	R1-36 38-76
DIODE	D1- D18
IC	A01--A138 & 93A

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NAME	TITLE	DATE
C. METTON	DRAFT	6-30-77
W. SUPERAT	CAE	7-7-77
S. JOYCE	ENG	7-7-77
R. BARKER	Q.C.	7-7-77
N. LENDINE	MGR.	7-8-77

TITLE: ASSEMBLY 16 BIT EXTENDED SELECTOR CHANNEL

3280-2

SIZE A | DWG | 1-1

SHEET 1

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