MANUAL UPDATE PACKAGE COVER SHEET

THIS PACKAGE UPDATES THE FOLLOWING PUBLICATIONS

PUB. NO.	OLD REV.	NEW REV.	TITLE
29-494	R00	R04	Power Conditioner Maintenance Manual

This revision includes changes reflecting:

ECNs 2914, 2955, 3092, 3122

SCNs

Briefly, the changes are as follows:

This package consists of:

This instruction sheet

New Title sheet

34-028R04D08 Sheet 1, 2

34-028R04D03 Sheet 1 of 1

35-615R06E03 Sheet 1 of 1

34-030D08 Sheets 1, 2, 3

34-030R01D03 Sheet 1 of 1

Preface - Sheet i/ii

Sheet iii/iv

Index - Sheet I-1/I-2

Publication Number 29-494R04

POWER CONDITIONER MAINTENANCE MANUAL

INTERDATA®
A UNIT OF
PERKIN-ELMER DATA SYSTEMS
2 Crescent Place, Oceanport, New Jersey 07757 • (201) 229-4040

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PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-494

TITLE Power Conditioner Maintenance Manual

REVISION R04 DATE May 1977

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
i/ii	R03	3/77						
iii/iv	R03	3/77						
1-1	R00	5/76						
1-2								
1-3/	R00	5/76						
1-4	R00	5/76						
2-1	R01	9/76						
2-2	R00	5/76						
2-3	R00	5/76						
2-4	R00	5/76						
I-1	R03	3/77						

PREFACE

This manual contains installation and maintenance information for the Power Conditioner. Applicable drawings are included at the back of the manual.

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REVISIONS			
PRE PRODUCTION APPROVAL	DEV	INIT	DATE
REVISED SHEETS 1, 2, & 3 FOR PREVIOUS REVISION SEE R00 MICROFILM IN FILE. AREA K9, 35-614 WAS R00 & 35-615 WAS R02			
	JRB	TV	030258	3-19-76	R01
REVISED SHEETS 1 & 2 AREA K9, 35-615 WAS R01 AREAS F1, B7 DIODES SHOWN DOTTED WERE NOT SPEC'D ADDED NOTE 3. AREA D5, C122 WAS 4.7/50V; AREA B5, C140 WAS 0.1/30V & WAS CONNECTED TO R140; AREA A6, ADDED R199; AREA F4, ADDED R200 & C142; AREA J6, CHARGER ON/OFF WAS WAS CONNECTED TO D109 CATH.			
	JRB	TV	030251M	3-30-76	R02
RELEASED FOR PRODUCTION END: [illegible] DATE: 4/3/76			
REVISED SHTS 1 & 2, ADDED THE FOLLOWING COMPONENTS: D122-D131, D133, C143 & C144, R102, R189, R201 & R202. C142 WAS SPEC'D AS 15uF. AREA F1: DELETED DIODES, AREA B5: DELETED C116 0.1uF, R140 33Ω. REVISED CIRCUITRY AREA E2, G6. AREA L9: 35-615 R08 WAS R06.			
	WS	2914	8-26-76	R03
AREA A1 & 1B & 2A ADDED COLORS TO WIRES CHANGED 2B3 WAS 2A3 & 2A3 WAS 2B6, CHANGED A WAS B & B WAS C. REVERSED POSITIONS OF F301 5A AND P/O S301. DELETED (FUSE) F302 5A. AREA D1, ADDED AC1 & AC2. ALSO CHANGED SHT 2.			
	JM	DV	3122	5-25-77	R04

GRN. BLK WHT. F301 5A P/O S301 P/O S301 24-069 L301 (BE) (BC) (AC1) (AC2) D301 23-023 R301 1.0 25W R302 1.0 25W P1 J1 2B3 2A3 2A6 P/O 11-186 C136 475 200V C137 475 200V R156 100K R155 100K R154 100K R153 100K C110 15 200V C111 15 200V 30-048 T102 D101 23-042 C143 .1 100V R189 10, 5W D102 23-042 L101 30-050 2uH C107 330 6.3V R102 5.0 10W E103 5.0 10W C108 16500 6V R104 21-075 .006 WHT WHT L102 30-023 40uH P5+L 100-2-113-2 200-2-212-2 P5 GND & LGND 114-2-127-2 213-2-227-2 YEL YEL C B A

P15 BIAS R145 2K Q115 20-023 P15 AUX 2K7 R144 100 1% Q113 R143 3.3K Q112 20-023 20-023 T101 30-049 C109 540 PF 1000V R196 .12, 5W 20-030 Q103 20-030 Q105 R109 450 N.I. 1uH MAX 5W WW R197 .12, 5W R134 33 D125 D126 D127 D128 D129 D130 23-034 R138 4.7K R139 4.7K R148 4.7K R147 4.7K Q117 Q118 20-027 20-023 Q114 Q116 20-027 R146 22 R137 33 D107 23-025 D105 23-025 R142 6.8K R195 10K

A103 19-191 A103 19-191 A103 19-192 CLK1 A103 19-192 CLK2 R150 17.2K 1% C117 330PF 2%

P15 BIAS R194 10K C135 .0039 C134 .0039 R193 5.1K Q132 20-013 2A4 P12 GND R149 6.8K Q131 C142 100 25V R200 100 1/2W D131, 23-034 D133 D122 23-022 23-034 Q129 20-013 Q128 20-013 R135 10K R133 10K R136 1% 1K, 1W C113 23-034 R165 1.5K Q124 20-013 D111 23-034 R124 160K R125 15K R126 100 C122 15 25V R180 6.8K C140 0.47 150V 140-2 C4 Q127 20-013 Q130 20-013 R184 6.8K R183 10K P12 GND 2R4 R174 47K R171 100K C123 2.2 20V R191 6.8K C128 150 PF R190 5.1K C129 0.1 30V R198 6R C141 0.1 30V R105 10K R192 1K 1% C144 15 µF D124 23-034 R201 150 R202 22 D123 C 23-028 C139 0.1, 30V R151 4.99K 1% R152 20K 1% Q119 20-038 R141 13.3 1% R199 1 1W

R104 19-094 NC 09 Vcc V2 10 VOUT 01 NC 08 NC 14 COMP 13 VREF 06 NON INV IN 05 INV IN 07 CUR LIM SENSE 04 CUR 03 02 11 12

P/O 30-051 T301 P1 10 11 12 1 5 6 7 D113 23-034 D114 23-034 SEE NOTE 3 D115 23-034 D116 23-034 D117 23-034 C124 100 50V C126 4.7 50V C127 4.7 50V R185 681 1% C125 0.47 150V R181 150K 1% R177 23.7K 1% R178 15K R173 100K R179 10K R186 1K 1% R182 357K 1% Q126 20-038 R176 2K 1% R175 68K R172 20K 1% Q125 20-013 D112 23-043F02 6.2V, 1% R168 10K Q123 20-023 P15AUX 2K7 R167 6.8K R169 68K Q122 20-013 R166 10K R170 68K R164 3K D109 23-034 D110 23-034 R162 10K R163 10K Q121 20-013 R161 47 D108 23-034 Q120 2.2 20V R160 820K R159 10K P15 BIAS C121 0.1 30V R158 3K R157 10K 20-013 Q120 R106 2K PFDTO (POWER FAIL) 135-2 PWR FAIL GND 235-2

M105 19-085 Vcc RESET OUTPUT TRIGGER DISCHARGE THRESHOLD CONT. VOL GND 08 04 03 02 07 06 05 01

P/O 11-186

A103 19-191 08 09 13 12 10 NC 11 NC

CHARGER ON/OFF → 3E7

COMPONENT NUMBERING	
101-299	HI VOLTAGE BOARD
301-399	CHASSIS
401-499	BATTERY OPTION BD

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-614 R01	BATTERY OPTION
35-615 R08	HI VOLTAGE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET	REV LEVEL	4	4	1
INDEX	SHT. NO.	1	2	3

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
:ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
:ALL CAPACITORS ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE PART OF 35-615.
3. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

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SCALE: ~ TOLERANCE .XXX ± .005 .XX ± .02 .X ± .03 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED

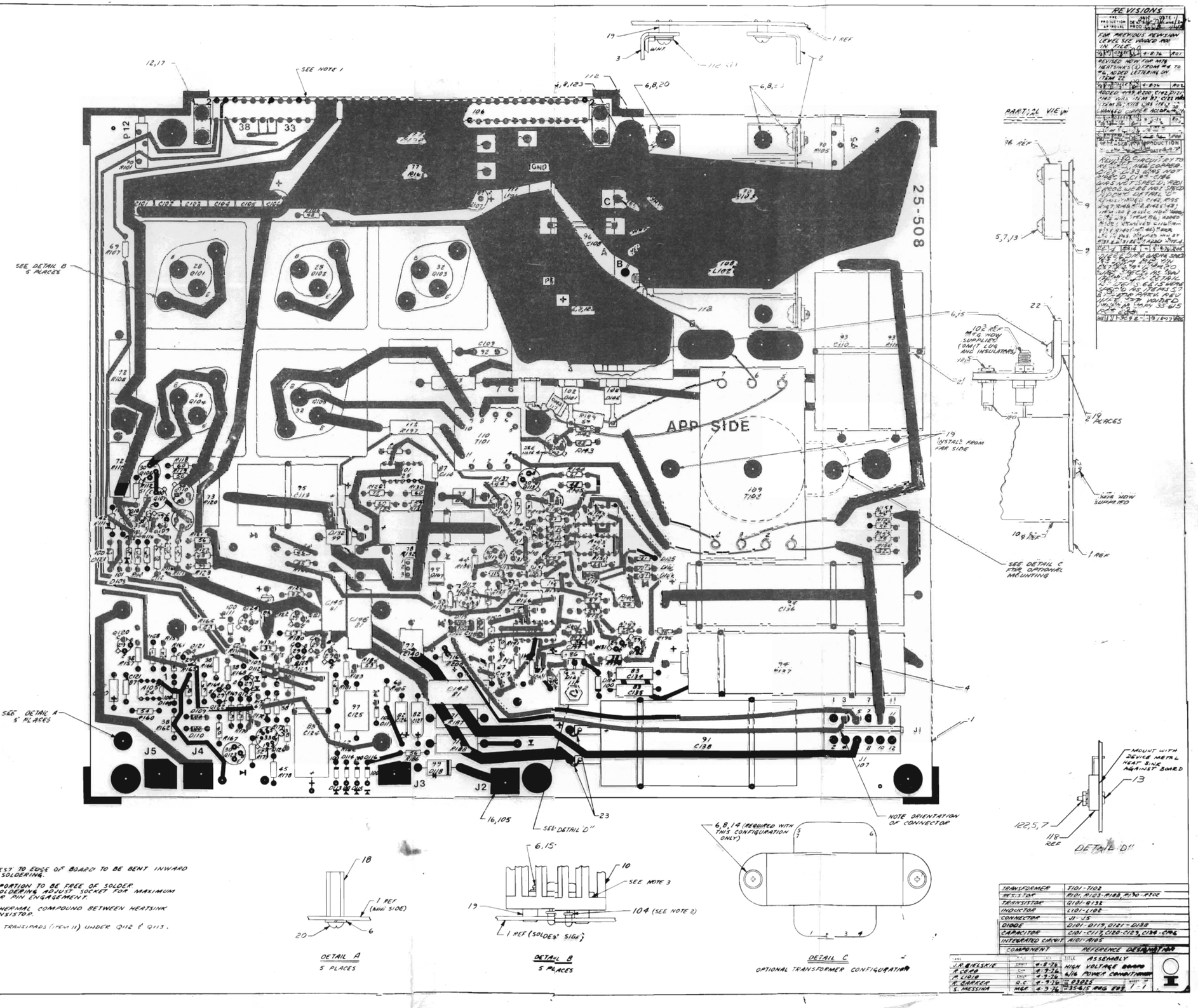
NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	11-10-75
H. MATTER	CHK	4-9-76
P. LIOIO	ENGR	4-9-76
J. JAMES	SYS TEST	4-9-76
S. MESSINA	MGR	4-9-76

TITLE FUNCTIONAL SCHEMATIC POWER CONDITIONER

TASK NO 03025 SHEET 1 OF 3

DWG NO. 34-028 R04 006

BRUNING 44-231 24538



REVISIONS

SYM	DESCRIPTION	DATE	APPROVED
	PRODUCTION RELEASE	4-8-76	
P01	REVISED PER MCR 4-8-76	4-8-76	
P02	REVISED PER MCR 4-8-76	4-8-76	
P03	REVISED PER MCR 4-8-76	4-8-76	

NOTES:

1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
2. INTERIOR PORTION TO BE FREE OF SOLDER BEFORE SOLDERING ADJUST SOCKET FOR MAXIMUM TRANSISTOR PIN ENGAGEMENT.
3. APPLY THERMAL COMPOUND BETWEEN HEATSINK AND TRANSISTOR.
4. EQUIP 3 TRANSIPADS (ITEM 11) UNDER Q112 & Q113.

TRANSFORMER	T101-T102
RESISTOR	R101, R103-R188, R190-R202
TRANSISTOR	Q101-Q132
INDUCTOR	L101-L102
CONNECTOR	J1-J5
DIODE	D101-D119, D121-D138
CAPACITOR	C101-C117, C120-C123, C134-C196
INTEGRATED CIRCUIT	A101-A105
COMPONENT	REFERENCE DESIGNATION

J.R.BIELSKIE	DRAFT	4-8-76
R.COEN	CHK	4-9-76
A.LEIB	ENGR	4-9-76
R.BARKER	Q.C.	4-9-76
S.MESSINA	MGR.	4-9-76

TITLE: ASSEMBLY HIGH VOLTAGE BOARD 4/16 POWER CONDITIONER

D-23022 REV. P3

23-515 ANG ASS'Y. SHEET 1 OF 1

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REVISIONS		
PRE PRODUCTION APPROVAL	DEV	INIT / DATE JMC 9-15-76

GREEN/YELLOW
BRN
F301 5A
P/O 5301
BLUE
24-069 L301
D301 23-023
P301 1.0 25W
P302 1.0 25W
P1
J1
2B3 A
2A3 B
2A6 D
P/O 11-200
P15 BIAS
C136 475 200V
C137 475 200V
R156 100K
R155 100K
R154 100K
R153 100K
C110 15 200V
C111 15 200V
30-048F01
T102
D101 23-042
D102 23-042
C143 .1, 100V
R189 10, 5W
C108 16500 6V
L101 30-050 3 uH
C107 330 6.3V
R103 5.0 10W
R102 5.0 10W
P5GND
P5+L
100-2-113-2
200-2-212-2
P5GND
E
GND
114-2-127-2
213-2-227-2
L102 40uH 30-023
R104 Z1-075 .006
WHT WHT
YEL YEL
C B
A
T101 30-049F01
C109 540 MF 100V
R196 .12, 5W
R197 .12, 5W
20-030 Q109
20-030 Q105
R109 450 N.I. 1 mN MAX 5W WW
P15 AUX 2K7
R145 2K
Q115 20-023
R144 100 1%
Q113 20-023
R143 3.5K
Q112 20-023
R134 33
R138 4.7K
R139 4.7K
R148 4.7K
R147 4.7K
Q117 20-023
Q118 20-027
Q114 20-023
Q116 20-027
R146 22
33
D107 23-025
D105 23-025
R142 6.8K
D125 23-036
D126 23-036
D127 23-036
D128 23-036
D129 23-036
D130 23-036
A103 19-191
A102 19-192
A101 19-192
R150 17.2K 1%
C117 330PF 2%
R195 10K
R135 10K
R133 10K
R136 1% 1K, 1W
P15 BIAS
R194 10K
C135 .0039
C134 .0039
R193 5.1K
Q132 20-013
P12 GND 2R4
R149 6.8K
Q131 20-013
D131 100 23-034 25V
R200 100 1/2 W
C142 .1
D119 23-034
Q119 20-038
A101 19-191 13.3 1%
R199 1 1W
P15 BIAS
C140 0.47 150V 140-E
C4
R124 160K
R125 15K
Q127 20-013
R165 1.5K
100
R126
Q124 20-013
D111 23-034
C122 15 25V
R188 68K
R189 10K
R180 68K
Q130 20-013
Q129 20-013
D133 23-022
D122 23-034
Q128 20-013
R174 47K
R171 100K
C123 2.2 20V
R191 6.8K
C138 150 MF
R190 5.1K
C129 0.1 30V
P12 GND 2R4
NC 09
NC 01
NC 08
NC 14
Vcc
V2
VOUT
VREF
COMP
A104 19-094
C141 0.1 30V
R198 68
R105 10K
R192 1K 1%
R201 150
R202 22
D124 23-034
C144 15 MF
D123 G 23-028
C139 0.1, 30V
R151 4.99K 1%
R152 20K 1%
CHARGER ON/OFF 3E7
P/O 30-051
T301
D113 23-034
D114 23-034
D115 23-034
D116 23-034
D117 23-034
SEE NOTE 3
C124 100 50V
C126 4.7 50V
C127 4.7 50V
R185 681 1%
C125 0.47 150V
R181 150K 1%
R177 23.7K 1%
R176 6.8K
R186 1K 1%
R182 3.57K 1%
R178 15K
R173 100K
R179 10K
Q126 20-038
R175 2K 1%
R172 20K 1%
Q125 20-013
D112 23-043F02 6.2V, 1%
R170 68K
R169 68K
R166 10K
Q123 20-023
R167 6.8K
R164 3K
Q122 20-013
P15 BIAS 2K7
D103 23-034
D110 23-034
R162 10K
R163 10K
Q121 20-013
R159 10K
R160 820K
R161 47
D108 23-034
C120 2.2 20V
A105 19-085
TRIGGER
DISCHARGE
THRESHOLD CONT. VOL.
Vcc
RESET
OUTPUT
GND
C121 0.1 30V
R158 3K
R157 10K
R106 2K
20-013 Q120
PFDTO (POWER FAIL) 135-2
PWR FAIL GND 235-2
P/O 11-200
A103 19-191
NC
NC

COMPONENT NUMBERING	
101-299	HI VOLTAGE BOARD
301-399	CHASSIS
401-499	BATTERY OPTION BD

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-614R01	BATTERY OPTION
35-615F01	HI VOLTAGE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET	REV. LEVEL			
INDEX	SHT. NO.	1	2	3

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
:ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
:ALL CAPACITORS ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE PART OF 35-615F01.
3. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

DRAWING 44-231 24536

SCALE – NONE

NAME	TITLE	DATE
J. CONWAY	DRAFT	7-8-76
R.F. CERO	CHK	9-9-76
E. CENTOFANTI	ENGR	
B. MULLER	SYS TEST	
S. MESSINA	MGR	

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TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

TASK NO. 03013
DWG NO. 34-030 D08
SHEET 1 – 3

INTERDATA
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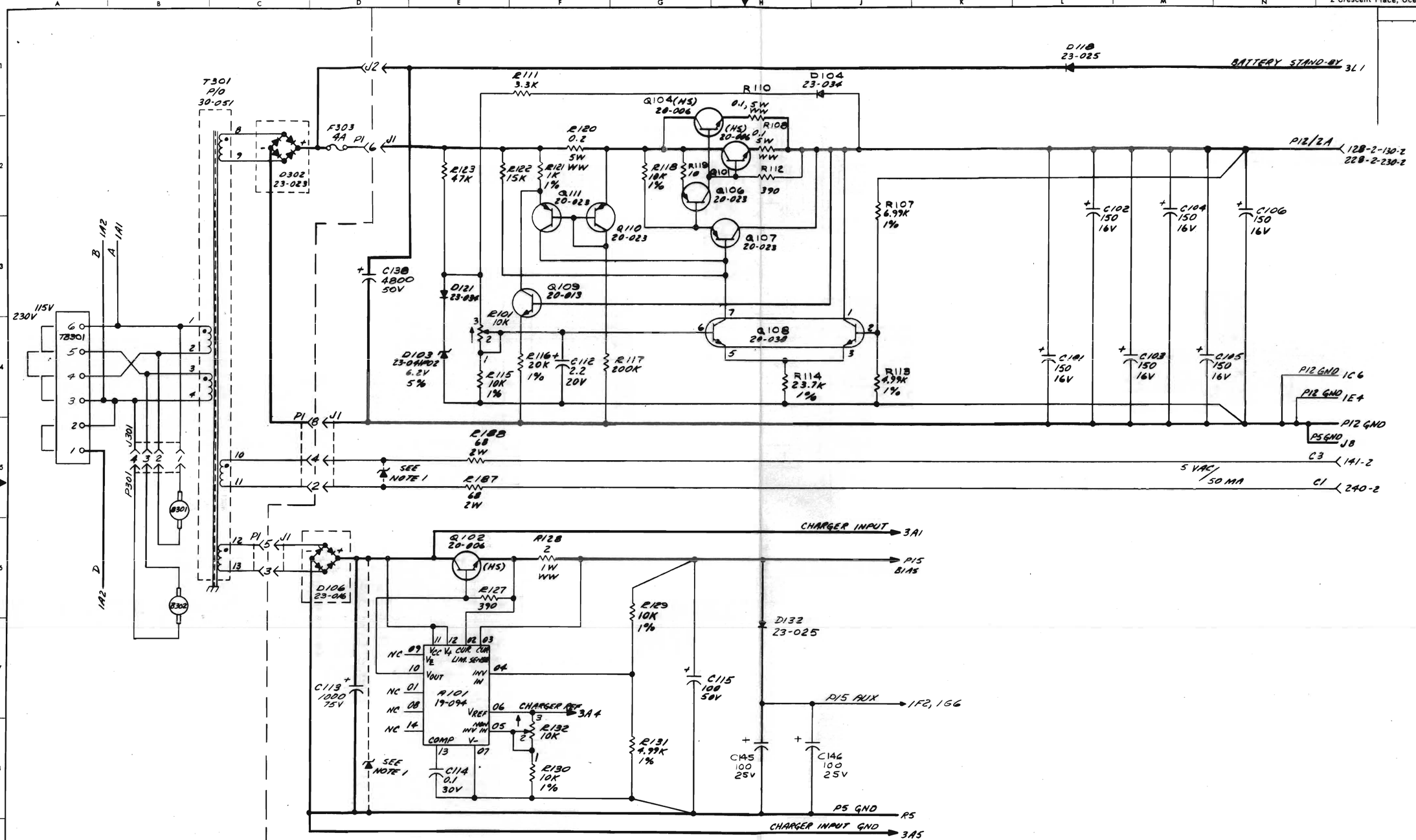
REVISIONS



NOTES:
1. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

SCALE – NONE	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .07, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	J. CONWAY	DRAFT	7-8-76
		CHK	
		ENGR	

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TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

TABS NO. 03013
DWG NO. 34-030 D08
SHEET 2 OF 3

BRUNING 44-231 24539

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REVISIONS

2J6 CHARGER INPUT
2F7 CHARGER REF
2J9 CHARGER INPUT GND
1K6 CHARGER ON/OFF

R403 1 1W 3% WW
R402 1K
C401 0.1 100V
R404 10K
R405 10
Q403 20-006 (MS)
R406 390
Q404 20-023
Q401 20-023
Q402 20-023
Q405 20-023
D401 23-025
R407 12.7K 1%
R401 15K
R408 100K
C402 0.1 30V
Q407 20-013
R411 390K
R413 100
R406 20-038
R415 10K
R409 100K
R410 100K
R412 100K
Q408 20-013
R414 33K
R416 1950 1%

BATTERY BOARD
35-614

HI VOLTAGE BOARD
P/O 35-615F01

BATTERY STAND-BY → 2R1
J3
138-2 TO BACK PANEL EXT BATT (+)
238-2
BAT+
18V
139-2 TO BACK PANEL EXT BATT (-)
239-2
BAT-
J5
J4
P/O 5301

CHASSIS ASSY
P/O 11-200

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SCALE – N

NAME	TITLE	DATE
J. CONWAY	DRAFT	7-8-76
	CHK	
	ENGR	

TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

DWG. no. 03013
DWG. no. 34-090

DRAWING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

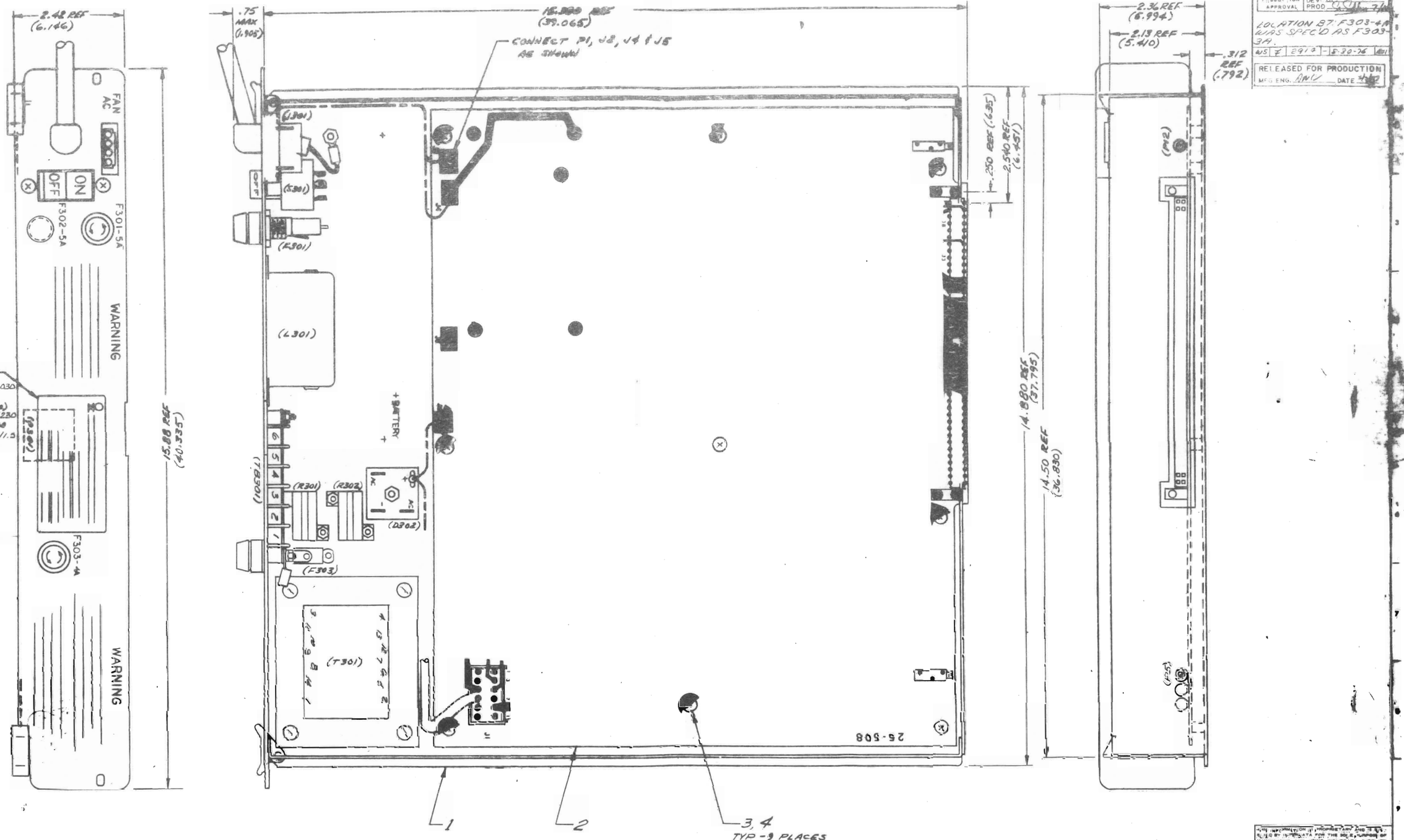
REVISIONS

PRE PRODUCTION APPROVAL	UNIT	DATE
	DEV.	12.7.76
	PROD.	

LOCATION ST. F303-4A WAS SPEC'D AS F303-3A.

W/S	Z	2913	-	5-20-76	ADD

RELEASED FOR PRODUCTION
MFG ENG. AMV DATE 4-6-77



NOTE: DESIGNATIONS IN PARENTHESES ARE FOR REFERENCE ONLY; DIMENSIONS IN PARENTHESES INDICATE METRIC EQUIVALENT IN CM.

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SCALE - 1-1

TOLERANCE: XXX ± .005, XX ± .02, X ± .06, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J. CONWAY	DRAFT	7-7-76
R.F. CERO	CHK	9-9-76
E. CENTOFANTI	ENGR	1-7-77
R.A. BARKER	QC	12-30-76
L. PEZZI	MGR	1-10-77

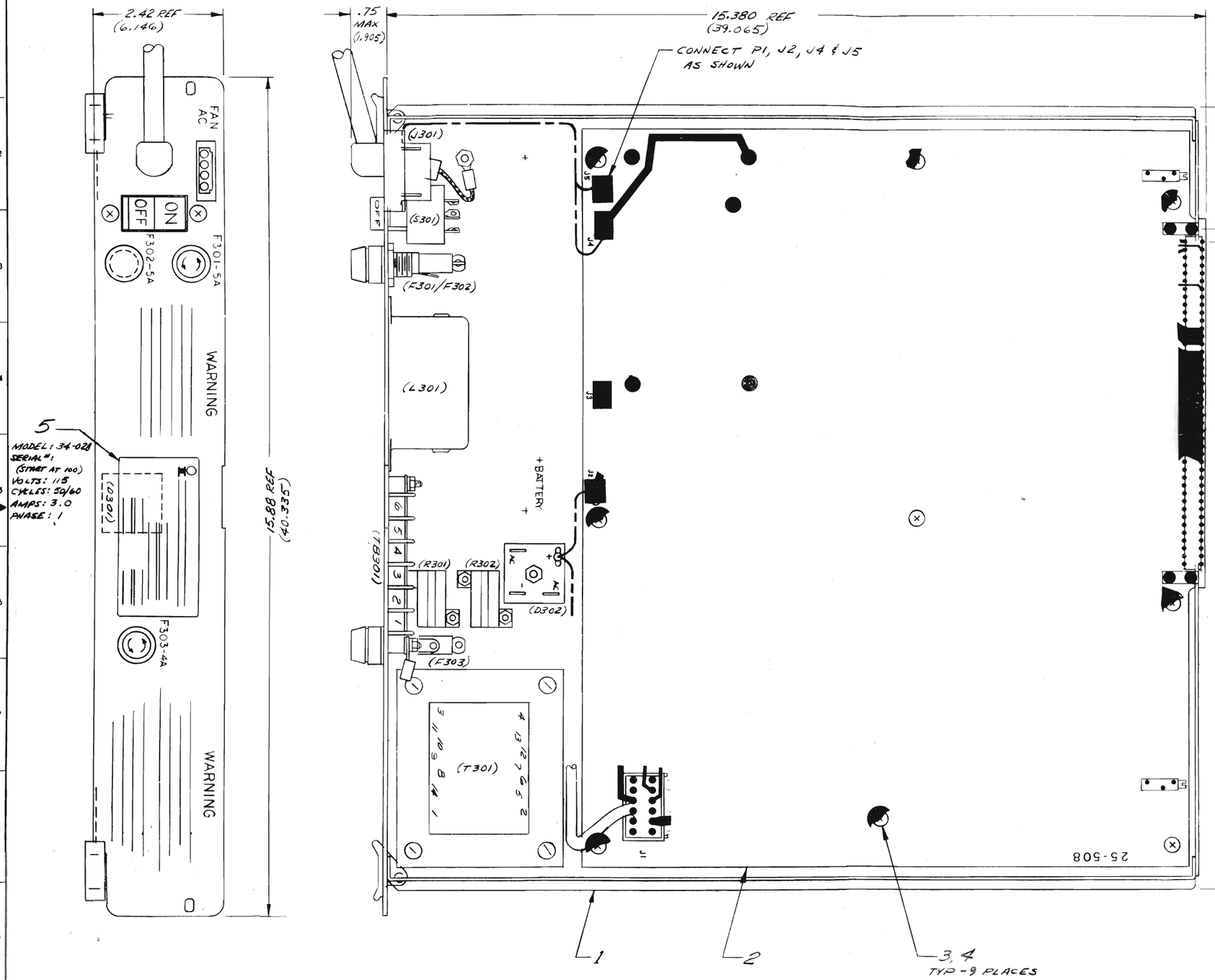
TITLE ASSEMBLY, SEMI-MEMORY POWER CONDITIONER (VDE)

SIZE 03015 — 34-030 R01D03 — 1 — 1

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

PRE PRODUCTION APPROVAL	DEV PROD			
REVISED DRAWING TO REFLECT CHANGES TO ITEM 1.				
2	JW	030276-E	3-18-76	002
RELEASED FOR PRODUCTION MFG ENG [signature] DATE 4.9.76				
LOCATION B6: F303-4A WAS SPEC'D AS F303-3A.				
1	7	29.14	8.26.76	R02
LOCATION N7. ITEMS, OUTPUT LABEL & NOTE 2 WERE NOT SPEC'D				
WS	12V	29.55	VI-29.76	R03
AREA A3 PLUG WAS FUSE HOLDER.				
M	07	3122	5.25.77	R04



NOTE: 1) DESIGNATIONS IN PARENTHESES ARE FOR REFERENCE ONLY; DIMENSIONS IN PARENTHESES INDICATE METRIC EQUIVALENT IN CM.

2) OUTPUT LABEL: MARK WITH THE FOLLOWING INFO.:
+5 VOLTS @ 25 AMPS
+12 VOLTS @ 2 AMPS

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	H. MATTER	CHK	4-9-76
	G. WELLY/LIDIO	ENGR	4-9-76
	R.A. BARKER	Q.C.	4-9-76
	P. ABITANTE	MGR	4-9-76

TITLE ASSEMBLY, SEMI-MEMORY POWER CONDITIONER

TASK NO. 08046 SHEET OF 1 — 1

DWG NO. 34-028 R04 D03

DRAWING 46-231 24538

MANUAL UPDATE PACKAGE COVER SHEET

THIS PACKAGE UPDATES THE FOLLOWING PUBLICATIONS

PUB. NO.	OLD REV.	NEW REV.	TITLE
29-494	R04	R07	Power Conditioner Maintenance Manual

This revision includes changes reflecting:

ECNs 3687, 3572, 3597

SCNs

Briefly, the changes are as follows:

This Package Consists Of:

This Instruction Sheet

New Title Sheet

Page Revision Status Sheet

Sheet iii/iv, 1-1, 1-2, 2-1, 2-2, 2-3, 2-4

Delete 34-028D08

Delete 34-028D03

35-615R07E03 Sheet 1 of 1

34-030R02D08 Sheets 1, 2, 3

34-030R02D03 Sheet 1, 2

Publication Number 29-494R07

POWER CONDITIONER

MAINTENANCE MANUAL

PERKIN-ELMER

Interdata Division
2 Crescent Place
Oceanport, N.J. 07757

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PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-494

TITLE Power Conditioner Maintenance Manual

REVISION R07 DATE June 1978

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
i/ii	R03	3/77						
iii/iv	R07	6/78						
1-1	R07	6/78						
1-2	R07	6/78						
1-3/ 1-4	R00	5/76						
2-1	R07	6/78						
2-2	R07	6/78						
2-3	R07	6/78						
2-4	R00	5/76						
I-1	R03	3/77						

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High Voltage PC Board Assembly, 35-615R07E03
Battery Option PC Board Assembly, 35-614R02C03
VDE Schematic, 34-030R02D08
VDE Assembly, 34-030R02D03

CHAPTER 1
POWER CONDITIONER INSTALLATION

1.1 INTRODUCTION

INTERDATA computer systems feature a highly modular structure allowing exact configurations to suit user needs. The Semi-Memory Power Conditioner (34-030) supports the 6/16 Processor with MOS Memory rather than Core Memory. In expansion systems where both MOS and Core Memories are used, the Semi-Memory Power Conditioner can be used in conjunction with older version power conditioners (34-017, 34-020, 34-026) used for Core Memories, to satisfy user requirements. The Semi-Memory Power Conditioner also features an option consisting of an internal Battery and Charger Board that can sustain the system's power requirement for a 1.5 hour period if the Power Conditioner source voltage drops below a specified level. Provision has also been made for the user to connect his own back-up power source through the Power Conditioner rear panel. This chapter provides the user with installation information for the 34-030 Power Conditioner installed in a standard INTERDATA cabinet.

1.2 POWER CONDITIONER MOUNTING

The Power Conditioner unit is placed in the upper three card slots of a standard INTERDATA System Chassis (refer to Figure 1-1) and is attached to the chassis with four screws (two in the front and two in the rear). The unit is properly installed in the chassis if the ac connector is mated with the FAN AC receptacle located at the left side of the Power Conditioner's front panel. Refer to the Semi-Memory Power Conditioner Assembly Drawing (34-030D03) for views of the front panel.

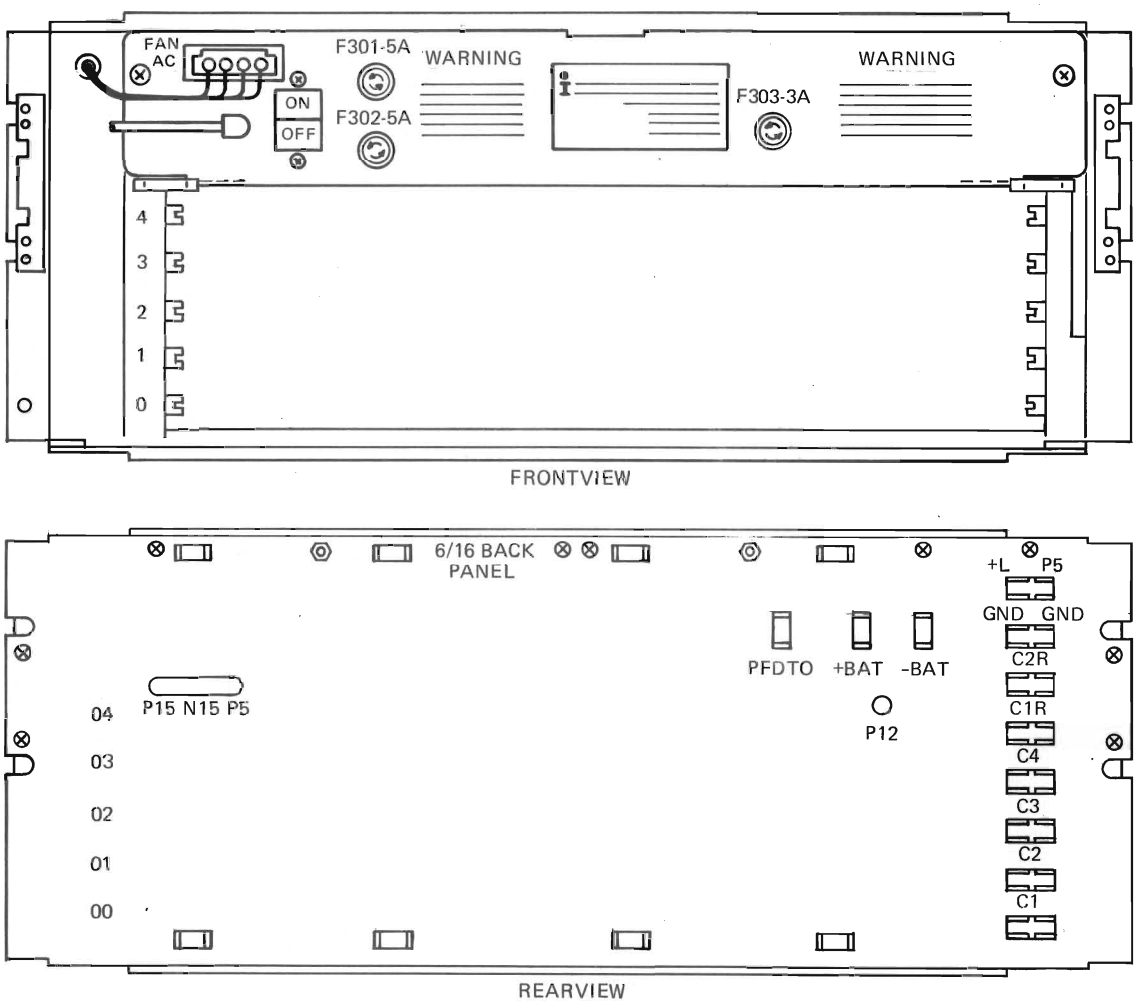


Figure 1-1. Views of Installed Power Conditioner Unit

1.3 BATTERY OPTION

This option consists of an 18 volt battery with a trickle charger mounted on a board for easy installation into the Power Conditioner unit. Five screws are provided for mounting the board and for establishing electrical contact. The charger is set for 21.0 volts (slightly above the battery voltage under load conditions) at the factory. A current limiting of 200 ma is characteristic of the battery charger. This board can be checked independently from the other portions of the Power Conditioner.

1.4 PRIMARY POWER

Primary power supplied to the Power Conditioner can be either 115 Vac or 230 Vac ±10%, 47 to 63 Hz, depending on the available power at the installation. The unit is strapped at the factory for either 115 or 230 volt operation. Only if 230 volt operation is specified by the user in his purchase order will the unit be strapped for 230 volt operation. The user can, however, convert the Power Conditioner from 115 to 230 volt operation by performing the following procedure:

1. Remove the unit from the chassis exposing terminal board TB301 (Refer to drawing 34-028D03 for the location of TB301.)

2. Verify that TB301 terminals are strapped for 115 Vac operation:

   1 to 2
   3 to 4
   5 to 6

3. Remove all straps from TB301.

4. For 230 volt operation, strap terminals 2 and 3 of TB301.

5. Place the unit back into the chassis.

6. Label the Power Conditioner "Connected for 230 Vac Operation."

7. Change the 5 Amp fuse to 3A.
   Change the 3 Amp fuse to 2A.

WARNING

PLACE THE ON/OFF SWITCH (S301) TO THE OFF POSITION PRIOR TO REMOVING THE UNIT FROM THE CHASSIS TO DISCONNECT THE INTERNAL BATTERY (OPTIONAL) AND TO REMOVE THE LINE VOLTAGE (EITHER 115 OR 230) AT TB301 AND AT THE PRIMARY SIDE OF TRANSFORMER T301 (PINS 1-4). FAILURE TO DISCONNECT THE INTERNAL BATTERY WITH THE ON/OFF SWITCH CAUSES THE BATTERY TO DRAIN. THIS IS ESPECIALLY IMPORTANT FOR TURNKEY CONSOLE OPERATION WHERE THE OPERATOR MAY TURN THE CONSOLE OFF, BUT LEAVE THE POWER CONDITIONER ON.

1.5 POWER CONDITIONER EXPANSION

If more than one 34-030 Power Conditioner units are used at an installation, the C4 contacts located at the rear panel, must be strapped together to insure proper power turn on. For expansion involving the use of 34-017, 34-020, or 34-026 units, strapping at the rear panel is accomplished differently. Refer to Figures 1-2 and 1-3 for strapping requirements.

CHAPTER 2
POWER CONDITIONER MAINTENANCE

2.1 INTRODUCTION

This chapter provides maintenance information for the INTERDATA Semi-Memory Power Conditioner (34-030). Included is a listing of general specifications, theory of operation, and procedures for performing voltage checks and adjustments. The following drawings are included in this manual for convenient reference:

Functional Schematic	Chassis Assembly	Component Locator
34-030D08	34-030D03	35-615E03 (High Voltage Board) 35-614C03 (Battery Option Board)

2.2 GENERAL SPECIFICATIONS

Input

115 or 230 Vac ± 10%, 50 or 60 Hz

Outputs

P5	+ 5.0 Vdc	25.0 Amperes
P12	+ 12.0 Vdc	2.0 Amperes

Regulation

Mnemonic	
P5	<160mv (No Load to Full Load)
P12	<160mv (No Load to Full Load)

Ripple and Noise (Maximum peak to peak)

Mnemonic	
P5	<70mv
P12	<30mv

Ambient Temperature Range

Operating	0°C TO 50°C
Storage	-40°C TO +70°C

Output Current Limiting

Mnemonic	Max Short Circuit Output Current
P5	<34 AMPS
P12	<1.0 AMPS

2.3 THEORY OF OPERATION

This section describes the operation of the 34-030 Power Conditioner. First, a general overview is presented in the section entitled Block Diagram Description. Second, the block diagram of Figure 2-1 is explained in greater detail in the section entitled Circuit Description.

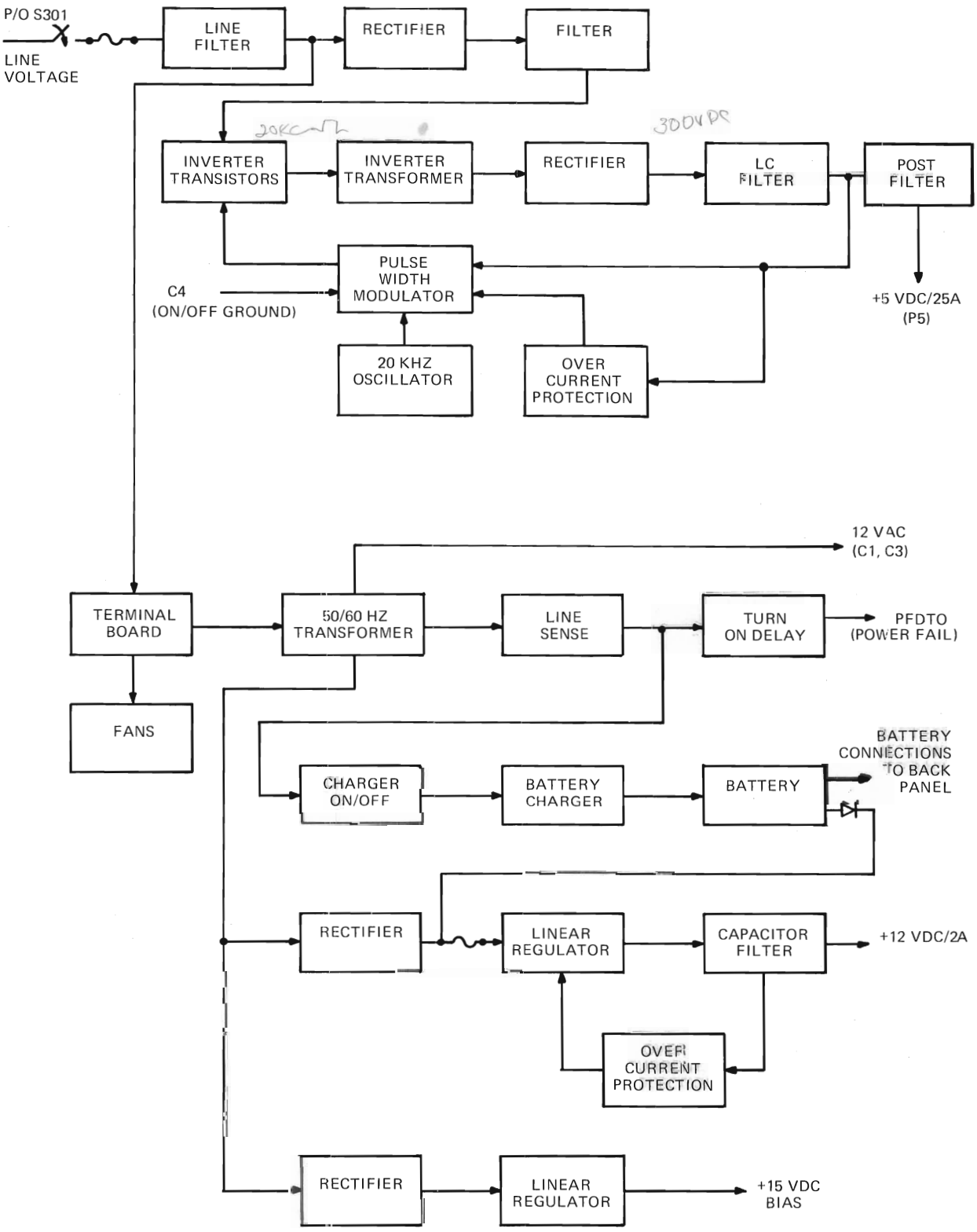


Figure 2-1. Power Conditioner Block Diagram

2.3.1 Block Diagram Description

With the line switch (S301) placed in the ON position, the Display Panel LOCK-ON-OFF switch controls the +5 volt output (P5) of the Power Conditioner. With the Display switch to the OFF position, P5 is not active, but the +12 volt output (P12) remains active to maintain information stored in the memory. The rectifier and filter (capacitor bank) produce 300 Vdc from the ac line. This dc voltage is first converted into a 20 kHz square wave by the pulse width modulator, 20 kHz oscillator, and inverter transistors, and then applied to the primary side of the inverter transformer. The voltage is stepped down to an appropriate level for the P5 output. Next, full wave rectification occurs and the signal is applied to the LC filter for smoothing. The pulse width modulator senses the +5 volt output to regulate P5 by controlling the 20 kHz square wave duty cycle. The +12 volt circuit receives its input voltage from the 50/60 Hz transformer. This ac voltage is rectified and applied to a linear (pass) regulator and capacitor filter to produce P12. Both P12 and 12 Vac output produced by the 50/60 Hz transformer are independent of the Display Panel switch. The 50/60 Hz transformer also energizes the +15 Vdc bias supply to energize the Power Conditioner's control circuits.

2.3.2 Circuit Description

The following sections describe in greater detail the major functional elements of the Power Conditioner. The reader, when referring to the functional schematic 34-030D08, should observe the following convention to locate a circuit area or component being described in the text. In the three digit coordinate given in parentheses, for example, (1H2), the first digit (1) refers to sheet 1 and the next two digits (H2) refer to the coordinates of the circuit component, transformer T101 in this case.

2.3.2.1 Rectifier And Filter (115 Vac Connection)

If the unit is connected for 115 Vac line operation, the rectifier is connected as a doubler, producing 300 Vdc. The filter capacitors charge through the series resistors R301 (1D1) and R302 (1D2) limiting the turn-on current and preventing turn-on surges from causing equipment malfunction.

2.3.2.2 Rectifier And Filter (230 Vac Connection)

If the unit is connected for 230 Vac operation, a bridge rectifier is used rather than the doubler for 115 Vac operation. However, in both cases, the rectifier output is approximately 300 Vdc. Removing the strap at TB301 pin 1 and pin 2 (2A4), converts the rectifier D301 (1D1) into a bridge rectifier.

2.3.2.3 Inverter Transistors And Inverter Transformer

Two high voltage transistors Q103 and Q105 (1H3) switch the rectified line (300Vdc) through the inverter transformer T102 (1J1) at a 20 kHz rate. Capacitors C110 and C111 (1G1) divide the 300 Vdc into two 150 volt sources. Transistor Q103 switches the upper 150 volt source and transistor Q105 switches the lower source. Base drive to Q103 and Q105 is supplied from T101 (1H2). Integrated circuit A104 (1G4) controls the base drive to the high voltage transistors.

Other secondaries on T101 (pins 4, 5 and 8, 9) supply additional drive power to the high voltage transistor bases. As current through these windings increases due to increasing load requirements, additional drive power becomes available. Turn off drive is provided by both Q117, D105 (1F3) and Q114, D107 (1F3) circuit components.

2.3.2.4 5 Volt Rectifier And Filter

Schottky rectifiers D101 and D102 (1K1) rectify up to 25 amperes of P5 output current. Pulsating dc is filtered through inductor L102 (1K2) and capacitor C108 (1L1). Output current flowing through resistor R104 (1K2) provides a current sensing signal for the P5 overcurrent circuit.

2.3.2.5 Pulse Width Modulator Circuit

The pulse width modulator circuit monitors the P5 output voltage and modulates the duty cycle of the high voltage transistors to maintain P5 at +5 volts in line with load variations. The P5 output current is also monitored and controlled to prevent overloading the unit. A +5 volt reference is established by integrated circuit A104 (1G4). The A104 unit compares this reference to the P5 output voltage and produces an error signal at its output, pin 10. The level of this signal is compared to the sawtooth riding on a dc level generated at the base of Q132 (1D4). The on time of Q131 (1E4) and Q115 (1E2) is varied to control the on time of the high voltage transistors.

2.3.2.6 +12 Volt Regulator

Zener diode D103 (2E4) provides a reference for dual transistor Q108 (1H3) which acts as a differential amplifier. The output voltage is fed back through R107 (2J2) and R115 (2J4). The amplified error signal appears at pin 7 of Q108 and controls the conduction of Q107 and Q106 that act as drivers for pass transistors Q104 and Q101 (2G2). Resistor R120 (2F2) monitors output current for overload protection.

2.3.2.7 +15 Volt Bias Supply

Integrated circuit A101 (2E7) forms a +5 volt reference. The A101 unit compares the output voltage to the reference and the amplified error signal appears at pin 10 to control pass transistor Q102 (2E6). The current is monitored through R128 (2F6) for overload protection.

2.3.2.8 Line Sense Circuit

The ac line is monitored by a winding from T301, pins 5, 6 and 7 (1A6). The output appears at D109 (1H7) and is high when the ac line is too low for operation. This signal holds the inverter transistors in the off mode resulting in no P5 output. This circuit does not control the P12 output or the unregulated ac output across C1 through C3.

2.3.2.9 KEY CONTROL (C4)

This signal from the Display Panel is received by the Power Conditioner (1B5) and only controls the P5 output. When a low (short to ground) is received, the P5 output is enabled.

2.3.2.10 POWER FAIL (PFDTO)

The power fail circuit receives its input signal at the anode of D110 (1J7). Its signal is from the line sense circuit or the key control function. Upon receiving a high, the PFDTO output is low indicating either a fault in the ac power or an OFF command from the Display Panel key. When a low is received, P5 is allowed to rise, and at least 1.5 seconds later, PFDTO will change state to a high. When an OFF command is received, PFDTO will drop to a low, and at a minimum of 3ms later, P5 will go out of regulation.

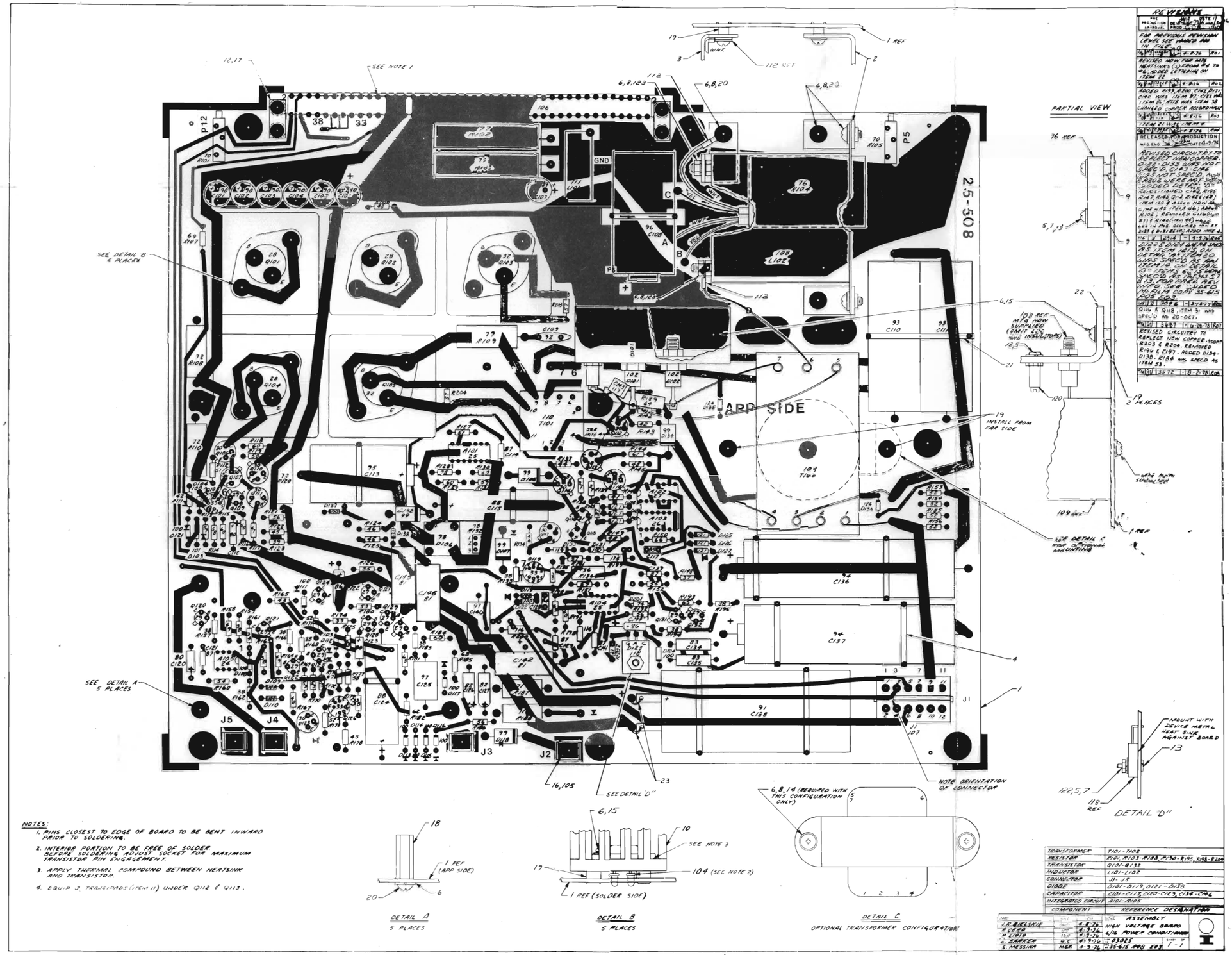
2.3.2.11 Battery Option

The battery option includes the following: a battery, battery charger, and a charger ON/OFF. The battery supports the P12 output in the event of ac power failure and is capable of maintaining the P12 output in regulation for a minimum of 1.5 hours.

2.4 VOLTAGE CHECKS AND ADJUSTMENTS

Although the Power Conditioner voltages are adjusted at the factory, the user should verify all voltages prior to connecting the unit to the system. Some voltage checks and adjustments require the Power Conditioner tray to be pulled out, while others can be performed with the tray in. Refer to the high voltage board assembly drawing (35-615E03) and the battery option board assembly drawing (35-614C03) for the location of components and adjustments. Steps 4 through 6 in the following procedure are optional with the battery charger board.

1. Pull out tray to expose the high voltage board components.
2. Measure the dc voltage across the capacitor C115.
3. If necessary, adjust potentiometer R132 for a 15±.05 Vdc reading.
4. Disconnect the battery cables from J3 and J5.
5. Measure the voltage across J3 and J5.
6. If necessary, adjust potentiometer R415 at the battery charger board for a reading of 21.0 Vdc and connect the battery cables to J3 and J5.
7. Push the tray in.
8. At the rear panel, measure the dc voltage across one of the gold pins 28, 29 or 30 of slot 5 and the GND faston.
9. Adjust P12 for a +12±.05 Vdc reading.
10. Measure the voltage across the P5 faston and the GND faston.
11. Adjust potentiometer P5 for a +5±.05 Vdc reading.



REVISIONS

		FOR PRODUCTION RELEASE	DATE 7-8-76	
		FOR PREVIOUS REVISION LEVEL SEE PAGES AN IN FILE		
A	1	7-8-76		901
		REVISED NOTE FOR MTG HEATSINKS (2) FROM 4A TO 4G. ADDED LETTERING ON ITEM 22		
A	2	7-8-76		902
		ADDED A29 FROM THE DIAG. CKT. WAS ITEM 87, C122 WAS ITEM 75, R118 WAS ITEM 38 CHANGED JUMPER ASSIGNMENT		
A	3	7-8-76		903
		ITEM 11, 12, 13 ITEM 14		
A	4	7-8-76		904
		RELEASED FOR PRODUCTION MFG ENG	DATE 8-3-76	
		REVISED CIRCUITRY TO REFLECT NEW COPPER. DISC. D133 WAS NOT SPEC'D. C93-C96, L133 NOT SPEC'D. R202 & 203 ARE NOT SPEC'D. ADDED DETAIL 'D'. REVISED TABLE. CHG. R105 FROM 2.4 K Ω, 1/2 W TO 2.4 K Ω, 1 W. ITEM 106 & ASSOC. HDW CHG. WAS 1703-1 (BLK) HDWE R102. REVISED CIRCUITRY R213 & R140 (ITEM 84) WAS 1/4 W, NOW 1/2 W. ADDED R215 & D135 & D136 ADDED NOTE 4.		
A	5	12-14	9-9-76	905
		Q102 & D104 WERE SWAPPED AS PER ECN 10,044 DETAIL 'D' ITEM 20 WAS SPEC'D AS ITEM 19 ON DETAIL 'D' ITEM 6 WAS CHG'D TO SPECIFY MFG AS 3 & 13. ITEM 3 WAS CHG'D TO MFG AS MILFAM PART 35-875 FOR 5KV		
A	6	3572	9-27-76	906
		Q114 & Q118, ITEM 31 WAS SPEC'D AS 20-027.		
A	7	3687	10-28-76	907
		REVISED CIRCUITRY TO REFLECT NEW COPPER - FROM R203 & R206. REMOVED R196 & D197. ADDED D136-D138. R198 WAS SPEC'D AS ITEM 53.		
A	8	3532	8-2-76	908

TRANSFORMER	T101 - T102
RESISTOR	R101, R103-R188, R190-R195, R198-R204
TRANSISTOR	Q101-Q132
INDUCTOR	L101-L102
CONNECTOR	J1 - J5
DIODE	D101-D119, D121 - D130
CAPACITOR	C101-C117, C120-C129, C134-C146
INTEGRATED CIRCUIT	A101-A105
COMPONENT	REFERENCE DESIGNATION

NAME	TITLE	DATE	SIZE ASSEMBLY
J.R. RADESKIE	ENG	4-8-76	HIGH VOLTAGE BOARD
R. CEBA	DES	4-9-76	4/16 POWER CONDITIONER
P. LEWIS	TECH	4-9-76	
K. GARRECK	QC	4-9-76	371022
S. MESSINA	MFR	4-9-76	35-615 REV EDIT

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REVISIONS		
PRE PRODUCTION APPROVAL	INIT DEV	DATE 9-13-76

AREA F3 & F4 : Q118 & Q116 WERE SPEC'D AS 20-027. P.C. BRD 35-615F01 WAS R00.

W/A 3687 | 5-31-78 | R01

AREA H1: C110 & C111 WERE SPEC'D AS 15.00V. AREA H2: T101 WAS SPEC'D AS 30-049F01. AREA F2: D134, 23-025 WAS NOT SPEC'D. AREA H1 & J3: D135 & D136 (23-017) WERE NOT SPEC'D. AREA H2 & H3 DELETED R196 FROM EMITTER Q103. ADDED R203, 13.3 TO BASE Q103. DELETED R197 FROM EMITTER Q105. ADDED R204, 13.3 TO BASE Q105. AREA G3: CONNECTED ANODE OF D107 & D105 TO GND. AREA C5 D137, 23-034 & D138 23-036 WERE NOT SPEC'D. AREA D5: R184 WAS SPEC'D AS 68K. AREA E5 COLLECTOR OF Q129 WAS CONNECTED TO COLLECTOR OF Q128 P.C. Brd. 35-615F01 WAS R00. REVISE SHT. 2.

W/A 3572 | 6-13-78 | R02

COMPONENT NUMBERING	
101-299	HI VOLTAGE BOARD
301-399	CHASSIS
401-499	BATTERY OPTION BD

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-614R01	BATTERY OPTION
35-615F01 R07	HI VOLTAGE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

USED IN MANUAL 29-494

SHEET	REV. LEVEL	2	/	
INDEX	SHT. NO.	1	2	3

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   :ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
   :ALL CAPACITORS ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE PART OF 35-615F01.
3. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

SCALE – N

NAME	TITLE	DATE
J. CONWAY	DRAFT	7-8-76
R.F. CERO	CHK	9-9-76
E. CENTOFANTI	ENGR	
B. MULLER	SYS TEST	
S. MESSINA	MGR	

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TASK NO. 03013 | DWG NO. 34-030R02D08 | SHEET OF 1 — 3

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REVISIONS			
AREA M5 : 12VAC/50MA WAS SPEC'D AS 5VAC/50MA.			
WAW	3572	6-13-78	R01

T301 P/O 30-051

F303 4A

D302 23-023

J2 — J1 — P1

D118 23-025 — BATTERY STAND-BY — 3L1

D104 23-034

R111 3.3K

R110

Q104(HS) 20-006

R108 0.1, 5W WW

(HS) 20-006 — R109 0.1 5W WW

R120 0.2 5W WW

R123 47K

R122 15K

R121 1K 1%

R118 10K 1%

R119 10

Q101

R112 390

Q111 20-023

Q106 20-023

Q110 20-023

Q107 20-023

P12/2A — 12B-2-130-2, 22B-2-230-2

C138 4800 50V

D121 23-034

Q109 20-013

R101 10K

Q108 20-038

R107 6.99K 1%

C102 150 16V

C104 150 16V

C106 150 16V

D103 23-040 MPD2 6.2V 5%

R115 10K 1%

R116 20K 1%

C112 2.2 20V

R117 200K

R114 23.7K 1%

R113 4.99K 1%

C101 150 16V

C103 150 16V

C105 150 16V

P12 GND 1C6

P12 GND 1E4

P12 GND

123 GND J8

115V 230V

78301

B 142 A 141

J301 P301

(B301) (B302)

R188 68 2W

R187 68 2W

SEE NOTE 1

Q3 — 141-2

12 VAC 50 MA

C1 — 240-2

CHARGER INPUT — 3A1

Q102 20-006 (HS)

R128 2 1W WW

P15 BIAS

R127 390

D106 23-046

C113 1000 75V

R101 19-094

R129 10K 1%

R131 4.99K 1%

R132 10K

R130 10K 1%

C114 0.1 30V

D132 23-025

C115 100 50V

P15 AUX — 1F2, 1G6

C145 100 25V

C146 100 25V

P5 GND — R5

CHARGER INPUT GND — 3A5

CHASSIS ASSY P/O 11-200

HI VOLTAGE BOARD P/O 35-615F01

NOTES:
1. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

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		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

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DWG NO 34-030 R01 D08
SHEET OF 2 — 3

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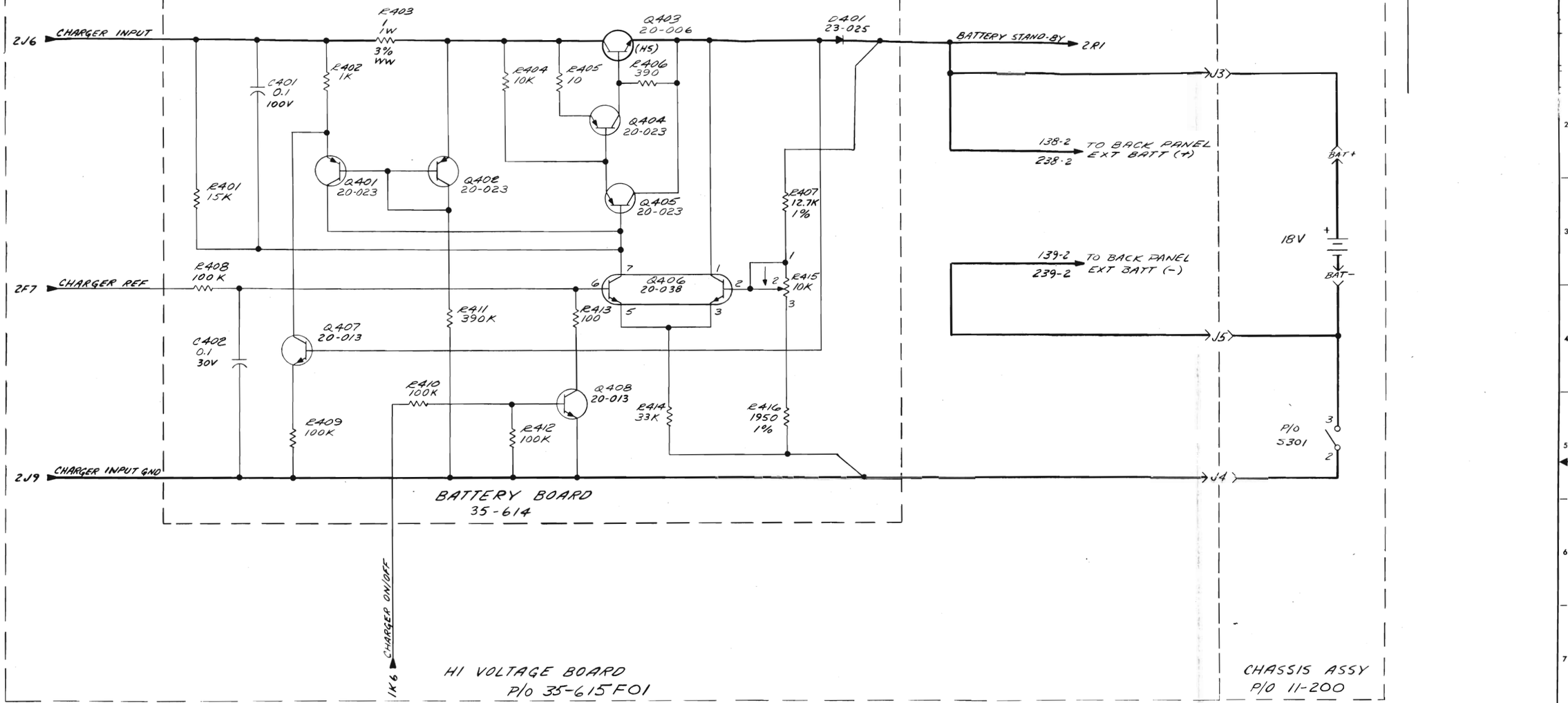

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	NAME	DATE
SCALE – N	B. GRAY	11-8-75
DRAFT		
CHK		
ENGR		

TITLE FUNCTIONAL SCHEMATIC POWER CONDITIONER

DWG 03013
34030 008
SHEET 3 OF 3

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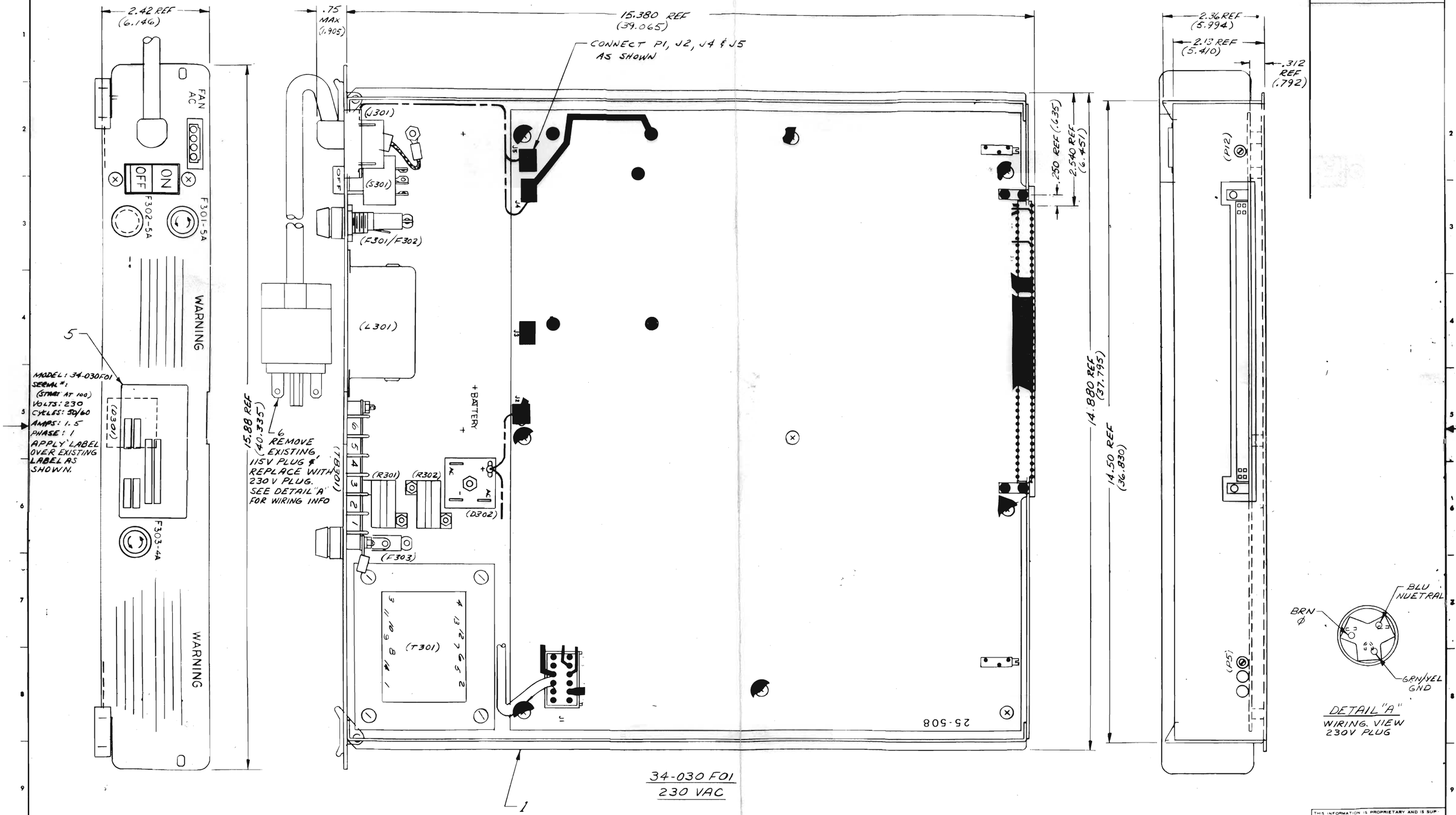
REVISIONS



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	NAME	DATE
SCALE – 1–1	R. SEAY	DRAFT 1-30-78
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	R. CERO	CHK
	G. WELLY	ENGR
	R.A. BARKER	Q.C.
	P. ABITANTE	MGR

TITLE ASSEMBLY, SEMI-MEMORY POWER CONDITIONER (VDE) 230 VAC

SIZE A, CAGE NO 03077 (8881), DWG NO 34-030 R02 D03, SHEET 2 OF 2

DRAWING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	BS	7-12-76
PROD	CSL	7-12-76

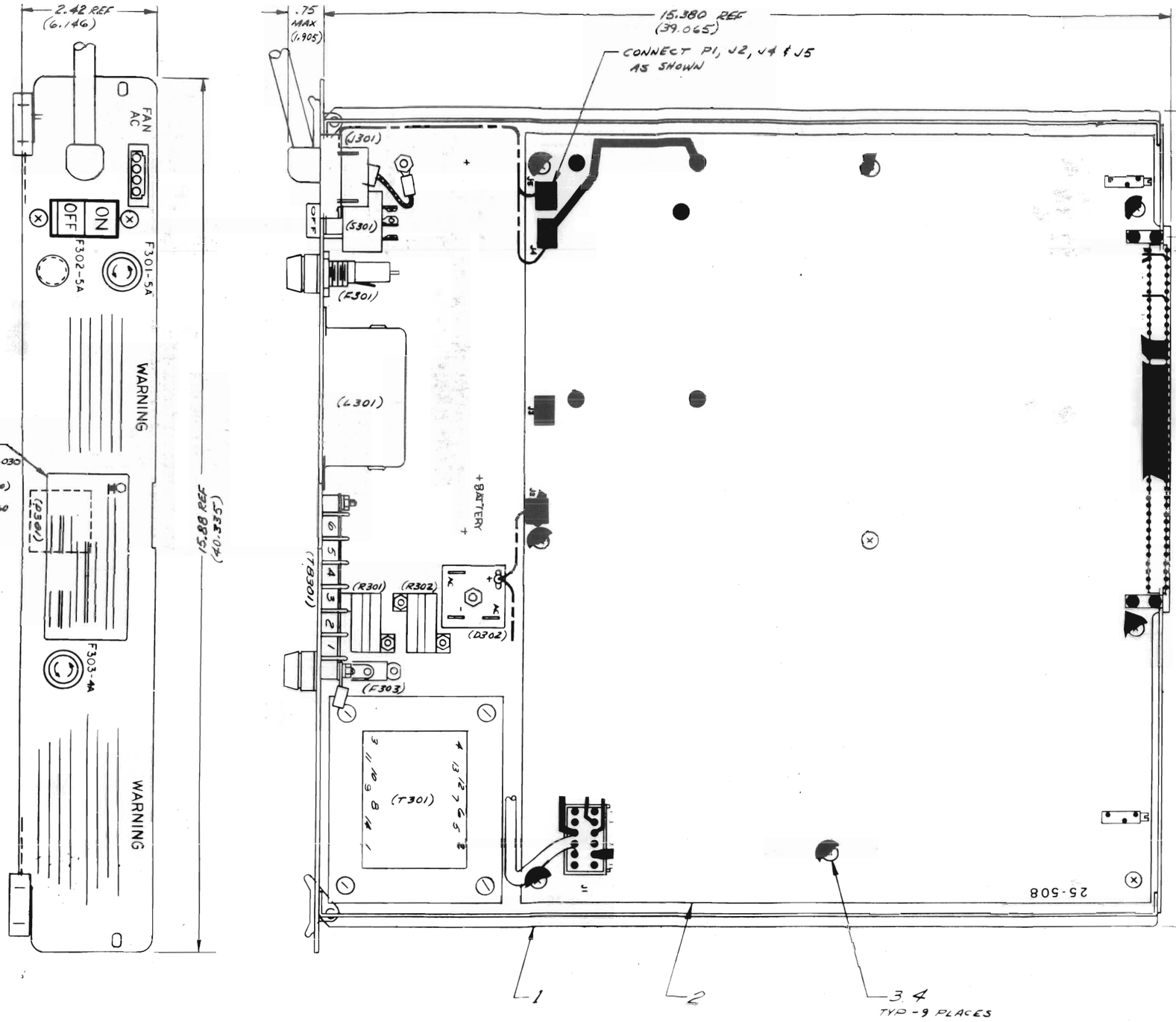
LOCATION B7. F303-4A WAS SPEC'D AS F303-3A

NS	K	2914	-	8-30-76 A01

RELEASED FOR PRODUCTION
MFG ENG. [illegible] DATE 11/4/77

ADDED SHT. 2. ASSY WAS SPEC'D AS SHT 1-1 IN AREA AS 115V WAS 115/230, 3.0A WAS 3.0/1.5

NTA	BV	3592	6-27-78	B02



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SCALE - 1-1

NAME	TITLE	DATE
J CONWAY	DRAFT	7 7 76
R F CERO	CHK	9 9 76
E CENTOFANTI	ENGR	1 7 77
R A BARKER	QC	12 30 76
L PEZZI	MGR	1 10 77

TITLE ASSEMBLY, SEMI-MEMORY POWER CONDITIONER (VDE) 115 VOLTS

DWG NO 03013 SHEET OF 1 — 2

ASSY NO 34-030R02003

DRAWING 44-231 24538

Publication Number 29-603

MODEL 5/16
MAINTENANCE MANUAL

INTERDATA®
A UNIT OF
PERKIN-ELMER DATA SYSTEMS
2 Crescent Place, Oceanport, New Jersey 07757 • (201) 229-4040

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Printed in U.S.A.
August 1977

RECEIVED AUG 1 7 1977

PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-603

TITLE Model 5/16 Maintenance Manual

REVISION R00 DATE 8/77

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
Title Page	R00	8/77	35-638 D03	R01	7/77			
i/ii	R00	8/77	35-638 D08	R01	7/77			
iii thru vi	R00	8/77	35-639 D03	R00	7/77			
1-1 thru 1-18	R00	8/77	35-639	R00	7/77			
2-1 thru 2-15/ 2-16	R00	8/77	35-640 D03	R01	7/77			
3-1 thru 3-44	R00	8/77	35-640 D08	R02	7/77			
4-1 thru 4-4	R00	8/77						
A1-1/ A1-2	R00	8/77						
A2-1 thru A2-5/ A2-6	R00	8/77						
A3-1 thru A3-41/ A3-42	R00	8/77						
A4-1 thru A4-10	R00	8/77						
01-100 D12	R00	7/77						
02-276 D08	R01	7/77						
17-436 D08	R00	7/77						
34-028 D03	R04	5/77						
34-028 D08	R04	5/77						
35-637 E03	R01	7/77						
35-637 D08	R01	7/77						

FOREWORD

This manual provides the necessary information required to install and maintain the Model 5/16 Processor. Chapter 1 contains a general description of the 5/16 Processor plus detailed information and illustrations about the INTERDATA part numbering and drawing systems. Chapter 2 provides procedures required to physically install the 5/16 Processor and expansion chassis. Chapter 3 contains comprehensive maintenance information including a block diagram analysis of the 5/16 Processor, a micro-program description, the data and instruction word formats, a description of the micro-code, and a functional diagram analysis of the 5/16 Processor. Appendixes provide a mnemonics list for easy location of signals in the schematic diagrams and the microcode listings for reference.

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5/16 ROM Option Component Locator	35-639R00D03
5/16 ROM Option Schematic Diagram	35-639R00D08
5/16 RAM Option Component Locator	35-640R01D03
5/16 RAM Option Schematic Diagram	35-640R02D08

CHAPTER 1
MODEL 5/16 GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 5/16 combines advanced circuits and packaging designs to give the user a price/performance optimized machine. The Model 5/16 is completely upward compatible with INTERDATA Models 3, 4, 74, and 7/16 Basic Processor user instruction set, interrupt handling, input-output formats, and control sequencing. In addition, many of the powerful features of the INTERDATA Models 5, 70, and 80 are included. Because of this compatibility, the Model 5/16 can use a wide range of existing software and peripheral devices.

The Model 5/16 offers a comprehensive set of 100 instructions making the system both easy to program and efficient to operate. Through multi-function instructions and direct-memory addressing, coding and debugging time is reduced to a minimum.

Memory is addressable to the eight-bit byte level, and is expandable from the basic 8,192 bytes to 65,536 bytes. All memory is directly addressable with the primary instructions; no paging or indirect addressing is required. Sixteen 16-Bit general registers can be used as accumulators, fifteen of which can also be used as index registers. Register-to-register instructions permit operations between any of the sixteen general registers, eliminating redundant loads and stores.

The Model 5/16 also provides a flexible Input/Output system in addition to conventional means of programmed I/O. In the Automatic I/O Service Mode, the Processor acknowledges all I/O interrupts and automatically performs much of the overhead prior to activating the Interrupt Service Routine.

1.2 SCOPE

This chapter is intended to enable the digital technician to understand the INTERDATA documentation system. Number Notation, the Part Numbering System, and the Drawing System are described. Illustrations are provided to help understand these systems. Another publication which may be of interest to Model 5/16 users is the Model 5/16 User's Reference Manual, Publication Number 29-588.

A cross reference between INTERDATA part numbers and standard industry part numbers for the ICs and transistors found in the Model 5/16 may be found at the end of this chapter.

1.3 DOCUMENTATION

This paragraph describes the style and conventions used with INTERDATA documentation.

1.3.1 Number Notation

The most common form of number notation used in INTERDATA documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 1-1 lists the hexadecimal characters employed.

TABLE 1-1. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hex	Binary	Decimal	Hex	Binary	Decimal	Hex
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

To differentiate between decimal and hexadecimal numbers, hexadecimal numbers are preceded by the letter "X," and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are X`1234', X`2EC6', X`A340', X`EEFA', and X`10B9'.

1.3.2 Part Numbering System

INTERDATA parts, drawings, and publications use a common numbering system. The part number and drawing numbers for drawings which describe the part are related. The publication number is often related to the part number of the device or program described. Figure 1-1 shows the format used for INTERDATA part numbers. The fields are described in the following paragraphs.

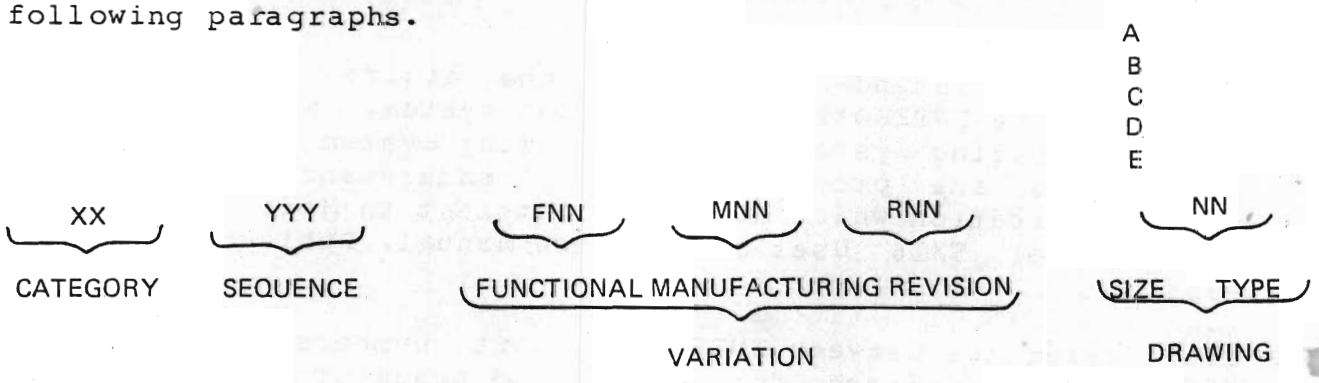


Figure 1-1. Part Number Format

1.3.3 Category Field

The two-digit Category Number indicates the broad class or category to which a part belongs. Typical examples of category number assignments are:

01 - Basic Hardware Systems
02 - Basic Hardware Expansions
03 - Basic Software Systems
04 - Software Packages
05 - Micro-programs
06 - Test Programs
07 - Subroutines of General Utility
10 - Spare Parts Packages
12 - Card File Assemblies
13 - Panels
17 - Wire and Cables
19 - Integrated Circuits
20 - Transistors
27 - Peripheral Equipment
29 - Manuals
34 - Power Supplies
35 - Assembled Printed Circuit Boards
36 - Electro-Mechanical Devices

1.3.4 Sequence Field

The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 1-1 are minimum lengths (insignificant zeros must be added to maintain these minimums).

1.3.5 Functional Variation Field

The optional Functional Variation Field consists of the letter "F" followed by two digits. The F field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For example, a power supply may be strapped internally to operate on either 110 VAC or 220 VAC. Except for this strap, all power supplies of this type are identical. The strapping option is easily described by a note on the assembly and test specification drawings. Therefore, this is a functional variation.

1.3.6 Manufacturing Variation Field

The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

An important exception to the meaning of the M Field exists for categories related to software. In software, the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they can be in symbolic form or in relative or absolute binary form. Thus, there are many ways to present the same identical program.

The format for the M Field and its meaning for software is:

Mxy

where x identifies the media selection (i.e., Paper Tape, Magnetic Tape, Cassette, etc.) and y identifies object or source and the format.

Meaning of x		Meaning of y	
Conceptual	0	1	Object program standard format 32-Bit Processor
Paper Tape	1		
Cassette	2	4	Memory image
Magnetic Tape (800 BPI)	3	6	Object Program standard format 16-Bit Processor
Cards	4	7	Object non-standard format
Disc (2.5 MB)	5	8	Object established task
Disc (10MB)	6	9	Source program
Magnetic Tape (1600 BPI)	7		

These numbers refer to the physical program placed on an approved media for INTERDATA Software. A Paper Tape Object program is standard format and, for a 16-Bit Processor, has an M16 identifier. A Magnetic Tape Object program is standard and, for a 32-Bit Processor, has an M31 identifier.

In addition to the foregoing, there are three unique M numbers which have special meaning:

00 Conceptual Object
91 32 Bit Object Listing
92 Programming Specifications
95 Program Description
96 16 Bit Object Listing

98 Operating Procedures
99 Documentation and Manuals

1.3.7 Revision Field

The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. The R field changes often reflect improvements. A part with a revision level HIGHER than the one specified can be used; however, a part with a revision level LOWER than specified should not be used.

NOTE

A part number must contain a Category number and a Sequence number. All other fields are optional.

1.3.8 Drawing Field

The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A - 8 1/2" x 11"
B - 11" x 17"
C - 17" x 22"
D - 22" x 34"
E - 34" x 44"

The two digits indicate the drawing type as follows:

01 - Parts List
02 - Machine Details
03 - Assembly Details
05 - Art Details
06 - Wire Run List
08 - Schematic
09 - Test Specification
10 - Purchase Specification
11 - Bill of Material
12 - Information
13 - Program Listing
14 - Abstracts
15 - Program Description
16 - Operating Instruction
17 - Program Design Specifications
18 - Flow Charts
19 - Product Specification
20 - Installation Specification
21 - Maintenance Specification
22 - Programming Specification
23 - Replaceable Parts List
24 - Application Information
25 - Functional Specifications

Examples

The following list provides some examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060 The 60th printed circuit board assigned a part number under this system.

35-060M01 A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.

35-060F01 A printed circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.

35-060R01 A revised 35-060 printed circuit board which probably supercedes the 35-060.

35-060A01 The 8 1/2 by 11 inch parts list for a 35-060.

35-060B08 The 11 by 17 inch schematic for a 35-060.

06-072A13 An 8 1/2 by 11 inch listing of the 06-072 program.

06-072A12 An 8 1/2 by 11 inch information drawing on the 06-072 program. Probably a part of the program.

29-060 The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

1.3.9 Drawing System

This paragraph describes the drawings provided with INTERDATA equipment. Drawings provided with peripheral devices and other purchased items may vary from the system described in this paragraph.

A digital system may be divided into a collection of functionally independent circuits such as Memory, Processor, and I/O Device Controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each schematic contains a variety of information including type and location of discreet Integrated Circuits (ICs), pin connections, all interconnections within the schematic, connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register mnemonic name has a maximum of three letters, excluding "I, O, Q, and Z".

2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant positions, and continuing to N-1 on the right, where N is the number of bits in the register.

3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The ICs mounted directly to the logic board are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. Refer to Figure 1-2.

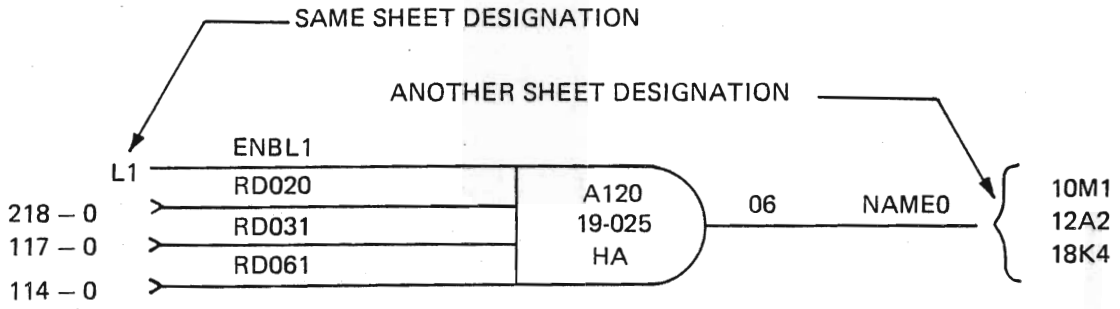


Figure 1-2. Example of a High Speed AND Gate

The designations, numbers, and references shown in Figure 1-2 are:

A20 - This shows the component location on the logic board. Figure 1-2 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connectors (Conn 0 and Conn 1) are on the right and components on top, the components are numbered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is 01 and the first capacitor is C1.

19-025 -The number 19 is the category number of ICs, and the 025 is the sequence number of the component.

HA - Designates that this component is a high speed AND gate. Some other common designators used are:

- P - Power Gate
- SB - Schottky High Speed Power Gate
- SG - Schottky Gate
- SG0 - Schottky High Speed Gate, Open Collector
- SO - Schottky High Speed Gate, Open Collector
- B - Buffer
- SB - Schottky High Speed Buffer
- LOR - Low Power Schottky OR
- LN - Low Power Schottky NOR

L1 - This input lead is from area L1 on the same schematic sheet.

10M1, 1242, 18K4 - Designate outputs to another logic schematic sheet.

218-0, 117-0, 114-0 - Designate inputs from Connector 0.

Pin numbers (01, 02, 04, 05 and 06) correspond directly to the actual IC pin numbers.

Figure 1-3 shows the locations of the header connectors (Conn 0 and Conn 1) and the cable connectors (Conn 2 and Conn 3). All logic boards always contain Header Connectors 0 and 1; however, any combination (either, both, or none) of cable connectors (Conn 2 and Conn 3) may be provided.

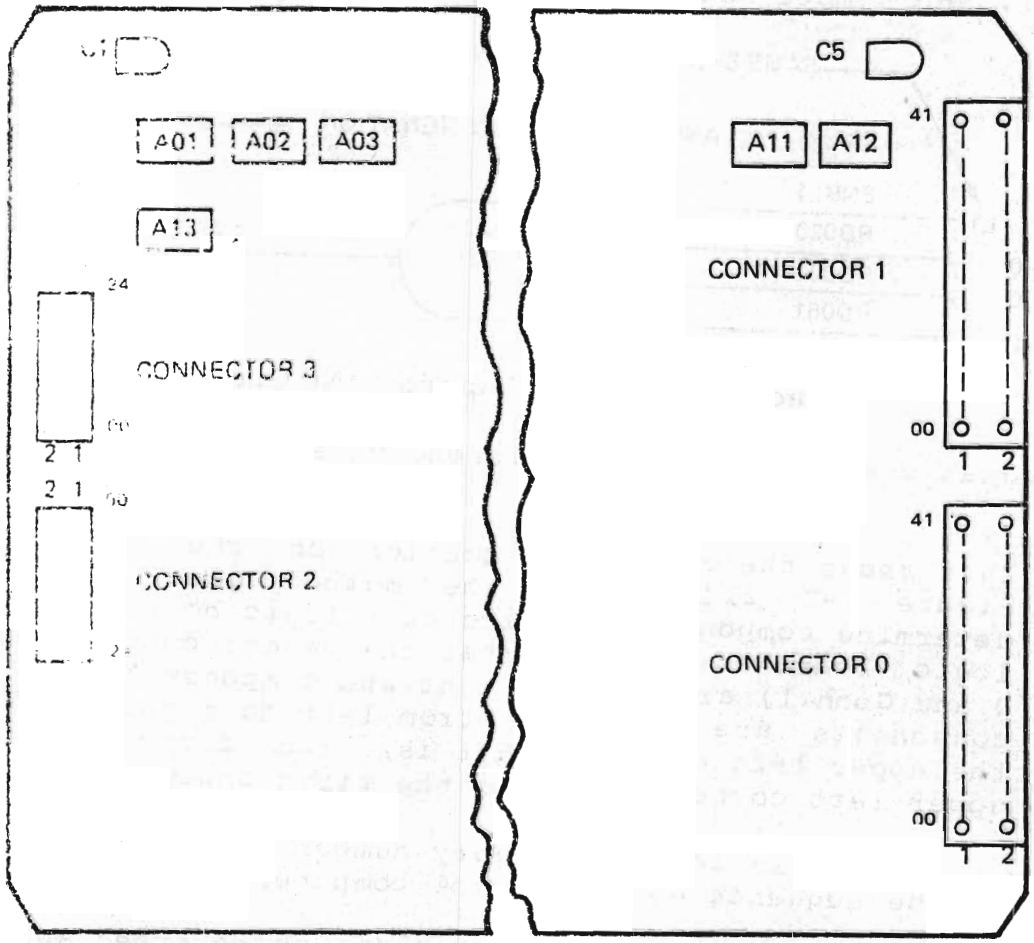


Figure 1-3. Example of a Logic Board Layout

Whenever possible, the immediate output from a flip-flop (1 or 0 side) has a mnemonic name preceded by an F. A flip-flop whose name is PSEL (processor selected) has an output mnemonic, on the 0 side, FPSEL0 (see Figure 1-4). This provides the digital technician with an indication, when observing a mnemonic at the terminal end of a net, that the signal is the output of a flip-flop rather than a decoded function.

Clocked devices, flip-flops, and counters, in particular, are drawn in a manner which indicates information concerning their inputs. An input which has a circle adjacent to the pin designation implies that a low active signal is required to perform the specified operation. In addition, an inverted V at the clock input shows that the device changes state on an edge. Thus, if no circle is present the chip is positive edge triggered. Refer to Figure 1-4 for examples.

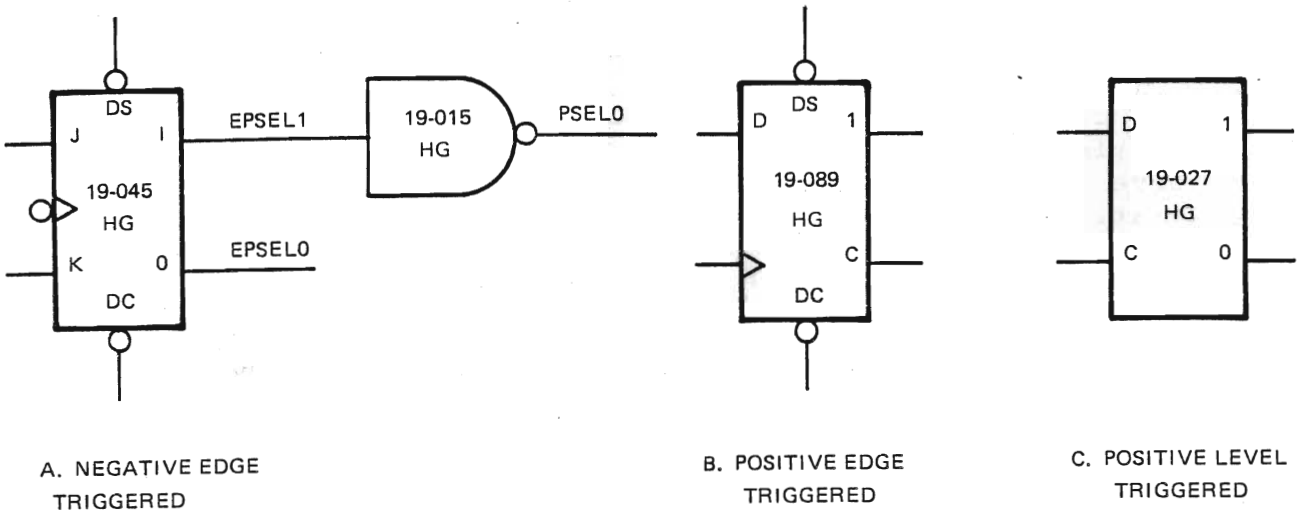


Figure 1-4. Examples of Clocked Devices

Figure 1-5 shows the pin numbering scheme for the header and cable connectors. Header connectors always have two rows of pins and 42 positions. Cable connectors always have two rows of pins but may vary in the number of positions. The number of positions may only vary in increments of five positions (10 contacts). For instance, if 24 positions are desired, five blocks of five positions each (25 positions) must be used.

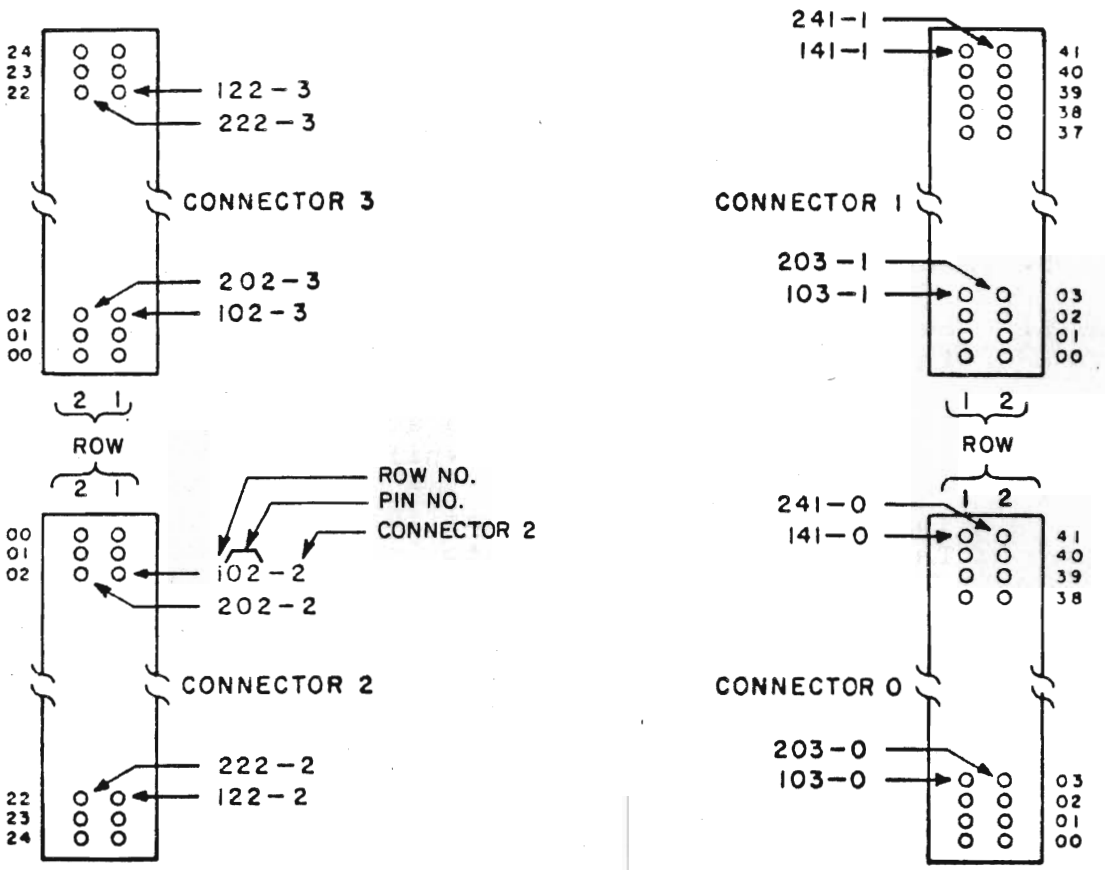


Figure 1-5. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually a collector where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules are observed.

1. All mnemonic names are a maximum of six characters.
2. All decimal digits and upper case letters except the letters "I, O, Q, and Z" are permitted.
3. No other characters are permitted.
4. Where possible, mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a mnemonic exists.
5. Mnemonic names are not repeated within a schematic.
6. Every mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop has the "1" state indicator, while the reset side has the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion. Logic 0 = .5VDC or less, Logic 1 = 2.4VDC or more.
7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same mnemonic name. For example, assume a signal NAME1 which may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

There are times when a net fans-out to many sheets of a schematic. It is also possible for a net to fan-out to sheets on different schematics. In such situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 1-2 is on a schematic, Sheet 20. The output NAME0, appears on Sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 1-2 the ENABL1 may have many other terminations in addition to the one shown. Generally, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that on schematics, signals are coordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the Back Panel Map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 1-2, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figure 1-6 is a typical schematic sheet with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic Digital System and some of the more common expansions are commonly included in the rear of the appropriate Digital System Maintenance Manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.

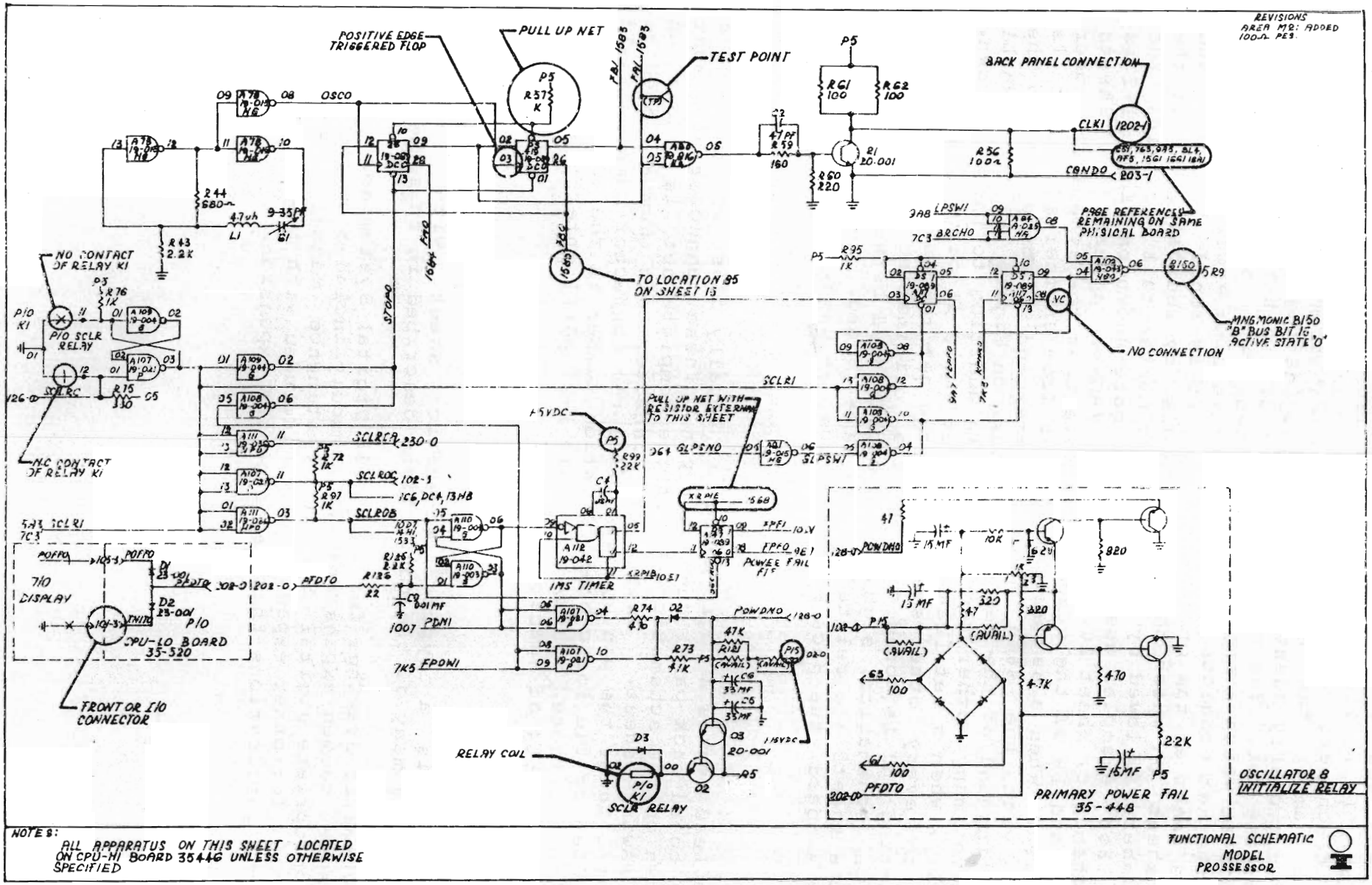


Figure 1-6. Functional Schematic Format Diagram

1.4 PART NUMBER CROSS REFERENCE LIST

The following is a cross referenced Interdata Parts List.

INTERDATA Part No.	Type	VENDOR/JEDEC Number
19-001	Dual 4 Input NAND DTL	(OBS)
19-002	Triple 3 Input NAND DTL	863
19-003	Quad 2 Input NAND DTL	849
19-004	Hex 1 Input NAND DTL	837
19-005	Dual Power Gate DTL	(OBS)
19-006	Dual Buffer DTL	(OBS)
19-007	Flip-Flop DTL	(OBS)
19-008	Gate Expander Dual 4 Input DTL	(OBS)
19-009	8 Bit Stack DTL	(OBS)
19-010	Differential Comparator LIN	710C
19-012	Dual 4 Input NAND Buffer TTL	74H40
19-013	Quad 2 Input NAND DTL	946
19-014	Dual J-K Flip-Flop DTL	(OBS)
19-015	Hex Inverter 1 Input	74H04
19-016	Quad 2 Input NAND TTL	74H00
19-017	Triple 3 Input NAND TTL	74H10
19-018	Dual 4 Input NAND TTL	74H20
19-019	Single 8 Input NAND TTL	(OBS)
19-020	Operational Amplifier LIN	(OBS)
19-021	Quad 2 Input Power DTL	(OBS)
19-022	Dual J-K Flip-Flop TTL	(OBS)
19-023	Selected Dual Buffer 19-006 with 20-30 nanosecond delay DTL	(OBS)
19-024	Triple 3 Input AND TTL	74H11
19-025	Dual + Input AND TTL	74H21
19-026	2-2-2-3 Input AND-OR TTL	74H52
19-027	4 Bit Adder TTL	7475
19-028	4 Bit Serial Adder TTL	7483
19-029	Quad Exclusive - OR TTL	7486
19-030	4 Bit Shift Register TTL	7495
19-031	One Shot TTL	74121
19-032	1 of 10 Decoder Open Collector	74145
19-033	Dual Sense Amplifier LIN	7524
19-034	Retriggerable One Shot TTL	74122
19-035	4 Bit Up/Down Counter TTL	74193
19-036	Quad 2 Input Open Collector TTL	7438
19-037	High Performance Operational Amp	748393
19-038	Dual 4 line to 1 line Mux TTL	74153
19-039	4 Bit ALU TTL	74181
19-040	4 Stage Look Ahead Carry TTL	74182
19-041	4 x 4 Register Stack TTL	74170
19-042	Dual Retriggerable One Shot TTL	74123
19-043	Quad 2 Input NAND Open Collector TTL	74H01
19-044	Hexadecimal Inverter Open Collector TTL	74H05
19-045	Dual J-K Flip-Flop TTL	(OBS)
19-046	Quad RS-232C Line Driver	ML1488
19-047	Quad RS-232C Line Receiver	MC1489A

19-048	8 Bit Shifter 24 Pin Dip	74198
19-049	1024 Bit PROM TTL	DM8587
19-050	8 Input NAND TTL	74H30
19-051	1024 Bit PROM TTL	74187
19-052	Dual 4 Input Buffer	(OBS)
19-053	4 2-line-to-1-line Data Sel. Mux	74157/9322
19-054	Quad2 Input NAND STTL	7400
19-055	Quad 2 Input NAND STTL	74S00
19-056	Quad 2 Input NAND Open Collector STTL	74S03
19-057	Hex 1 Input Inverter STTL	74S04
19-058	Triple 3 Input NAND STTL	74S10
19-059	Triple 3 Input AND STTL	74S11
19-060	Dual 4 Input NAND STTL	74S20
19-061	Dual 4 Input Buffer STTL	74S40
19-062	2-2-3-4 Input AND-OR Inverter SSTL	74S64
19-063	Dual D Edge Triggered Flip-Flop STTL	74S74
19-064	Dual J-K Flip-Flop STTL	74S112
19-065	Quad 2:1 Mux Non-Inverting STTL	74S157
19-066	Quad 2:1 Mux Inverting STTL	74S158
19-067	4 Bit ALU STTL	74S181
19-068	4 Stage Carry Look Ahead Carry STTL	74S182
19-069	8 line to 1 line Mux STTL	74151
19-070	4 Bit Synchronous Counter TTL	74161
19-071	Quad D Edge Triggered Flip-Flop	74175
19-072	4 Bit Left/Right Shift Register TTL	74194
19-973	Dual 4:1 Mux Tri-State TTL	8214(NAT)
19-074	8 Bit Priority Encoder TTL	9318(F)
19-075	16 x 4 Register Stack TTL	3101(INT)
19-076	1024 Bit Memory MOS	TM54062
19-077	256 Bit Memory TTL	6531(MON)
19-078	Dual 4 Input NAND Open Collector	74S22
19-079	Comparator Dual	NE521
19-080	1024 Bit PROM TTL	82S29(S1G)
19-081	Univ. Asynchronous Receiver/Transmitters	TR1042A (Western Digital)
19-082	2-2-3-4 Input AND-OR Invert Open Collector STTL	74S65
19-083	9 Bit Parity Generator/Checker STTL	82S62(51G)
19-085	Timer	MC1555
19-086	741 C DIP Operational Amplifier	741
19-087	747 DIP Operational Amplifier	747
19-088	733 C DIP Operational Amplifier	733
19-089	Dual D Edge Triggered Flip-Flop	74H74
19-090	High Speed (710) Differential Comparator DIP	710
19-091	Retriggerable Single One Shot	9600
19-092	Negative Voltage Regulator	1463
19-093	Positive Voltage Regulator	1469
19-094	Positive Voltage Regulator	723
19-095	Linear Positive Voltage Regulator	805
19-096	First In-First Out Serial Memory 64 Word 4 Bit	3341
19-097	Amplifier	(RES)
19-098	Quad 2:1 Multiplexer Non-Inverting	74157
19-099	Dual Sense Amplifier Inverting	75234
19-100	Dual Driver 8 Pin DIP	75452
19-101	Quad-2 Input Positive NAND Buffer	7437

19-102	6-1 Input Buffer/Buffer Open Collector	7407
19-103	1 of 10 Decoder	7442
19-104	Current Switch Memory Driver	75325
19-105	Dual Differential Driver	75114/9614
19-106	Dual Differential Receiver	75115/9615
19-107	Dual Sense Amplifier	7520
19-108	Quad 2 Input NAND	7400
19-109	Hex Inverter Buffer Driver Open Collector	7406
19-110	Hex Inverter	7404
19-111	Dual 4 Input NAND Buffer	7440
19-112	Optically Coupled Isolator	4N25
19-113	360 Dual Line Driver	75123
19-114	360 Triple Line Receiver	75124
19-115	Quad 2 Input AND TTL	74H08
19-116	Dual 4:1 Multiplexer STTL	74S153
19-117	4 Bit Magnitude Comparator STTL	74S85
19-118	Quad Bus Transceiver TTL	26S12A
19-119	Expandable AND-OR Invert TTL	74H55
19-120	Dual Timer	NE556
19-121	Matched Pair 19-085 (P.S. Timing)	(OBS)
19-122	1024 Bit PROM TTL	SEE 19-051
19-123	Dual Voltage Controlled Oscillator	74S124
19-124	4-2 Input NAND Buffer STTL	74S37
19-125	4-2 Input NAND Buffer STTL	74S38
19-126	Dual 2 Wide 2 Input AND/OR Inverter STTL	74S51
19-127	4-2 Input Exclusive OR STTL	74S86
19-128	13 Input NAND, 3-State STTL	74S134
19-129	3/8 Decoder STTL	74S138
19-130	2-4 Input NAND 50 Ohm Line Driver STTL	74S140
19-131	4D FF STTL	74S175
19-132	4 2/1 Mux STTL	74S258
19-133	4 Bit Binary Full Adder TTL	74283
19-134	Hexadecimal Buffer/Inverter TTL	8T98
19-135	4 Bit Binary Counter STTL	(98S16)
19-136	1 of 10 Decoder HS & HV	74145
19-137	Dual Peripheral Positive OR Driver 8 Pin DIP	75453(S16)
19-138	Character General	2513
19-139	Driver/Decoder	7447AN
19-140	8 Bit Latch	9334PCQM
19-141	Multi-Port Register	9338PCQM
19-142	1024 Bit PROM TTL	SEE 19-080
19-143	4K x 1 NMOS RAM	9050
19-144	4-Hysteresis Rec	8T38
19-145	Voltage Regulator + 15 Amperes	78M15AUC
19-145F01	Voltage Regulator + 12 Amperes	78M12AUC
19-145F02	Voltage Regulator -15	LM340T-15
19-146F00	Voltage Regulator -15	79M15/LM320T-15
19-146F01	Voltage Regulator -12	79M12/LM320T-15
19-146F02	Voltage Regulator -5	79M05
19-146F03	Voltage Regulator -5	7905/LM320T-5
19-147F01	8 Channel Analog Mux	H11-181A-5
19-147F02	8 Channel Analog Mux	Analog Devices A07503JN
19-148	Voltage Follower	LM310D
19-149	High Speed Op Amp	HA2-2525-5
19-150	2 Channel Analog Switch	DG1828A

		IH5048 CTW
19-151	Low Level Inst Amp	AD521JD
19-152	Linear Amp	BB3660J
19-153	4-2 Input NAND LPTTL	74LS00
19-154	Hex Inverter LPTTL	74LS00
19-155	3-3 Input NAND LPTTL	74LS10
19-156	2-4 Input NAND LPTTL	74LS20
19-157	8 Input NAND LPTTL	74LS30
19-158	4-2 Input NOR LPTTL	74LS02
19-159	4-2 Input OR LPTTL	74LS32
19-160	4-2 Input AND LPTTL	74LS08
19-161	3-3 Input AND LPTTL	74LS11
19-162	2-4 Input AND LPTTL	74LS21
19-163	4-2 Input NAND Schmitt Trigger LPTTL	74LS132
19-164	4-2 Input NAND Buffer LPTTL	74LS37A
19-165	2-D FF LPTTL	74LS74
19-166	2-JK FF LPTTL	74LS112
19-167	4-D FF LPTTL	74LS175
19-168	3 to 8 Decoder Demux LPTTL	74LS138
19-169	Hex Inverter Open Collector LPTTL	74LS05
19-170	4-2 Input NAND Open Collector LPTTL	74LS03
19-171	Dual Multivibrator	74LS123
19-172	4-2 Input Exclusive OR LPTTL	74LS86
19-173	8 to 1 AND/OR Invert Mux LPTTL	74LS151
19-174	4-2 Input AND/OR Mux LPTTL	74LS257
19-175	4-2 Input AND/OR Mux LPTTL	74LS157
19-176	4-2 Input Mux LPTTL	74LS258
19-177	4-1 Input AND/OR Mux LPTTL	74LS153
19-178	3-3-2-2 Wide AND/OR Inverter LPTTL	74LS51A
19-179	4-3-3-2 AND/OR Inverter LPTTL	74LS54
19-180	4 Bit Counter LPTTL	74LS161
19-181	4 Bit Up/Down Counter LPTTL	74LS193
19-182	4 Bit Left/Right Shift Register TTL	74LS194
19-183	2-Line Driver	75110
19-184	4 Bit Micro Controller	AMD2901
19-185	4K-Bit ROM	N82S115
19-186	4K-Bit PROM	82S215N
19-187	Quad 2:1 Mux with Storage LPTTL	74LS298
19-188	ROM Chip Programmed In House 16 Bit LSU	
19-189	ROM Chip Programmed In House 32 Bit LSU	
19-190	Quad Comparator	LM339
19-191	Quad 2-Input NOR Gate	CD4001AE
19-192	Dual D Flip Flop	CD4013AE
19-193	1024 Bit PROM TTL	SEE 19-051
19-194	2K PROM TTL	N82S131
19-195	2K PROM TTL	SEE 19-051
19-196	Quad 2 Input 3 State Mux. Non Inverting	74S257
19-197	1024 B Dynamic RAM (NMOS)	MK4096N-16
19-198	Field Programmable Logic Array	82S00
19-199F03	Field Programmable Logic Array	
19-200	16 x 4 First In-First Out (FIFO)	9430
19-201	CPU	MC6800
19-202	Peripheral Interface Adapter (PIA)	MC6820
19-203	Sync Serial Data Adapter (SSDA)	MC6852
19-204	1K RAM	MCM6810A
19-205	2 Phase Clock	MC6870A

19-206	4 Input 3 State Line Transceiver	8T26/8T26A
19-207	Error Checking, Polynomial Gen.	MC8506P
19-208	Dual VCO	MC4024P
19-210	CPU	2608-1/MCM6830P
19-213F01	5/16 Shift Control PLA	
F02	8/16E Shift Control PLA	
20-001	Transistor NPN High Speed Switch	2N3646
20-002	Transistor PNP 500 MA	MPS6534
20-003	Transistor	DT5-423/2N3902
20-004	Transistor NPN	2N5189/64493
20-005	Transistor	2N3056
20-006	Transistor NPN 15 Amps 100W T03 case	2N3055
20-007	Transistor NPN 3 Amps	TIP31A
20-008	Transistor PNP 3 Amps	TIP32A
20-009	Transistor Triac 2 Amps 100V	A03001
20-010	Transistor NPN 500 MA Code Driver	2N5845/2N5845/ 74659A
20-011	Transistor Photo	2N5777
20-012	Transistor PNP High Current Switch	2N2907/TS3413
20-013	Transistor NPN	2N3302
20-014	Transistor NPN	2N4238
20-015	Transistor PNP	2N4235
20-016	Transistor PNP	2N3740
20-017	Transistor NPN	2N3766
20-018	Transistor, Power Silicon NPN	2N3054
20-019	Transistor	2N6038
20-020	Transistor Switching 1 Amp T05 can	2N3725
20-021	Transistor NPN Silicon	MPS3646
20-022	Transistor NPN	2N1711
20-023	Transistor PNP	2N905A/J2N2905A
20-024	Transistor Switch	2N3776
20-025	PNP Hi Speed Switch	2N3467
20-026	Transistor Module, Quad	FSQ1079/FPQ3724
20-027	Transistor	2N2369
20-029	Transistor	
20-030	Transistor	HPX002
20-031	Transistor	2N3568
20-032	Transistor NPN	SEE 2N6486 SPEC
20-033	Transistor	KE4393
20-034	Transistor	2N3904
20-035	Transistor	2N3906
20-036	Transistor	MP54356
20-037	Transistor	D45H2
20-038	Transistor	2N2520
20-039	Transistor	2N222A
20-043	MOS FET	
21-025F01	1K ohm-15 to Common DIP	898 1-1K ohm (Beckman)
21-025F02	470 ohm-15 to Common DIP	898-1-470 ohm (Beckman)
21-025F03	330 ohm-15 to Common DIP	898-1-330 ohm (Beckman)
23-001	Diode High Speed-High Current	1N4150
23-002	Diode 5.1 V Zener	1N4733A
23-003	Diode 10V Zener	1N4750A
23-004	Diode 6.1 V Zener	1N4735A

23-007	Diode Mot Bridge	MDA962-2
23-008	Diode Int. Rectifier	40HF-5R
23-009	Diode	1N4735
23-010	Diode Int. Rectifier	S1Y1P
23-011	Diode Rectifier	2N681
23-012	Diode Thermistor	1D2032
23-013	Diode 9.3V	1N2163
23-014	Diode	1N3880
23-015	Diode	1N3889
23-016	Diode Bridge Rectifier	YS448
23-017	Diode	1N2070
23-018	Diode 13 V Zener	1N4746
23-019	Diode	1N3615
23-020	Diode 8.2V Zener	1N756A
23-021	Diode 9.1 V Zener	1N757A
23-022	Diode 3.3V Zener	1N746A
23-023	Diode Bridge Rectifier	KDH250
23-024	Diode, Power Fast Rec. 30 Amps	1N3909
23-025	Diode, Power Fast Rec. 3 Amps	MR841/A115A
23-026	Triac 600V 30 Amps	2N6162
23-027	Diac 32V	1N5761
23-028	Power SCR Thyristor	2N4441
23-029	Diode	1N4607
23-030	Diode	1N4156A
23-031	Diode 6.8 V Zener	1N4736A
23-032	Diode 9.1 V. Zener	1N4739
23-033	16 Diode Array	45190 (Litton)
23-034R01	Switch Diode 600 ma	TSC1N4607
23-035	Diode 40A	MBA4030
23-036	Diode	MPD-400
23-037	Zener Diode 2.4V	1N4370
23-041F00	Low Voltage Zener Diode	LVA51A40114/ LVA51A22819
23-041F02	Low Voltage Zener Diode	LVA62A40098/ LVA62A22941/LVA62A40212
23-042	Power Schottky	SD41
23-043F00	Zener Diode Avalanche 5.1V	
23-043F01	Zener Diode Avalanche 5.6V	
23-043F02	Zener Diode Avalanche 6.2V	
30-013F02	1.5uH inductor	Advanced Eng.)
30-013F03	2.2 uh inductor	
30-018	100 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
30-013	4.7uH Inductor	
30-019	50 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
33-032	Hexadecimal Switch	

CHAPTER 2
MODEL 5/16 INSTALLATION PROCEDURES

2.1 INTRODUCTION

The INTERDATA Model 5/16 Digital System features a highly modular structure which permits configurations to suit the user's exact needs. The Model 5/16 provides the means for convenient expansion as the user's requirements grow. This document describes the Processor and System Expansion Chassis, Power Supply Mounting, Filler and Turnkey Console Mounting, and the interconnecting cables. Printed circuit boards are discussed with respect to cabling and location only. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals. The following descriptions assume that the equipment is mounted in standard INTERDATA cabinets.

2.2 MECHANICAL COMPONENTS

This paragraph is intended to familiarize the reader with the mechanical components that are discussed in this document (i.e., Cabinet, Chassis Support Rails, and Filler Panels). Figures 2-1 through 2-4 provide the dimensions and mounting configurations for the Cabinet, Chassis Support Rails, and Filler/Display Panels. Figure 2-4 shows that the 5 1/4-, 7-, 8 3/4-, and 10 1/2-inch Filler Panels and the Display Panel mount in the same way (via retaining brackets), while the smaller 1 3/4-inch Filler Panel mounts with spring clips.

2.3 PROCESSOR AND EXPANSION CHASSIS MOUNTING

The Model 5/16 is available in an optional chassis which contains an integral Power Supply. In addition, a 7-inch Expansion Chassis is available for system expansion. The Expansion Chassis has the same overall dimensions as the Processor Chassis. The Processor Chassis has three slots available which can be used for mounting 7-inch or 15-inch peripheral controllers.

The Expansion or Processor Chassis slides into the rack on two chassis support rails (refer to Figures 2-2 and 2-3) from the front of the rack.

CAUTION

NO CHASSIS SHOULD BE MOUNTED IN CANTILEVER FASHION. CHASSIS SUPPORT RAILS MUST BE USED. IF A RACK CABINET OTHER THAN AN INTERDATA CABINET IS USED, CONSULT THE RACK MANUFACTURER FOR PROPER SUPPORT RAILS.

The chassis support rails are fastened to the mounting uprights at the front and rear of the rack. The Expansion or Processor Chassis is fastened in place, with screws, to the mounting uprights in front of the rack. All Expansion Chassis mount below the Processor Chassis. Expansion Chassis cabling is discussed in the next paragraph.

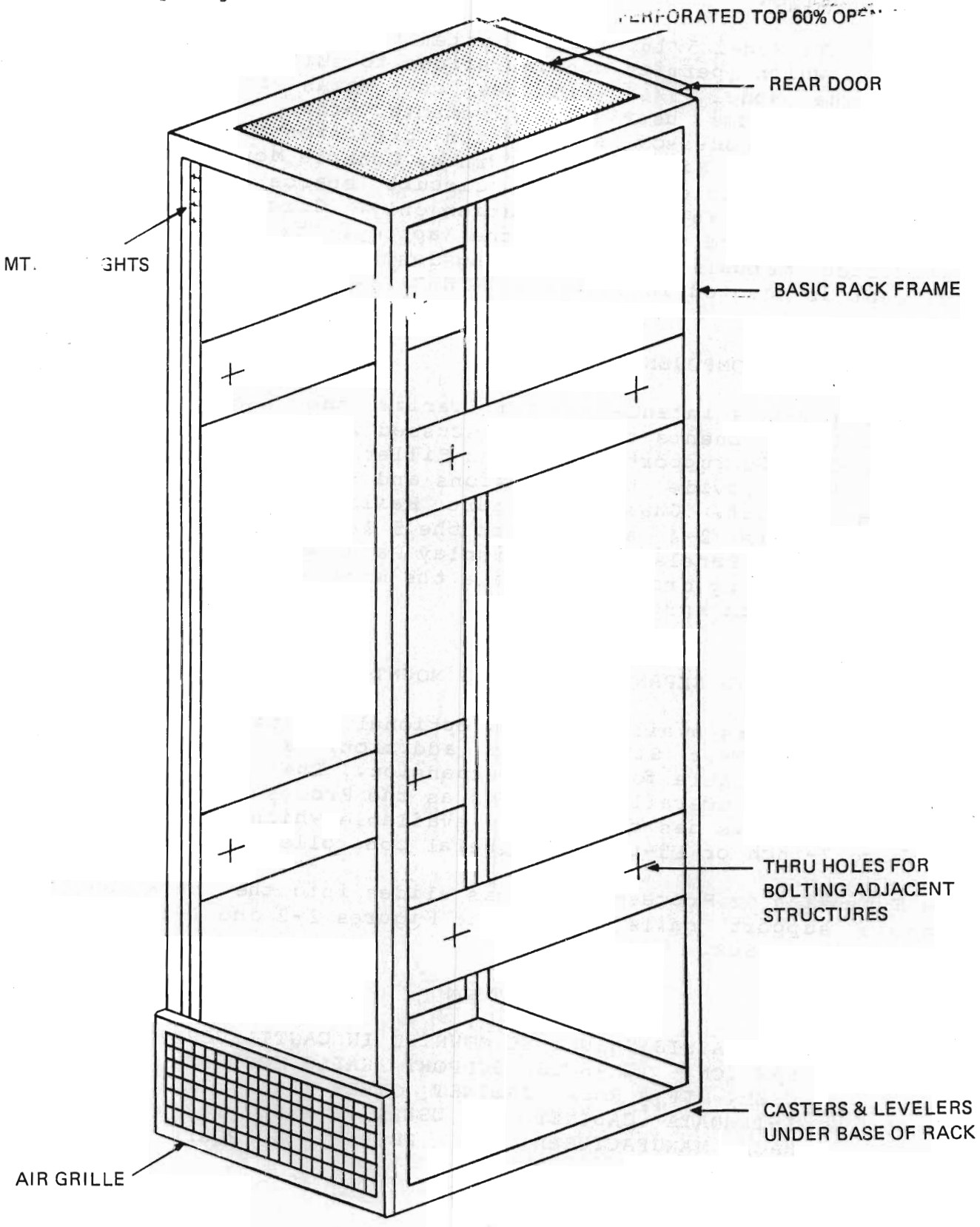


Figure 2-1. Basic Cabinet

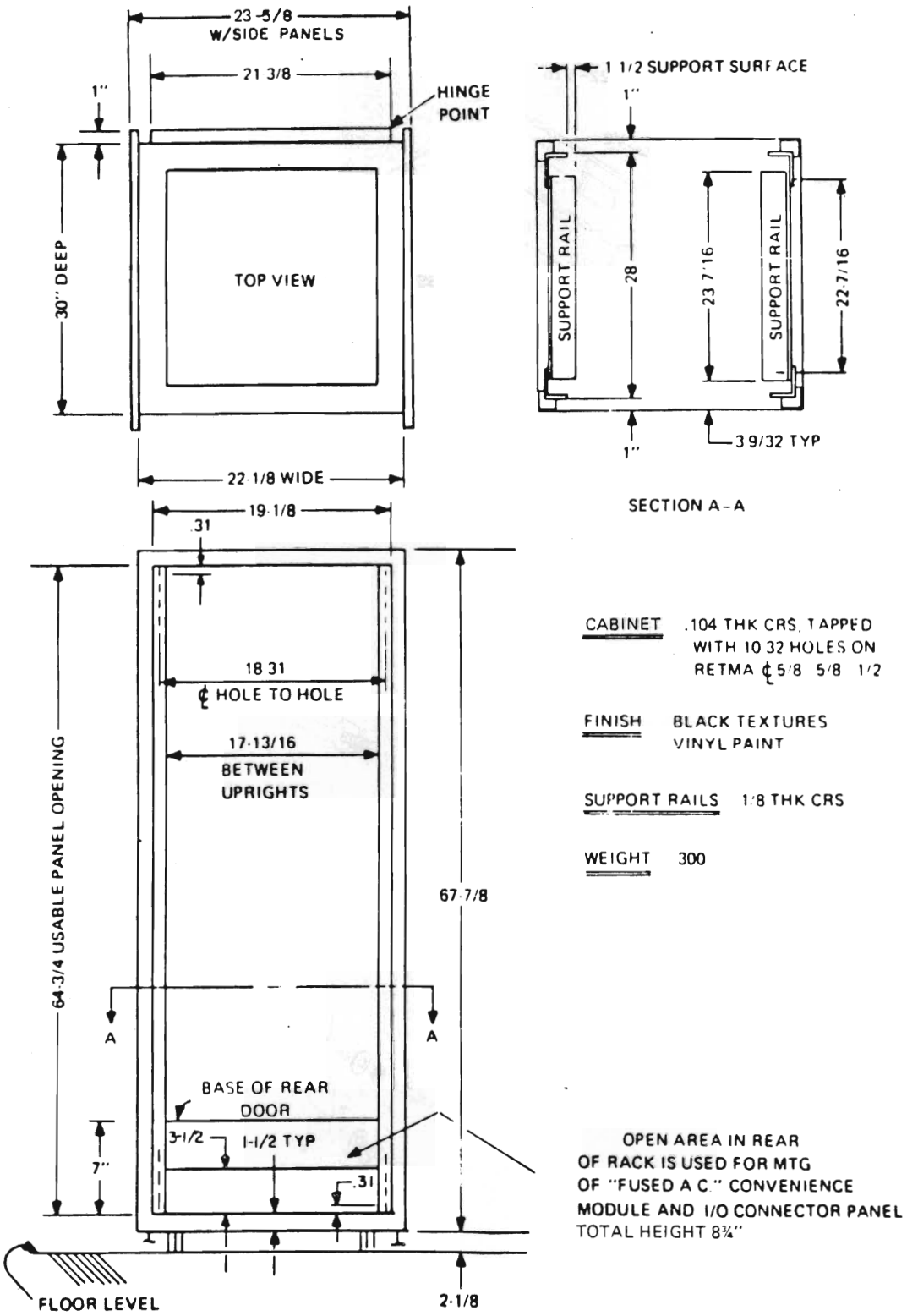


Figure 2-2. Basic Cabinet Physical Dimensions

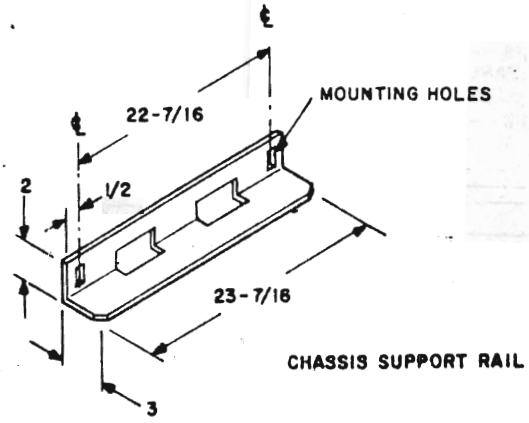


Figure 2-3. Chassis Support Rail

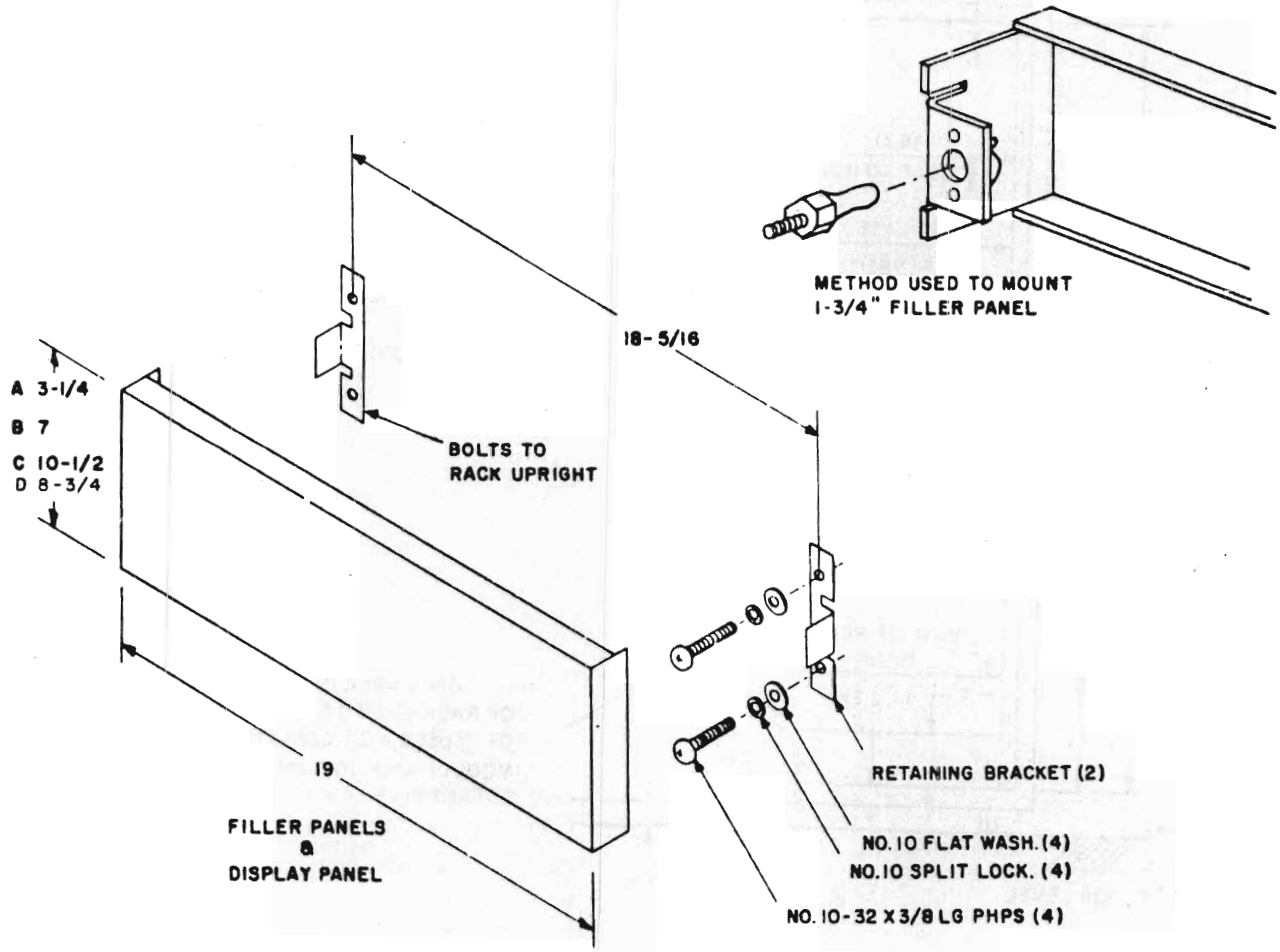


Figure 2-4. Typical Mounting Configuration for Display and Filler Panels

2.4 EXPANSION CHASSIS

The Expansion Chassis contains eight universal expansion slots which can accept combinations of single board peripheral controllers, system modules, or user-designed interfaces. Included with this 7-inch chassis are the cooling fans and interconnecting cables. The chassis may be ordered with or without a power supply.

Two 7-inch boards (half-boards) may be inserted into this chassis via the 16-398 Half-Board Adapter Kit (see Figure 2-5). The Half-Board Adapter Kit may hold two active 7-inch boards or one active and one blank 7-inch board, depending on requirements.

No wiring takes place between the boards and the adapters. The adapters are designed so that the connectors on the board plug directly into the Expansion Chassis.

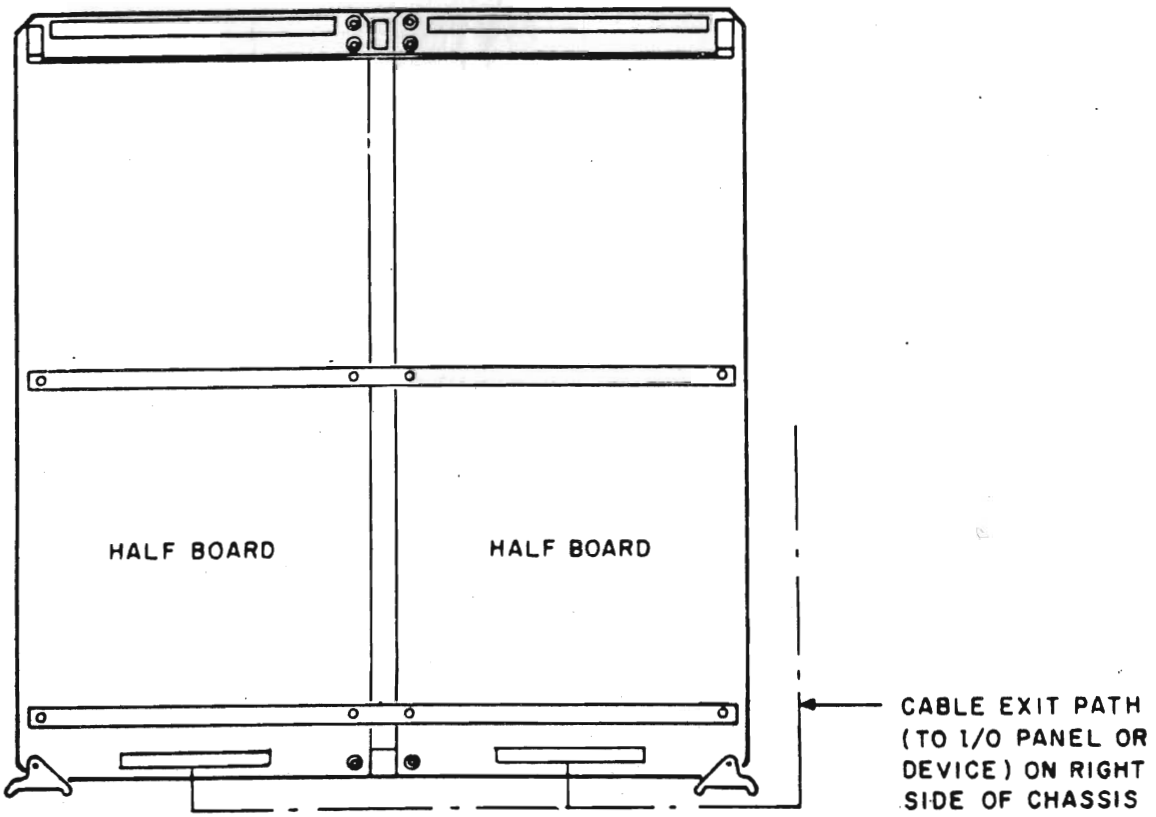
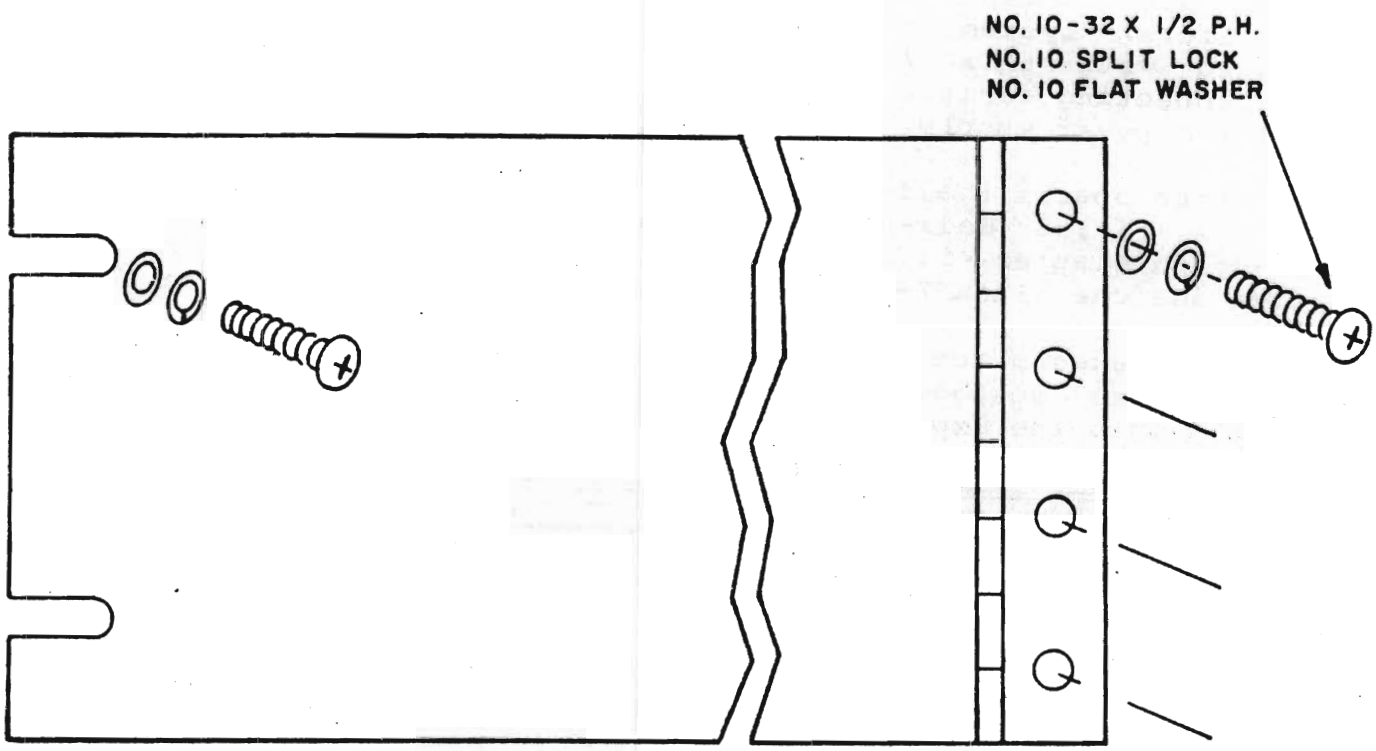


Figure 2-5. Half Board Adapter

2.5 EXPANSION POWER SUPPLY MOUNTING

The Expansion Power Supply mounts in the rear of the cabinet, behind the Processor and Expansion Chassis. It is attached to the right mounting upright (looking from the rear). One of three power supplies may be supplied with the Model 5/16 System.

These power supplies attach to the mounting upright via four 10-32 x 1/2 lg PHPS screws (refer to Figure 2-6).



When any power supply is in the installed operating position, it is secured to the left rear upright by two 10-32 screws. The power supply cable connects to terminal lugs at the right rear (looking from the rear) of its respective Processor or Expansion Chassis via Faston lugs and a connector for AC fan power.

There is adequate slack provided in the cable to allow the power supply to hinge out freely. In order to prevent the cable from being pinched between the power supply and Chassis Support Rails, a service loop is required. A maximum of five power supplies may be mounted in one rack.

WARNING

ALL AC FAN CONNECTORS ON POWER SUPPLIES WHICH ARE NOT CONNECTED TO MATING RECEPTACLES MUST REMAIN COVERED OR SHORTING MAY OCCUR.

Figure 2-6. Power Supply Mounting

The 115/230 volts fan switch on the chassis must be matched with the 115 volt or 230 volt strapping on the power supply (refer to Figure 2-7).

Exhaust fan plates are equipped with a switch to provide either 115 volt or 230 volt AC operation as shown in Figure 2-8.

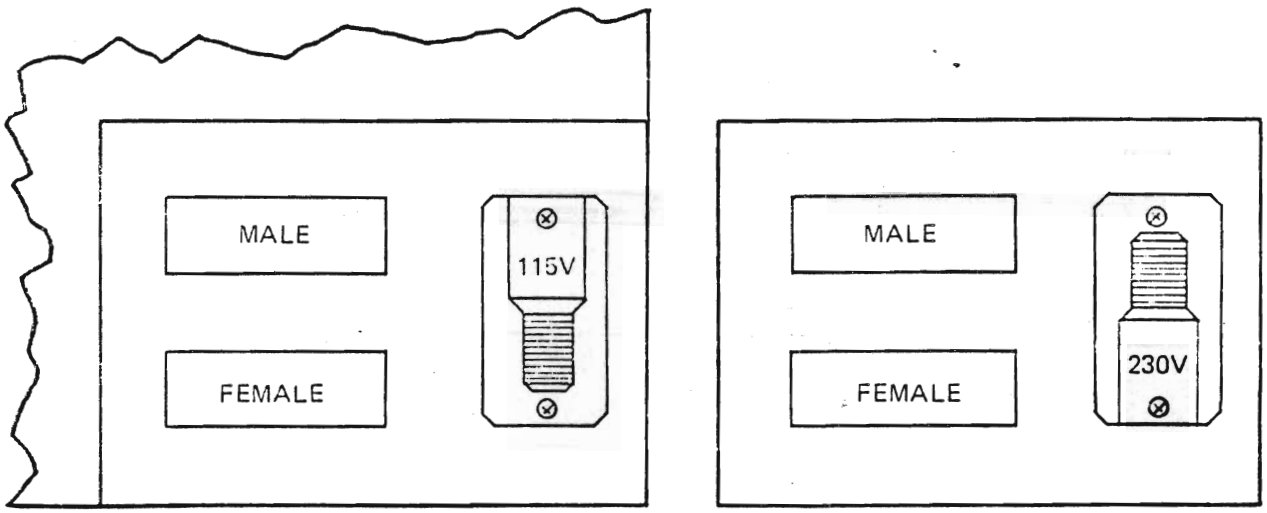


Figure 2-7. Fan Power Switch Match

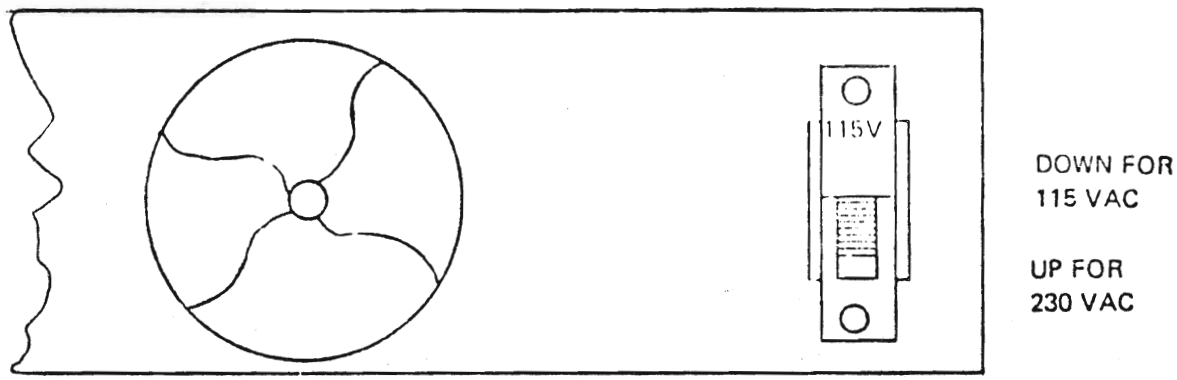


Figure 2-8. Exhaust Fan Switch Setting

2.6 TURNKEY CONSOLE PANEL INSTALLATION

The optional Turnkey Console is connected electrically to the system via ten Faston lugs. The Faston lugs are connected to the rear of the Processor Chassis. The terminal lugs are identified at the Faston Connector and are mated to their corresponding terminal pin (+L, LGND, C1, etc.) on the chassis (see Figure 2-9).

The Turnkey Console is physically mounted to the brackets provided on the Processor Chassis. A 1 3/4-inch filler panel may be mounted directly below the console on this same chassis (see Figure 2-10).

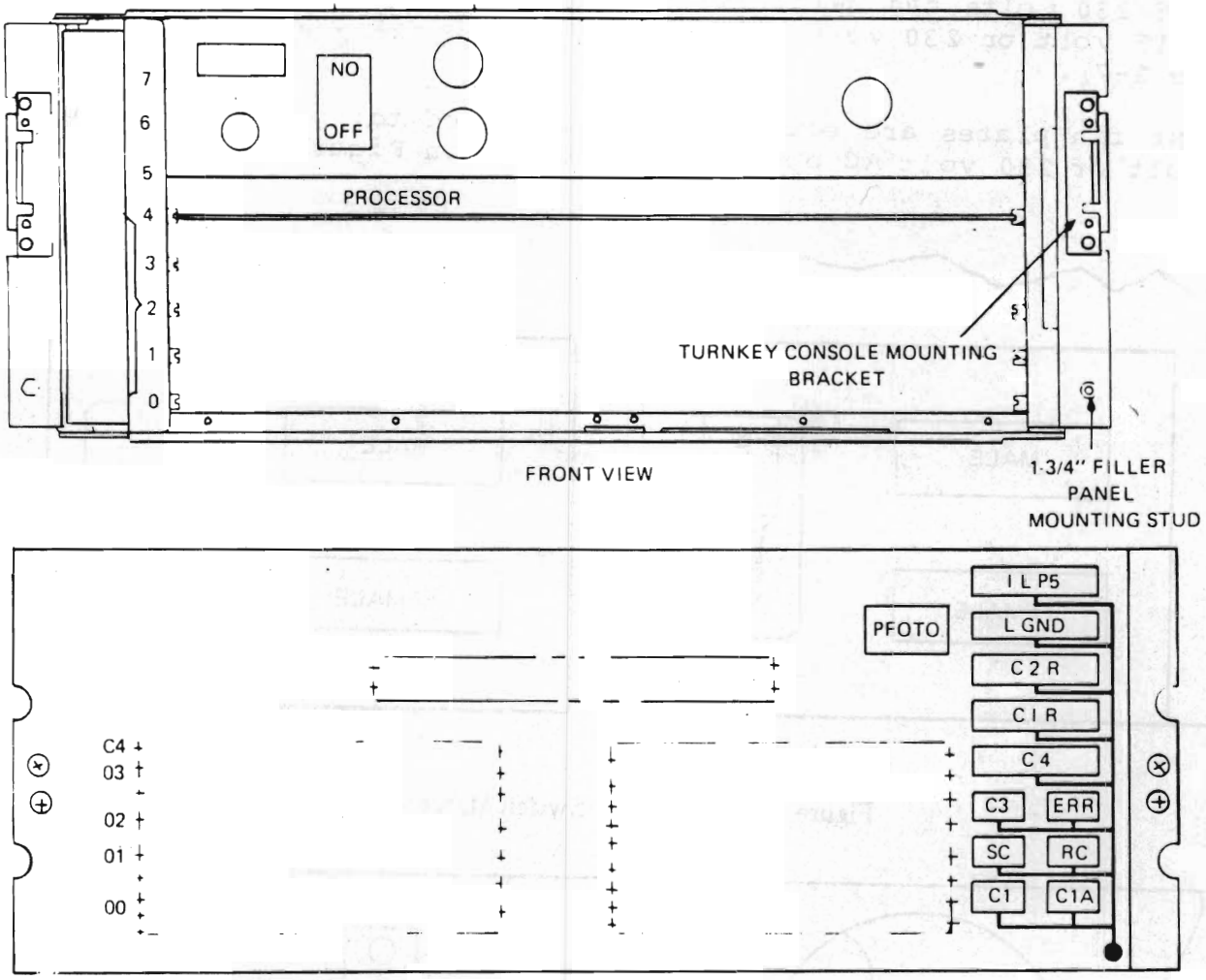


Figure 2-9. View of the Processor and Expansion Chassis

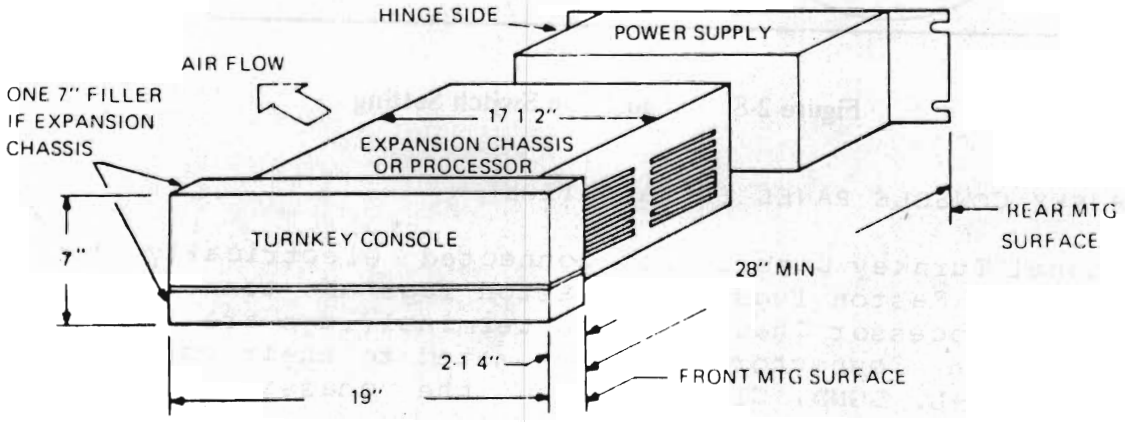


Figure 2-10. The Processor on Expansion Chassis

2.7 CONFIGURATION

2.7.1 System Expansion Chassis

When configuring a multi-chassis system, follow these rules:

1. Mount the system Expansion Chassis below the basic Processor Chassis.

2. Insure that no space is left between chassis.

2.7.2 Circuit Board Distribution

The Model 5/16 Digital System may be configured in a variety of ways. However, consider the following factors when determining circuit board distribution within the basic Processor and system Expansion Chassis.

1. All device addresses are hard-wired on the device controller cards (device addresses may be changed at option), so that the distribution of I/O device controllers in the chassis normally need be considered as a matter of priority in the RACK0/TACK0 "daisy-chain."

2. The interrupt priority of a given device controller is determined by its physical location on the serial RACK0/TACK0 line. Refer to Interrupt Priority Back Panel Wiring to determine which controller on the Multiplexor Bus has what priority. Devices that must be serviced in a certain amount of time, or loss of data access occurs, should be given a higher priority than a device with a high interrupt rate and no data loss, if not serviced.

The built-in serial port is hard-wired with the highest priority. Any devices on the Multiplexor Bus have the next lower priority, and devices on the Micro Bus have the lowest priorities.

2.7.3 Interrupt Priority Back Panel Wiring

The Acknowledge Control line from the Processor to the Multiplexor Bus carries the Interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with Interrupt Control circuits. Refer to Figure 2-11 to determine order of priority.

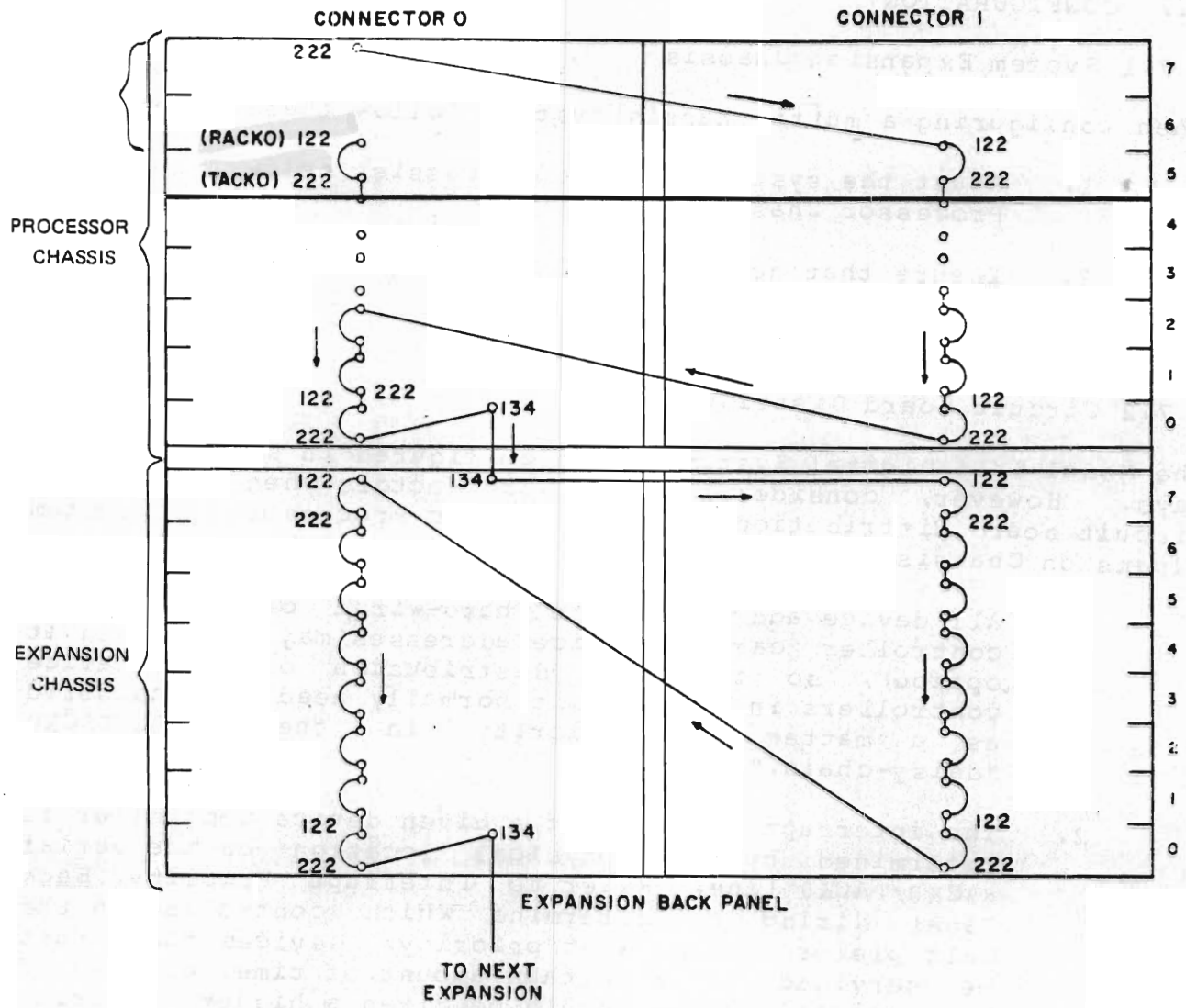


Figure 2-11. Standard Interrupt Priority

Back panel wiring for interrupt control at a given position is: The Received ACK (RACK0) at Pin 122-0 or 1 and the Transmitted ACK (TACK0) at Pin 222-1 or 0. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 or 0 of a given position to Terminal 122-1 or 0 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 or 0 and 222-1 or 0 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller that has an interrupt capability, the jumper from 122-1 or 0 and 222-1 or 0 must be removed from the back panel at that position.

Figure 2-11, showing the standard interrupt priority wiring, assumes a Model 5/16 Processor Chassis and one Expansion Chassis. The arrows indicate the direction of priority from the highest priority to the lowest. Slot 2 on Side 1 of the Processor panel has the highest priority. When Bus Buffers are installed, the standard interrupt priority must be modified. Refer to Figure 2-12, Interrupt Priority with Bus Buffer installed.

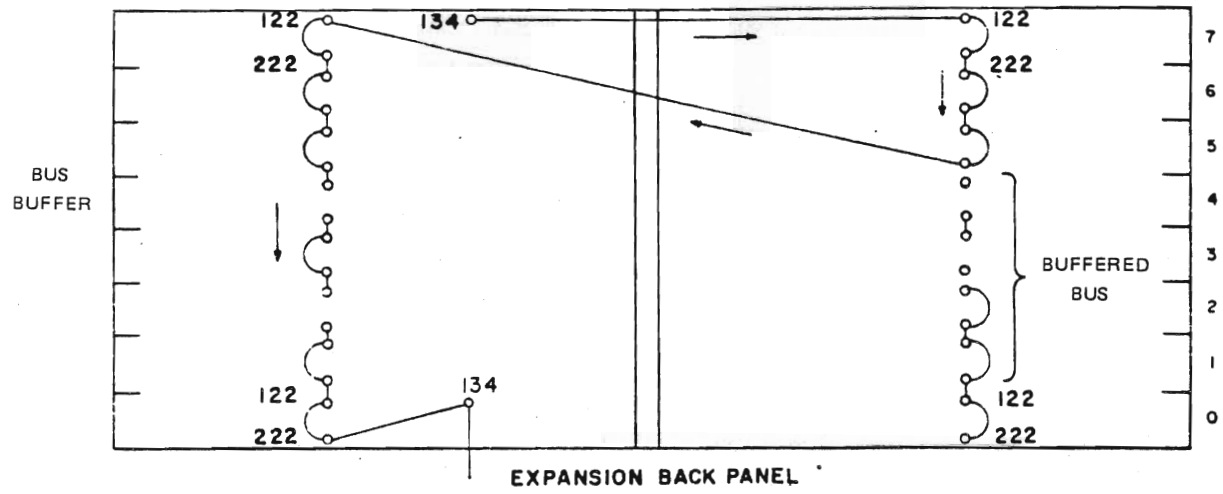


Figure 2-12. Interrupt Priority With Bus Buffer Installed

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices, see the appropriate installation specification.

The Micro-Bus priority is determined by position on the Micro Bus. Devices closest to the Processor have the highest priority.

2.7.4 Terminators

The termination end of both legs, Connector 0 and 1, of the Multiplexor Bus must have a standard INTERDATA termination card (35-433) installed. These cards are installed on the back panel at the lowest numbered slot of both connectors on the Multiplexor Bus that exists; e.g., if a bus buffer is installed in Slot 4 on the first expansion chassis and only the Processor Chassis and one Expansion Chassis is used in the system, the Multiplexor Bus must be terminated at Slot 0, Connector 0, and Slot 5, Connector 1 of the Expansion Chassis. In addition, the buffered bus should be terminated at Slot 0, Connector 1 of this chassis.

2.7.5 Processor Wire Wrap Information

Refer to Table 2-1 and schematic 35-637D08 for 5/16 Processor Wire Wrap information.

TABLE 2-1. WIRE WRAP INFORMATION

WIRE WRAP	RESULTING ACTION
AUTO RESTART (ROM) - A to C and B to D	ENTERS MEMORY ADDRESS X`FFFC' ON POWER UP
ALO (AUTOMATIC LOADER) - A to D and B to C	ENTERS THE AUTOMATIC BOOTLOADER ROUTINE ON POWER UP.
ASCII PROGRAMMER'S CONSOLE A TO C TO D	USER INSTRUCTION X`8800' IS TREATED AS AN ILLEGAL INSTRUCTION
ENABLE BREAKPOINT B TO E DISABLE BREAKPOINT A TO E	ENTERS ASCII CONSOLE ROUTINE ON POWER UP.

2.8 CABLES

2.8.1 Power Cable

The standard INTERDATA Cabinet is wired for 30 Ampere service. On the main power cable (part of the AC Distribution Panel), there is a 3-wire, twist lock, grounding, 125VAC, 30 Ampere, UL, (Hubbel No. 2610) plug. A 3-wire grounding, 30 Ampere, 125 VAC receptacle (Hubbel No. 2611 or equivalent) is required to accept this plug.

2.8.2 System Expansion Cable

A number of standard cables are available for configuring systems made up of an INTERDATA Expansion Chassis. The choice of cables depends upon system configuration. The following cables are available:

1. 17-193: I/O Expansion Cable, Connector "0"

   This cable is used to connect the "0" connector field between two adjacent 15-inch card files.

2. 17-194: I/O Expansion Cable (see note)

   This cable is used to connect the "1" connector I/O fields between two adjacent 15-inch card files.

3. 17-216: I/O Expansion Cable, 36 Inch Long

   This cable is used to connect two 15-inch files that are not adjacent. It must not be used to extend the basic Processor Multiplexor Bus.

It can be used to extend a buffered bus. It plugs into a "1" side connector. The "receiving" end can plug into the "0" or "1" side of the expansion file.

4. 17-183: "0" to "1" Connector

This cable can be used to interconnect the I/O Multiplexor Bus of the "0" field and the "1" field within a 15-inch card file.

There is no RACK0/TACK0 wire in this cable.

It can also be used to connect a "0" side (Slot 0) of a file, to the "1" side (Slot 7) of the next adjacent file, or vice versa.

NOTE

A strap is installed at the factory on the receive end of a 17-327 cable. This strap must be removed unless the cable is being used to jumper a private I/O Bus. This strap jumpers Pin 222-0001 of the upper chassis to Pin 122-0701 of the first expansion chassis. If these cables are used to extend a Bus Buffer the following wiring changes are required on the lower chassis.

Remove the strap from Pin 134-0700 to Pin 122-0701

Add a strap from Pin 134-0700 to Pin 122-0700

2.9 CONFIGURATION RULES

1. A maximum of 16 device controllers may be installed on the Multiplexor Bus or Micro I/O Bus of the Model 5/16. This assumes all drivers in the system are capable of sinking 48 milliamps or more and no more than one TTL Load (2 milliamps max.) on any Control Line or Data Line on the device controllers.

2. The Multiplexor Bus must be contained within the Processor Chassis and two adjacent 7-inch Expansion Chassis. The Multiplexor Bus must be buffered by a Bus Buffer or the equivalent for systems which require the Multiplexor Bus to be extended beyond these limits or in the case where the Bus must be extended by any 36-inch cable.

2.10 INSTALLATION OF OPTIONS

2.10.1 Test Aid Option

This paragraph provides the information necessary to install the M49-410 Test Aid on the processor.

1. Remove the display from the chassis.

2. Place Test Aid logic card over the pins on the Processor (CPU) board (Figure 2-13) and press down until Test Aid logic card rests on spacers on the processor board. The switch/display panel assembly may be placed on a table or mounted on the chassis as shown in Figure 2-14.

2.10.2 Boot Strap Loader (ALO) Option

The Boot Strap Loader Read Only Memory (ROM) device is installed on the 5/16 CPU board, 35-637, in the 24-Pin I.C. socket in location A124. This location excepts either a 1Kx8-bit or a 2Kx8-bit ROM If two 1Kx8-bit ROMs are used, the second ROM device is installed in location A115. Refer to Paragraph 2.7.5 for Processor wire wrap information and to Appendix 4 for the listing of the standard OS Bootstrap ROM.

2.10.3 RAM, ROM, and Micro-bus Options

These options are mounted to the bottom of the CPU board in a mother-daughter board fashion. Refer to 01-100 B12, Information Drawing, for physical locations and mounting hardware.

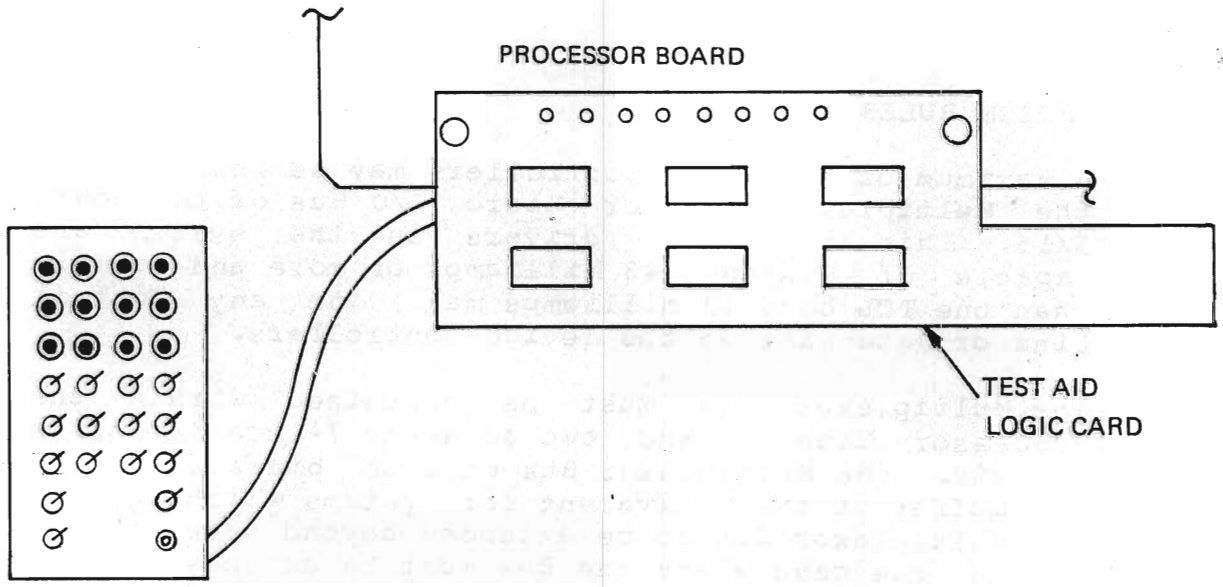


Figure 2-13. Test Aid Installation

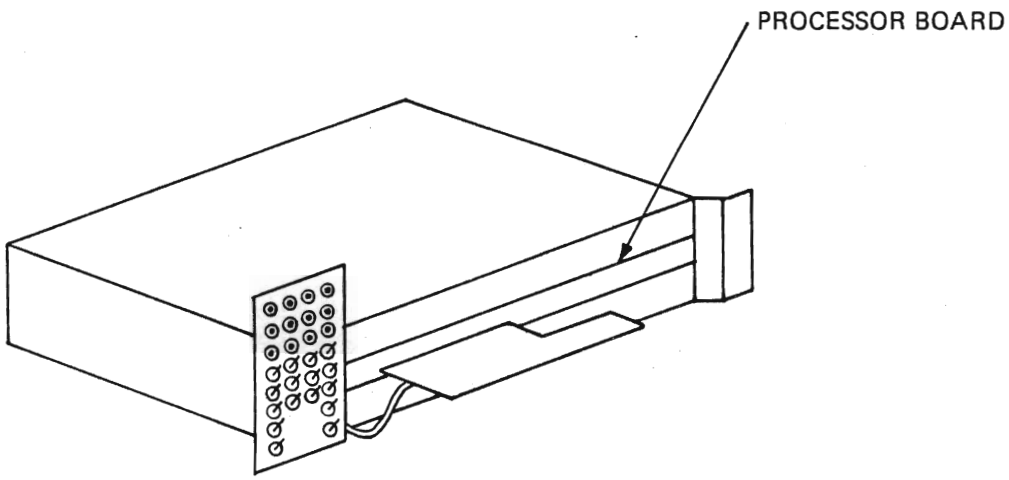


Figure 2-14. Switch Panel Mounting

CHAPTER 3
MODEL 5/16 MAINTENANCE INFORMATION

3.1 INTRODUCTION

The Model 5/16 Processor is a low-cost, 16-bit, general-purpose minicomputer. The latest MSI and LSI integrated circuit technology is used to construct a processor suitable for use in data communications, process control, or stand-alone scientific computer applications. The Model 5/16 Processor is modularly constructed for ease of maintenance and is compatible with the INTERDATA product line.

3.2 SCOPE

This chapter describes the functional operation of the Model 5/16 Processor and provides maintenance information useful to digital technicians maintaining this processor. A block diagram analysis, a micro-program description, and a functional analysis of major processor areas are included.

3.3 BLOCK DIAGRAM ANALYSIS

The following paragraphs refer to Figure 3-1.

3.3.1 System Organization

The Model 5/16 Processor is organized between two 16-bit busses. The B bus is the source for memory address and data and is one input to the Arithmetic Logic Unit (ALU). The S bus, which receives the ALU output, is the data source of the input/output bus and for the machine registers. The source and destination of data on the B bus and S bus, as well as the function performed by the ALU, are controlled by micro-instructions contained in the Read Only Memory (ROM).

3.3.2 Read Only Memory

The Read Only Memory (ROM) is a high speed, solid state, nondestructive memory organized into two pages of 512 words each. Each word in the ROM is 24 bits long and represents one micro-instruction.

Each micro-instruction readout of the ROM is latched in the 24-bit ROM Data Register (RD). The RD is the instruction register for the microprocessor. RD bits are decoded to select a source register and an ALU function. The ALU forms a result that becomes available some time before the end of the machine cycle. The result is then loaded into the appropriate destination register and the next micro-instruction is fetched.

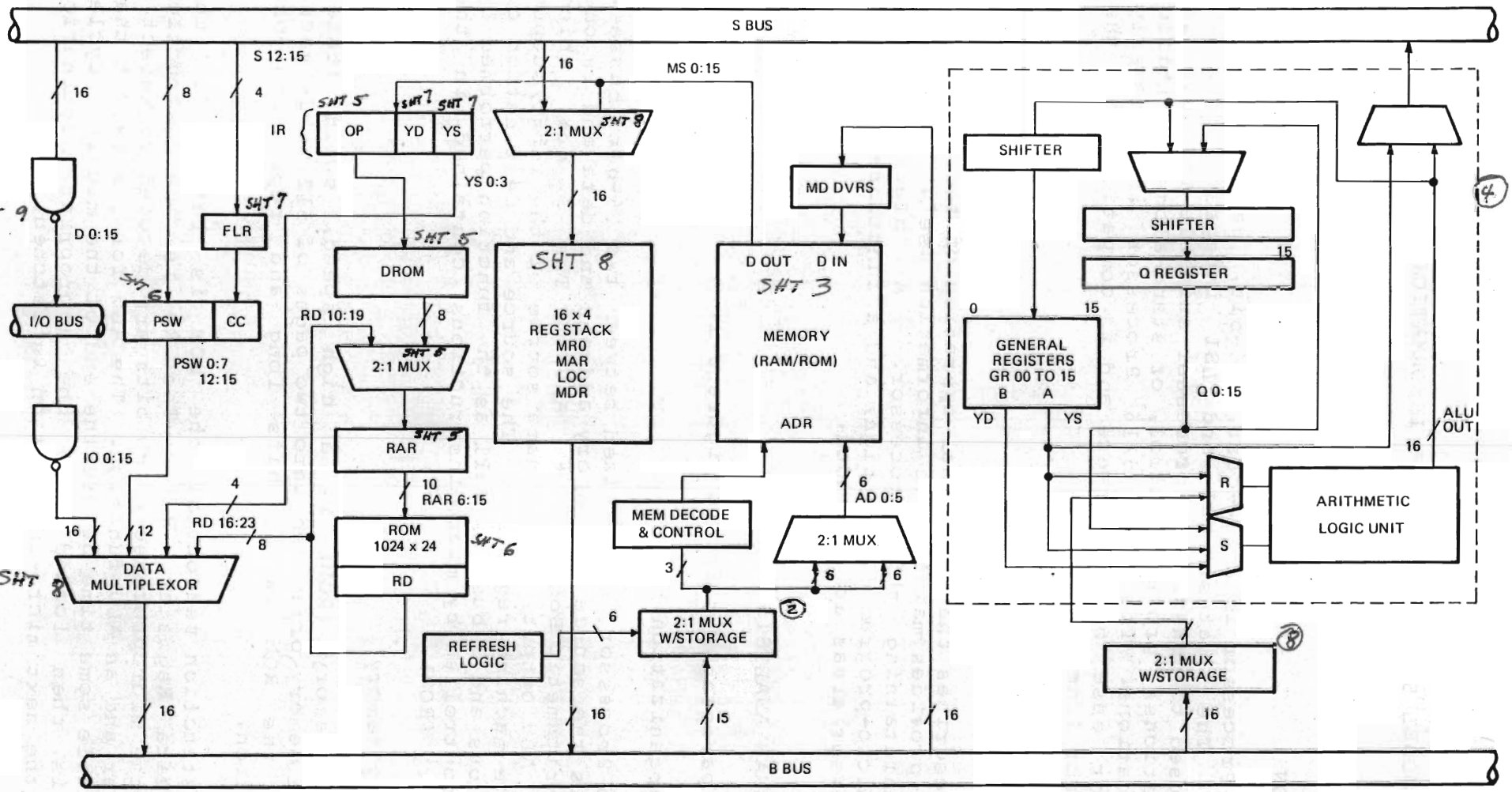


Figure 3-1. 5/16 Block Diagram

Locations in the ROM are addressed by the 10-bit ROM Address Register (RAR). Micro-instructions are normally executed from sequential addresses in the ROM. The RAR is an up-counter, incrementing by one as each new micro-instruction is read from the ROM. When it becomes necessary to jump out of sequence, the RAR can be loaded with a new address from the RD register or from one of the decoder read only memories, or it can be preset by the hardware.

3.3.3 Flag Register

The Flag Register (FLR) is a 4-bit register containing the following flags: Carry (C), Overflow (V), Greater than zero (G), and Less than zero (L). These flags are modified at the conclusion of a micro-instruction that allows flag register update to reflect the ALU output. At the beginning of a user instruction emulation sequence, the flag register is automatically cleared.

The flag register is loaded from bits 12 through 15 of the S bus when either the FLR or the Program Status Word (PSW) is the specified destination register.

3.3.4 Program Status Word

The Program Status Word (PSW) is a 16-bit register used to indicate the system status relative to the user program being emulated. Bits 0 through 11 of the PSW define enabled interrupts and the operational status or mode of the user level processor. Some of the PSW bits have hardware significance while others are of significance only to the microprogram. Bits 12 through 15 of the PSW make up the Condition Code (CC) which reflects the result of the most recent user level instruction.

Note that PSW bits 8 through 11 are not implemented. The Condition Code field may only be updated from the FLR. When the PSW is the specified destination, bits 0 through 7 of the S bus are loaded into bits 0 through 7 of the PSW. S bus bits 12 through 15 are captured in the FLR. At the conclusion of the next sequential micro-instruction, the contents of the flag register are copied into the Condition Code. Condition Code update from the flag register and subsequent clearing of the flag register also occurs when the microprogram initiates a user level instruction read.

3.3.5 Main Memory

The main memory is the source of user level instructions and data. It consists of solid-state, dynamic, Random-Access Memory (RAM) devices. The basic 5/16 Processor can have 8KB of RAM, optionally expandable to a maximum of 65KB. Memory is accessible to the halfword (16-bit) level only. Selection of a particular byte within a halfword is done externally to the memory by the microcode.

Because of the nature of the main memory devices, the microcode must periodically issue a refresh command to the memory. If this is not done, data decays to some quiescent state.

Main memory operations are discussed later.

3.3.6 Instruction Register

The Instruction Register (IR) holds the most significant 16 bits of the user level instruction currently being emulated. The IR may only be loaded from the main memory output. This register is divided into three fields. Bits 0 through 7 (OP) contain the user's operation code. Bits 8 through 11 (YD) specify the first operand register or a mask value for branching.

Bits 12 through 15 (YS) specify the second-operand, General Register or memory-reference, instruction-index register.

3.3.7 Decoder Read Only Memory

The Decoder Read Only Memories, DROM1 and DROM2, each contain 256 8-bit words. The microprogram can interrogate either of the DROMs at any time other than on a Branch micro-instruction or a memory operation. The DROMs are addressed by the operation code field of IR.

The data read from the DROM is jammed into the least significant eight bits of the RAR. The most significant two RAR bits remain unchanged. The result is a branch to an address in the current page of the ROM unique to the user's operation code.

3.3.8 General Registers

The general-register stack contains sixteen 16-bit registers. It is most often the case that the microprogram accesses the general registers without caring which one of the 16-registers it gets. Consequently, no provision has been made for the microprogram to randomly access an explicit general register. When emulating a user level instruction, the microcode only needs to access the registers specified in the user's instruction. Since the register addresses specified by the user are in the instruction-register fields labeled YD and YS, the microprogram can access the intended registers by specifying the YD or YS field. The hardware then selects the general register whose number is in the YD or YS field.

The YD field is implemented as an up/down counter so that sequential registers may be accessed. The YD field may also be cleared by the microprogram when it is necessary to access specific general registers.

3.3.9 Micro Registers

The four 16-bit micro registers labeled MR0, MAR, LOC and MDR are available to the microprogram for general use. None of these registers has any actual hardware significance. They are given

significance by the role they play in the emulation process resulting in the mnemonic designations.

3.3.10 Q Register

The Q Register is a 16-bit general purpose arithmetic or logical accumulator. It may participate as an operand to the Arithmetic Logic Unit (ALU) or it may be shifted left or right. The ALU output may be shifted left or right and then copied to the Q register or one of the general registers.

The Q Register and any of the sixteen general registers can be linked together to emulate the 32-bit shift and rotate instructions.

3.3.11 Arithmetic Logic Unit (ALU)

The ALU comprises a 16-bit parallel adder/subtractor and logical connect network with look ahead carry. Micro-instruction word bits are decoded to select the R and S gate inputs to the ALU and to select the function performed by the ALU.

The following ALU functions are provided:

R Plus S
R Minus S
S Minus R
R Or S
R And S
R Not And S
R Exclusive Or S
R Exclusive Nor S

3.3.12 Input/Output

Input/output operations can occur over the INTERDATA multiplexor bus or over the micro I/O bus interface. These external bus schemes represent the two ports available to the internal I/O pictured on the block diagram.

All I/O operations are initiated and controlled by the microprogram. Each operation is performed on a request/response basis using a bi-directional data bus and a number of control lines to identify the nature of the bus data.

3.4 MICRO-PROGRAM DESCRIPTION

The Model 5/16 Processor is designed to execute micro-instructions stored in a Read-Only Memory (ROM). Each micro-instruction causes one or more hardware functions to be performed. A micro-instruction can transfer the contents of one register to another, perform arithmetic or logical operations between registers, control input/output operations, or initiate main memory accesses.

A series of micro-instructions is called a microprogram. The complete Model 5/16 microprogram is, by definition, an emulator. It causes the Model 5/16 hardware to react to a user program in main memory and to external events as would the Processor described in the Model 5/16 User's Reference Manual, Publication Number 29-588. Every user level instruction, interrupt handling feature, and ASCII control console function is simulated in the Model 5/16 microprogram.

When executing instructions of the user level machine, the microprogram first presents the contents of the user's location counter to main memory as an address, and issues an instruction read command. The location counter is incremented by two and the hardware forces the machine to a fixed address in the ROM. It is from this point that the emulation sequence for every user level instruction begins.

When the user's instruction becomes available at the main memory output (access time), it is automatically copied into a special user level instruction register. The microprogram tests for machine interrupts such as I/O attention, DMA requests, or console stop. If none are pending, the general register specified by the R2/X2 field of the user's instruction is copied into the micro register MR0. The content of this register is used as the user level second operand (R2), if the instruction happens to be a Register-to-Register format. If the user's instruction is Register-to-Indexed Storage (RX) or Register Immediate (RI) format, MR0 contains the index register value (X2).

The microprogram now interrogates the first of two special Decoder Read Only Memories (DROMs). The address input to each DROM is the user level operation code. Consequently, the output of the DROM is unique to the particular operation code. In general, if the user's instruction is a Register-to-Register format, the first DROM output is the starting address of the appropriate instruction execution microcode sequence. If the user's instruction is not a Register-to-Register format, then the first DROM output is the address of the microcode sequence that fetches the rest of the user level instruction from main memory, increments the location counter again, performs indexing if specified, and sets up MR0 with the effective second operand. This sequence is terminated when the microprogram interrogates the second DROM, to obtain the starting address of the appropriate instruction execution sequence.

The instruction execution sequence consists of two or more micro-instructions as required to complete simulation of the particular user's instruction. Each instruction execution sequence is responsible for initiating the instruction Read for the next user level instruction. When this has been done, the loop is closed and the microprogram is back at the common emulation start address.

3.5 DATA AND INSTRUCTION FORMATS

3.5.1 Data Formats

All internal data paths are 16 bits wide. Hence the basic machine operand is a 16-bit halfword. In arithmetic operations, the most significant bit is interpreted as the sign bit of the number in the least significant 15 bits of a halfword. Positive fixed-point data is expressed in true binary form with a sign bit of zero. Negative fixed-point data is expressed in two's complement notation with a sign bit of one.

Binary information is represented in hexadecimal notation, base 16, for simplicity.

3.5.2 INSTRUCTION FORMATS

Model 5/16 micro-instructions can occur in one of three general formats designated Branch, Register-to-Register, and Register Immediate. The instruction formats are shown in Figure 3-2. The meaning of the micro-instruction fields is summarized in Table 3-1 and in the following paragraphs.

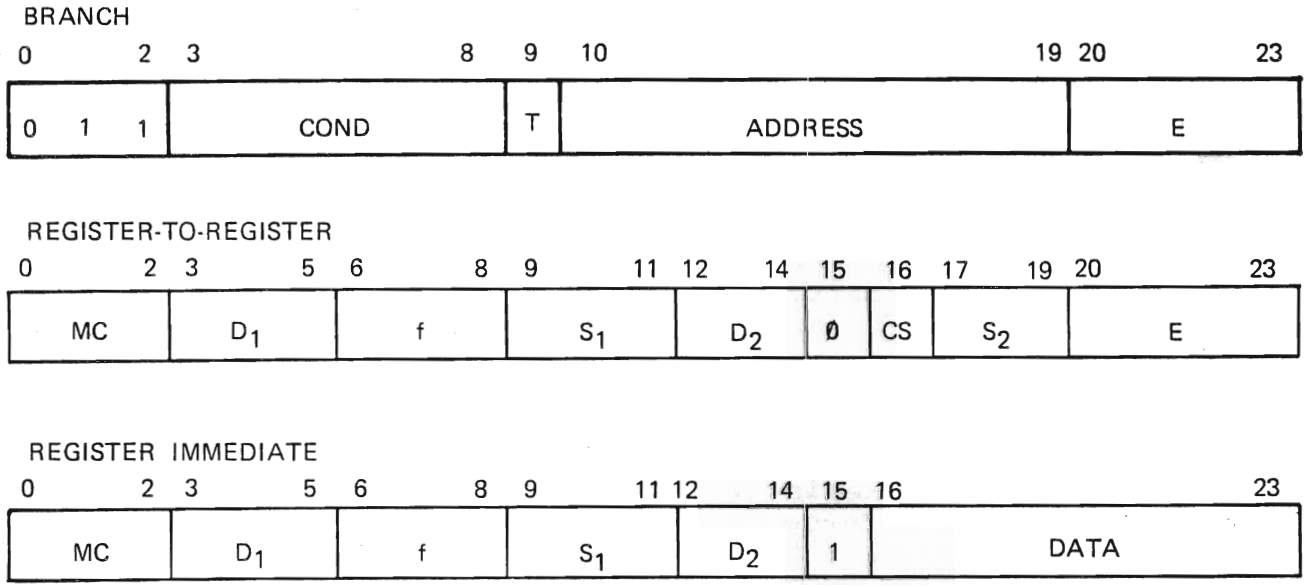


Figure 3-2 Instruction Word Formats

The Branch format is indicated by the 011 combination in bits 0 through 2 of the instruction. When these bits do not equal 011, an instruction format other than Branch is implied and these bits comprise the MC (Memory Control) field.

The MC field specifies a memory action (memory read, memory write, or instruction read) or it causes one of the DROMs to be interrogated.

On a Branch format, the COND field specifies the machine condition that is tested. The T bit then selects whether the true or false state of the condition or conditions is to be taken. If the Branch condition is met, the value of the ADDRESS field is copied into the ROM Address Register (RAR).

TABLE 3-1. MICROINSTRUCTION WORD FIELDS

FIELD	MEANING
MC	Memory Control
COND	Branch Condition
T	Branch on True/Branch on False Condition
ADDRESS	Branch address if condition met
E	Extended option field
D	*Internal Destination field
D	S Bus (External) Destination field
f	ALU Function Select
S	*Internal Source Selection
S	B Bus (External) Source Selection
CS	Cross Shift option (8 place rotate)
DATA	Immediate B Bus Data

* Bracketed area on Block Diagram (Micro-Controller).

The E field for Branch micro-instructions specifies additional functions to be performed. Typical E field options for Branch might clear the YD field of IR, increment or decrement the YD field of IR, or initiate a memory refresh cycle.

For Register-to-Register instructions, the E field may also specify arithmetic or shifted carry in or out, or both. It can specify that the Flag Register (FLR) be updated to reflect the S bus data. It can force a carry in situation to the ALU for increment and decrement functions, or it can be used to conditionally load the S bus destination registers. When the source or destination is I/O, the E field specifies the particular I/O operation.

The CS (Cross Shift) bit controls the B bus shifter latch. When a cross shift occurs, the two 8-bit bytes of the B bus are exchanged and then latched. This feature is useful for byte processing.

The S field selects the R and S gating into the ALU. Refer to Figure 3-1. The possible ALU inputs are:

1. The general register specified by the YD field of IR

2. The general register specified by the YS field of IR

3. The Q register

4. Zeroes (NULL)

5. The B bus shifter/latch

When the output of the B-bus shifter/latch is an ALU input, the source of the B-bus data is specified by the S field in the Register-to-Register format. In the Register Immediate format, the B-bus data comes from bits 16 through 23 (DATA) of the micro-instruction word. The f field selects the ALU function to be performed.

The D field determines what is to become of the ALU output. The ALU output can be gated out to the S bus. It can be shifted left or right one position and then copied into a general register or the Q register. The ALU output can be shifted and copied to a general register while the Q register shifts in the same direction. The ALU output can be copied to a general register while the S bus gets the contents of the general register specified by the YS field of IR. The ALU output can even be discarded.

The D field selects a destination register for S bus data or memory data.

3.6 MAIN MEMORY OPERATIONS

When the microprogram initiates a memory read, memory write, or instruction read, the data currently on the B bus is taken as the memory address. The micro-instruction that starts a memory operation must place the desired memory address on the B bus. That address may come from one of the registers MR0, MAR, LOC, or MDR, or from the least significant eight bits of the micro-instruction word itself for immediate instructions.

The micro-instruction that initiates a memory read command must be followed immediately by a micro-instruction whose destination is one of the registers MR0, MAR, LOC, or MDR. The specified register receives the memory data output regardless of S bus activity.

It takes two micro-instructions to do a memory read.

The micro-instruction that initiates a memory write command must be followed immediately by a micro-instruction that places the data to be written on the B bus. That data may come from one of the registers PSW, MR0, MAR, LOC, or MDR, or from the least significant eight bits of the micro-instruction in the case of Immediate instructions.

It takes two micro-instructions to do a memory write.

After issuing an instruction read command, the hardware automatically clears the ROM Address Register (RAR). The next micro-instruction performed is at address `000' in the ROM. During that micro-instruction, when memory data becomes available, it is automatically copied into the Instruction Register (IR).

3.7 SOURCE AND DESTINATION REGISTERS

3.7.1 Source Registers

Source and destination registers are available to any micro-instruction other than Branch. The S field of a micro-instruction selects the R and S inputs to the ALU. In general, the R input represents the first operand and the S input is the second operand. On the subtract micro-instruction, these roles are allowed to be swapped.

The valid R and S combinations are summarized in Table 3-2. When the B bus is an ALU input, the B-bus data comes from the micro-instruction word itself (Immediate) or the data source is selected from the S field.

TABLE 3-2. R AND S INPUTS TO THE ALU

RD BITS			SYMBOLIC REGISTER		COMMENTS
9	10	11	R	S	
0	0	0	YS	Q	YS = Register specified by YS field
0	0	1	YS	YD	YD = Register specified by YD field
0	1	0	NULL	Q	Q = Q register
0	1	1	NULL	YD	NULL = Constant of zeros
1	0	0	NULL	YS	Unused combination
1	0	1	B Bus	YD or X2	X2 causes YS to be selected
1	1	0	B Bus	Q	On last three combinations, B-bus data is an ALU input operand
1	1	1	B Bus	NULL	

Table 3-3 summarizes the B-bus source registers. The source registers may be used freely by the microprogram. The following paragraphs point out special considerations.

On arithmetic and logical micro-operations, the Assembler expects the two ALU operands to appear in order, first operand specified first, then the second operand. Except for subtract, the first operand must be one of the R registers and the second operand must be one of the S registers. See Table 3-2.

TABLE 3-3. B BUS SOURCE REGISTERS (S_2)

RD BITS 17	18	19	SYMBOLIC REGISTER	COMMENTS
0	0	0	-	Source is I/O
0	0	1	PSW	Program Status Word
0	1	0	YSI	YS field is copied to B bus bits 12:15
0	1	1	MEM	Use memory data output
1	0	0	MR0	Micro Register 0
1	0	1	MAR	Memory Address Register
1	1	0	LOC	User's location counter
1	1	1	MDR	Memory Data Register

The user's 16 general registers do not have individual source addresses. Instead, the common symbolic names YD, YS and X2 cause the actual general register address to be taken from the YD or YS field of the user's Instruction Register (IR).

When a micro-instruction specifies YD as a source, the general register, whose number is in the YD field of IR, is selected. When a micro-instruction specifies YS or X2 as a source, the general register specified by the YS field is selected.

When the B bus source is I/O, an input operation is performed. The nature of the input request is encoded in the extended field of the instruction.

Specifying MEM as a B bus source is only valid after a memory read operation and implies that the S bus destination register receives the memory data. If the previous micro-instruction specified memory read, the S bus destination register is loaded with the memory output data regardless of other S bus activity. If the previous micro-instruction did not specify memory read, the destination register is undefined.

3.7.2 Destination Registers

Destination registers are available to any micro-instruction other than a branch. The D field tells what processing is to occur to the ALU output. Table 3-4 summarizes the (D_1) field combinations.

TABLE 3-4. INTERNAL DESTINATION FIELD D_1

RD BITS 3	4	5	SYMBOLIC REGISTER	COMMENTS
0	0	0	Q	S bus selection also available
0	0	1	NULL	S bus selection also available
0	1	0	YDA	YD gets ALU output, S bus gets YS
0	1	1	YD or YS	Load register specified by YD or YS
1	0	0	YD&Q	Only applicable on Shift Right
1	0	1	YD	Only applicable on Shift Right
1	1	0	YD&Q	Only applicable on Shift Left
1	1	1	YD	Only applicable on Shift Left

When the D_2 field combination equals 0, 1, or 2, an S bus selection may also be made. For all other combinations, the Assembler sets the D_2 bus selection field to NULL. Table 3-5 summarizes the D_2 field combinations. When interpreting the destination specification, the Assembler fills in both the D_1 and (D_2) fields as shown in Table 3-6.

TABLE 3-5. S BUS (EXTERNAL) DESTINATION FIELD (D)

RD BITS 12	13	14	SYMBOLIC REGISTER	COMMENTS
0	0	0	-	Destination is I/O
0	0	1	PSW	Program Status Word
0	1	0	FLR	Flag Register
0	1	1	NULL	S bus data is lost
0	1	1	MEM	Only valid after memory write
1	0	0	MR0	Micro Register 0
1	0	1	MAR	Memory Address Register
1	1	0	LOC	Location Counter
1	1	1	MDR	Memory Data Register

Destination registers may be used freely by the microprogram noting the following special cases.

When the PSW is loaded, bits 12 through 15 of the S bus are captured in the FLR. At the end of the next micro-instruction, the FLR bits are automatically copied to the condition code field of the PSW. The condition code is also updated from the FLR after an Instruction Read command.

When I/O is the destination, an output operation is to be performed. The nature of the output operation is encoded in the extended field of the instruction.

From the D field, it is possible to load either YD or YS. The determination is made by the least significant bit of the D field. See Table 3-6. When YD is the destination, the general register specified by the YD field of IR, is loaded. Similarly, when YS is the destination, the general register whose number is in the YS field is loaded.

On a Shift Left micro-instruction, when YD is the destination, the ALU output - shifted left one bit position - is copied into the register specified by YD. When the destination mnemonic is YD&Q the register specified by YD gets the left-shifted ALU output and the Q register is shifted left one bit position. Carry In and Carry Out specifications have unique meanings on shifts.

Shift Right is similar to Shift Left. When YD is the destination, the register specified by YD gets the right-shifted ALU output. When the destination is YD&Q, YD gets the right-shifted ALU output and the Q register is shifted right one bit position.

TABLE 3-6. DESTINATION REGISTER SPECIFICATIONS

RD BITS 3	4	5	12	13	14	MNEMONIC	COMMENTS
0	0	0	0	1	1	Q	Q ←ALU OUT
0	0	0	1	0	0	MR0&Q	MR0←ALU OUT, Q←ALU OUT
0	0	0	1	0	1	MAR&Q	MAR←ALU OUT, Q←ALU OUT
0	0	0	1	1	1	MDR&Q	MDR←ALU OUT, Q←ALU OUT
0	0	1	0	0	1	PSW	PSW←ALU OUT
0	0	1	0	1	0	FLR	FLR←ALU OUT
0	0	1	0	1	1	NULL	ALU OUTPUT IS LOST
0	0	1	0	1	1	MEM	ALU OUTPUT IS LOST
0	0	1	1	0	0	MR0	MR0←ALU OUT
0	0	1	1	0	1	MAR	MAR←ALU OUT
0	0	1	1	1	0	LOC	LOC←ALU OUT
0	0	1	1	1	1	MDR	MDR←ALU OUT
0	1	0	0	0	1	YDA&PSW	PSW←YS, YD←ALU OUT
0	1	0	1	0	0	YDA&MR0	MR0←YS, YD←ALU OUT
0	1	0	1	1	1	YDA&MDR	MDR←YS, YD←ALU OUT
0	1	1	0	0	0	YD	YD←ALU OUT
0	1	1	0	0	1	YS	YS←ALU OUT
1	0	0	0	1	1	YD&Q	$YD \overset{R}{\underset{1}{\leftarrow}}$ ALU OUT, $Q \overset{R}{\underset{1}{\leftarrow}} Q$
1	0	1	0	1	1	YD	$YD \overset{R}{\underset{1}{\leftarrow}}$ ALU OUT
1	1	0	0	1	1	YD&Q	$YD \overset{L}{\underset{1}{\leftarrow}}$ ALU OUT, $Q \overset{L}{\underset{1}{\leftarrow}} Q$
1	1	1	0	1	1	YD	$YD \overset{L}{\underset{1}{\leftarrow}}$ ALU OUT

3.8.1 System Initialization

System initialization occurs on power up or as a result of depressing the initialize switch. All peripheral controllers and certain functions internal to the processor are reset. After this, microcode execution begins at ROM address `000'. Initialize sets the PWRUP branch condition. The PWRUP condition causes the microcode to take a branch to the `INTERRUPT' sequence. Refer to Figure 3-3.

The `INITIAL' sequence consists of a two micro-instruction loop. nature of an interrupt request. The first branch in the sequence is a branch on PWRUP to the `INITIAL' sequence. The PWRUP branch condition remains active until the microcode has done a refresh to every memory row.

The `INITIAL' sequence consits of a two micro-instruction loop. Refresh commands are issued to the memory until the PWRUP branch condition goes away. This refresh sequence places an initial charge on every memory device. Without this, no memory accesses could be guaranteed. After the refresh sequence, the `SELFTEST' micro diagnostic routine is entered.

3.8.2 Micro Diagnostic Routines

The micro diagnostic comprises a number of small subtests. If an error is detected in any subtest, the microcode hangs up on the failed test. The nature and order of these tests is summarized below and in Figure 3-5.

TEST.000 Using the immediate data path, the flag register is loaded with zeros. Conditional branches on the C, V, G, or L conditions test that the flag register does contain zero (all flags reset).

TEST.001 Using the immediate data path, the flag register is loaded with hexadecimal 1. Conditional branch instructions test that the flag register does contain one (C, V, and G reset and L set).

TEST.002 Using the immediate data path, the flag register is loaded with hexadecimal 2. Conditional branch instructions test that the flag register does contain two (C, V, and L reset and G set).

TEST.004 Using the immediate data path, the flag register is loaded with hexadecimal 4. Conditional branch instructions test that the flag register does contain four (C, G, and L reset and V set).

TEST.008 Using the immediate data path, the flag register is loaded with hexadecimal 8. Conditional branch instructions test that the flag register does contain eight (V, G, and L reset and C set).

TEST.010 Using the immediate data path, the Q register is loaded with hexadecimal 2. The flag register is then loaded from the Q register and conditional branches test for the value 2.

TEST.01A Using the immediate data path, micro register 0 is loaded with hexadecimal 5. The flag register is then loaded from MR0 and conditional branches test for the value 5.

TEST.011 Using the immediate data path, micro register 0 is loaded with hexadecimal D. Using unconditional cross shift, the two bytes of micro register 0 are swapped. Again, using cross shift, MR0 bits 4 through 7 are swapped down and loaded into the flag register. Conditional branches test that the flag register equals D.

TEST.012 Using the immediate data path. The Q register is loaded with hexadecimal AA. MDR is loaded from the Q register. LOC is loaded from MDR. MAR is loaded from LOC. MR0 is loaded from MAR. FLR is loaded from MAR. Conditional branches test that the least significant digit, after being propagated through the Q register and stack registers, still equals hexadecimal A.

TEST.013 Using immediate data and the flag register as a result accumulator, the exclusive OR of hexadecimal A and hexadecimal A is tested for zero.

TEST.014 Using immediate data and the flag register as a result accumulator, the exclusive NOR of hexadecimal A and hexadecimal 5 is tested for zero.

TEST.015 Using immediate data and the flag register as a result accumulator, the sum of hexadecimal 2 and hexadecimal 2 is tested for hexadecimal 4.

The remainder of the micro diagnostic is an exercise of the first 8KB of memory.

TEST.020 Writes address as data in each halfword location X`0000´ through X`07FE´. TEST.030 writes the ones complement of address as data in each halfword location X`0800´ through X`0FFE´. TEST.040 writes address as data in each halfword location X`1000´ through X`17FE´. TEST.050 writes the ones complement of address as data in each halfword location X`1800´ through X`1FFE´.

TEST.060 Checks that each halfword location X`0000´ through X`07FE´ contains its own address. TEST.070 checks that each halfword location X`0800´ through X`0FFE´ contains the ones complement of its address. TEST.080 checks that each halfword location X`1000´ through X`17FE´ contains its own address. TEST.090 checks that each halfword location X`1800´ through X`1FFE´ contains the ones complement of its address.

A failure in one of the last four tests causes the processor to hang up in a test loop on the offending address.

After the go/no-go diagnostic, the microcode tests for the machine options. First, the PSW is set to all zeros and LOC is set to X`FFFC´. If the ARST strap option is in affect, the Q register is set to X`0002´ for subsequent LOC increments and routine RESTART is entered. There the ASCII console device is given a Reset command and then, through TEST2, user code execution begins at X`FFFC´.

The ARST strap option being in effect means that the top 8KB of main memory consists of Read Only Memory devices. The instruction at the top of memory (X`FFFC´) must be a branch to the actual start of the user´s fixed program.

If the ARST strap option is not in affect, the ALO option is tested. The ALO (Automatic Loader) is basically an ROM device. The data in the ROM comprises an initial bootload capability.

The ALO option is a strap option. The ALO option becomes active on initialize and remains active until any I/O device is addressed. In practice, the device is the ASCII console.

If the ALO condition is active, the microcode enters routine AUTOLOAD. There, the ALO halfwords are read over the standard multiplexor bus. The first halfword is a new PSW value, the second halfword is a new LOC value, the third halfword is a 16 bit start address, and the fourth halfword is a 16 bit end address. If the start address is greater than the end address, routine RESET is entered. There the ASCII console is given a reset command and the ASCII console routine is entered. This situation is indicative of a failure with the ALO.

If the start address is less than the final address, the remaining halfwords are read from the ALO device and stored in sequential halfword locations in main memory. The area of memory loaded is identified by the start and end addresses. After the load, routine RESTART resets the ASCII console device and, through TEST2, user program execution begins at the address specified by the new LOC.

If there is no ALO, the ASCII console routine is entered through routine RESET.

Figure 3-4 shows the general interrupt support routines and Figure 3-6 shows the ASCII console routine.

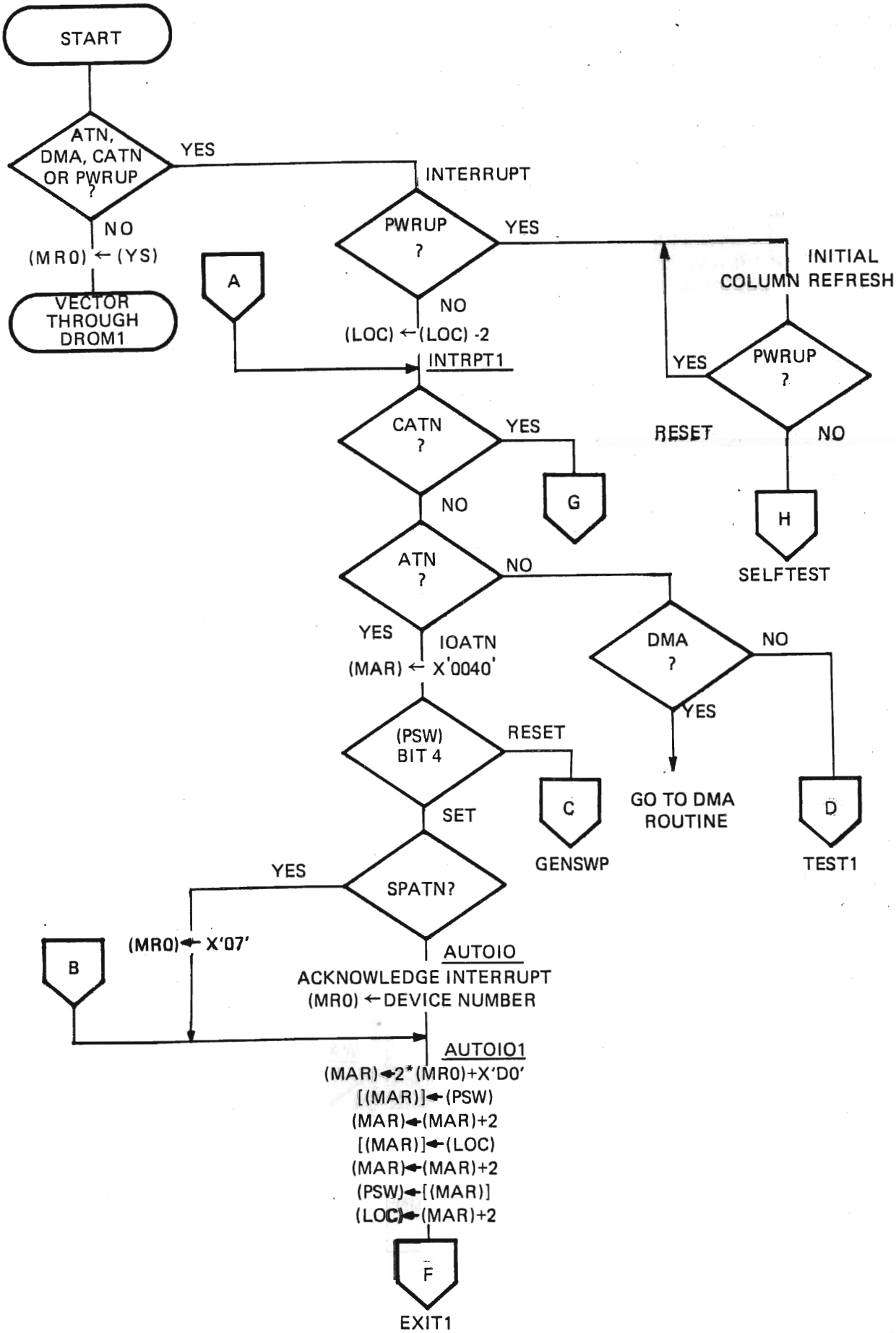


Figure 3-3. Initialization

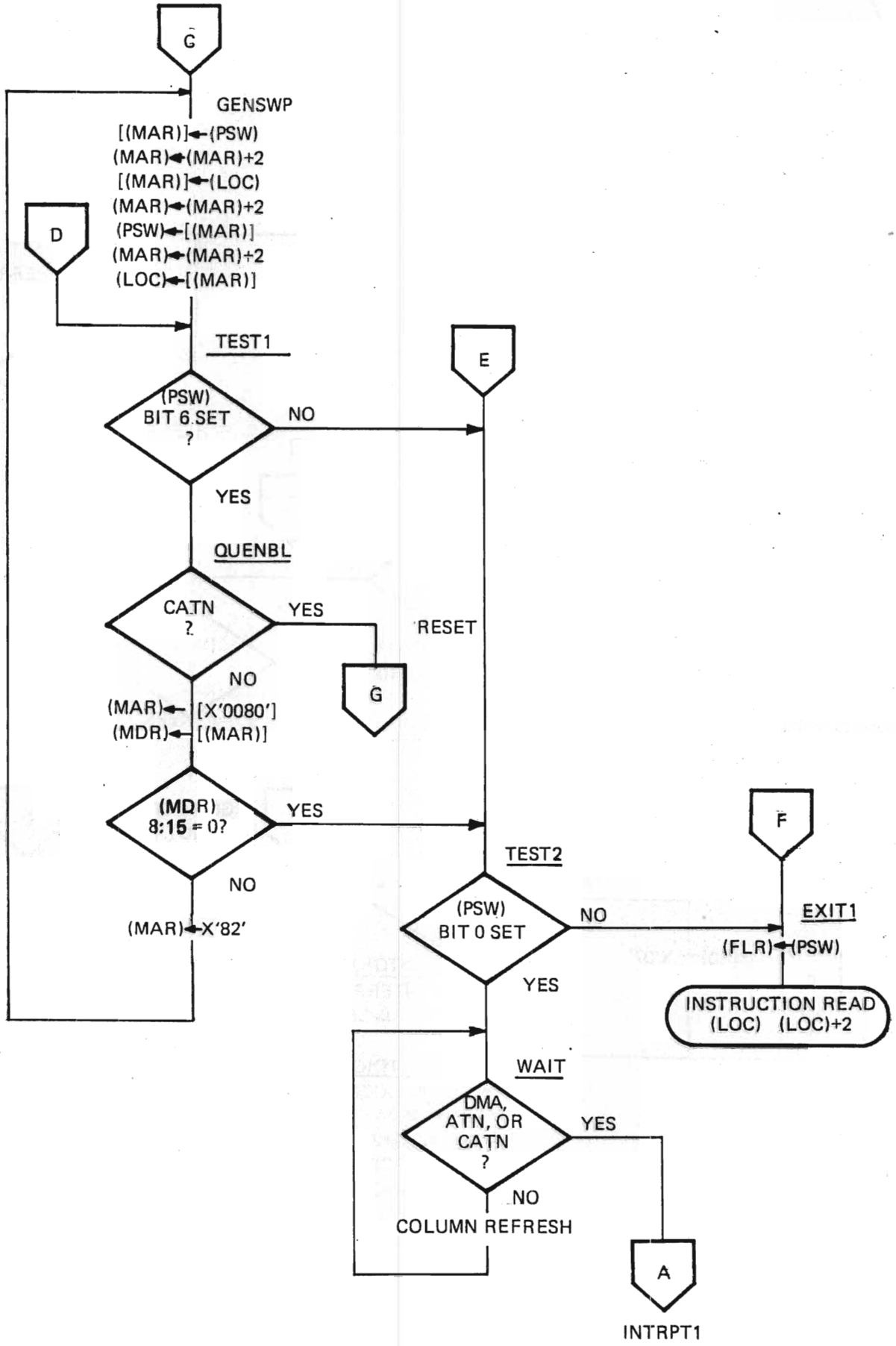


Figure 3-4. Interrupt Support

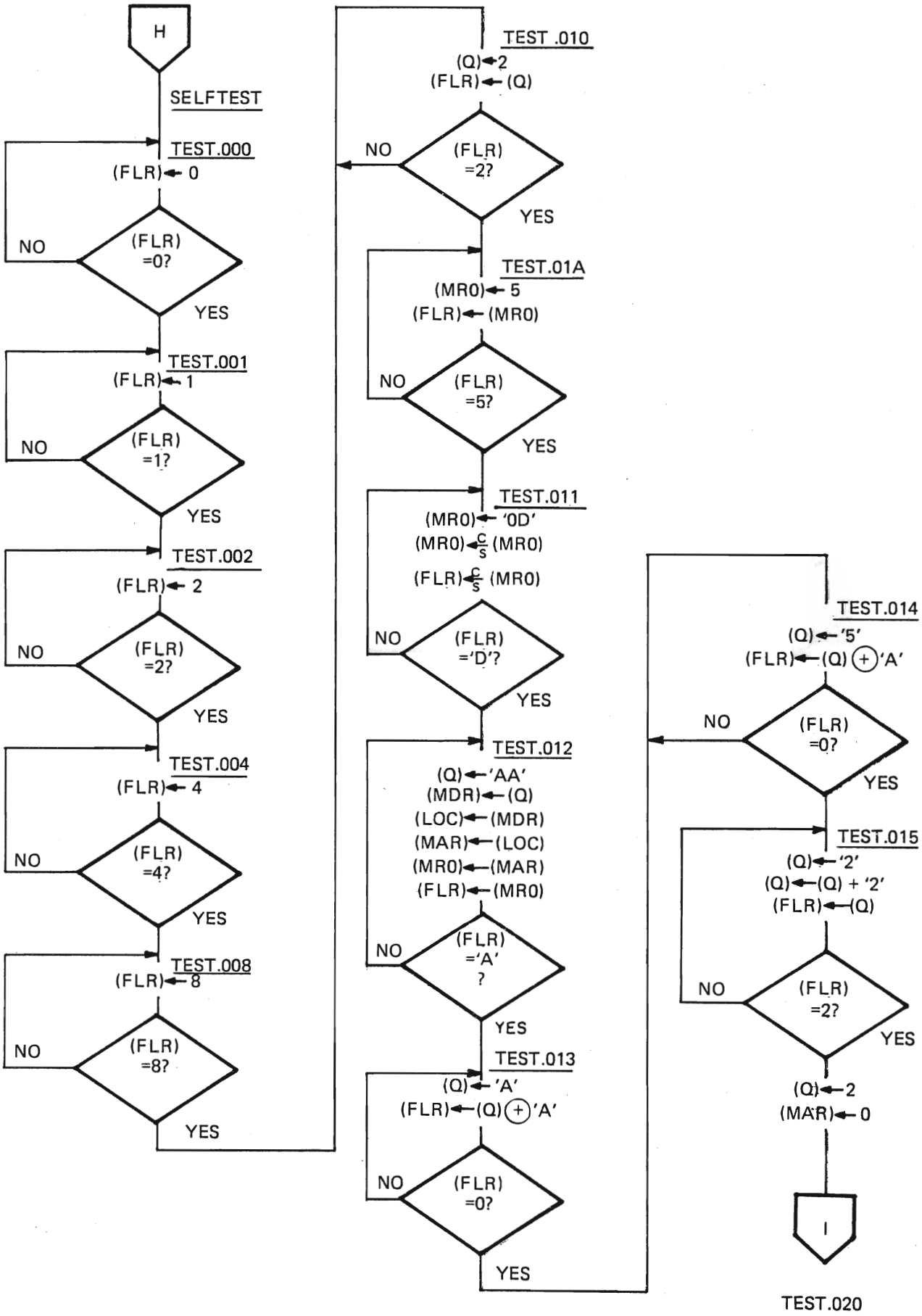


Figure 3-5. Micro Diagnostic Routines

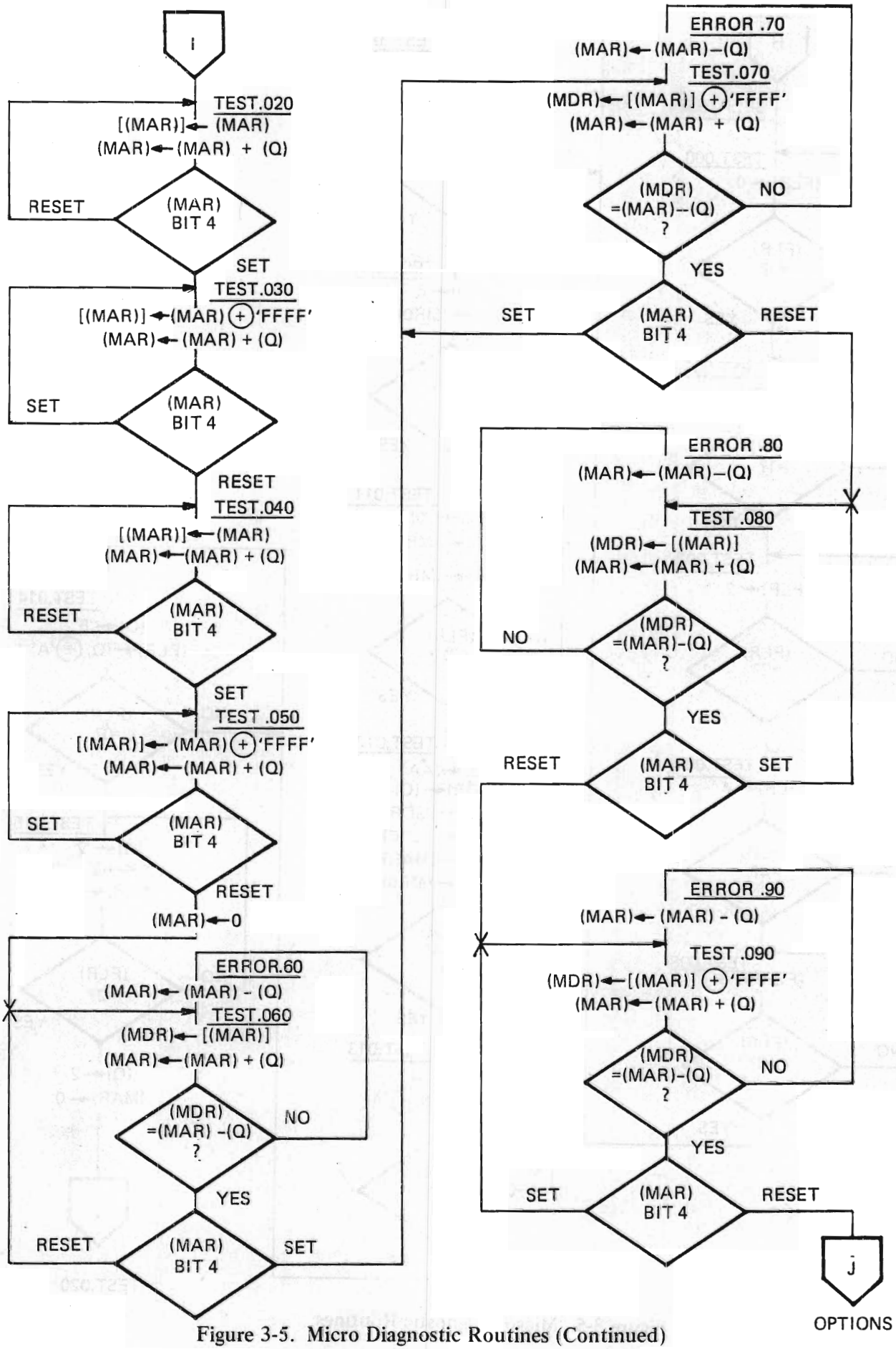


Figure 3-5. Micro Diagnostic Routines (Continued)

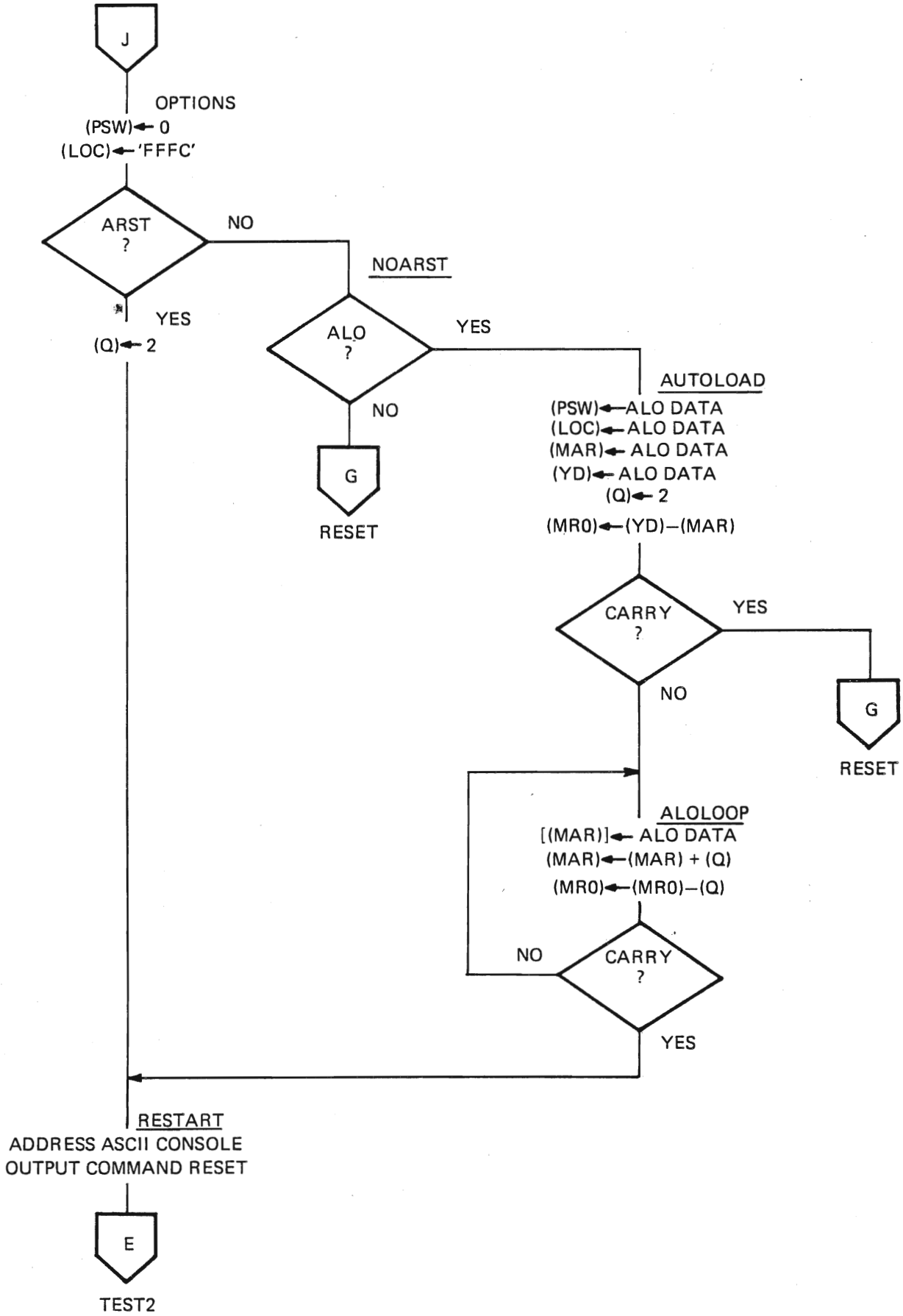


Figure 3-5. Micro Diagnostic Routines (Continued)

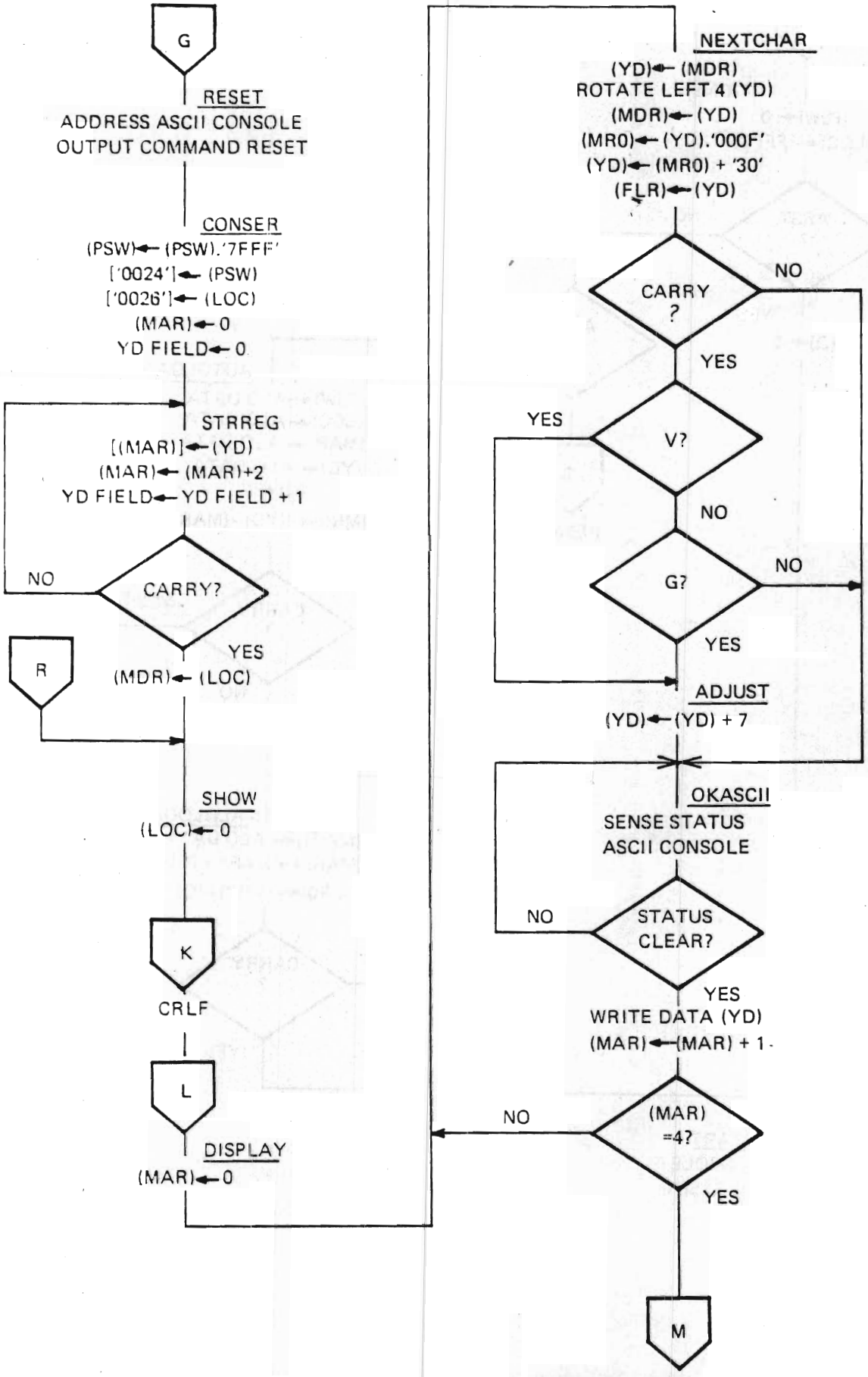


Figure 3-6. ASCII Console Support

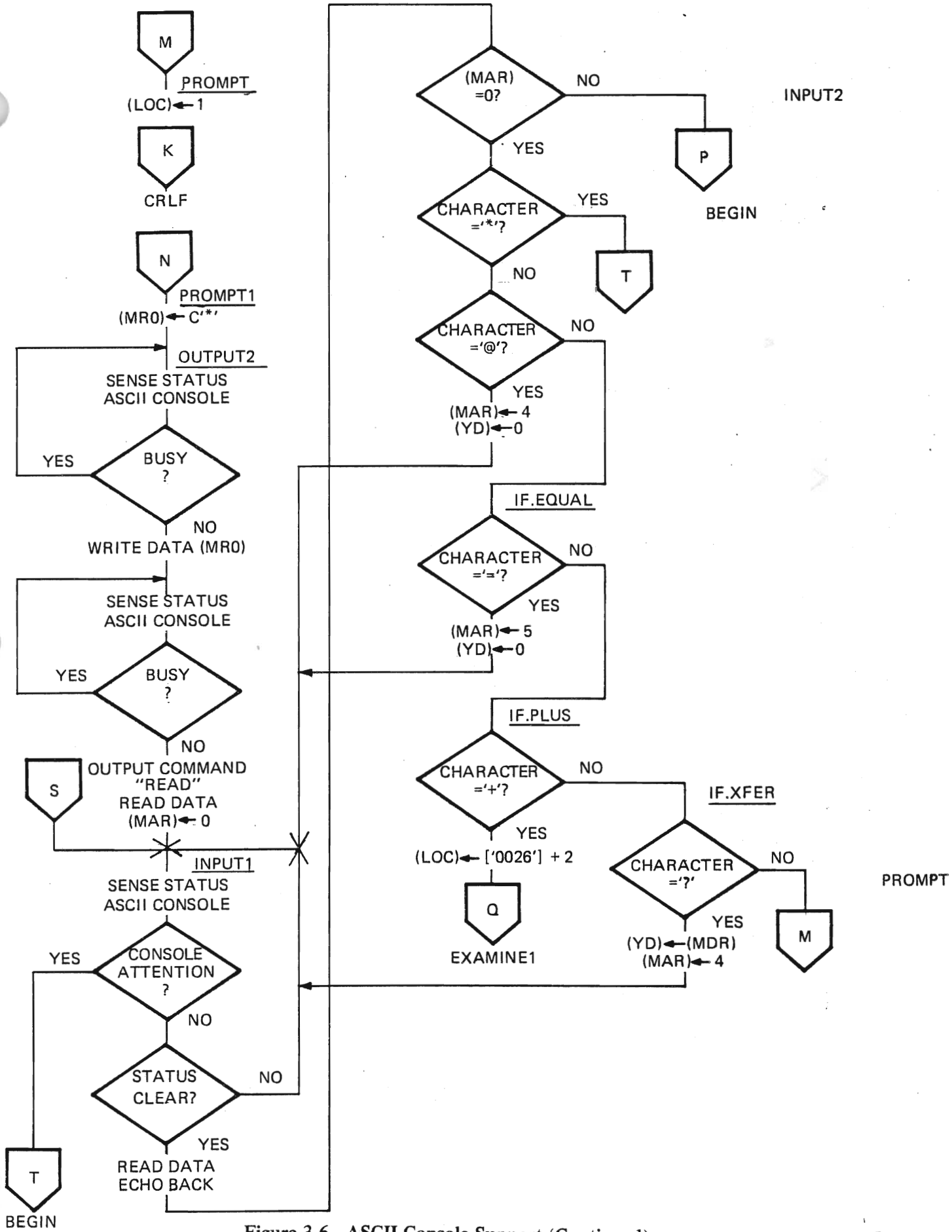


Figure 3-6. ASCII Console Support (Continued)

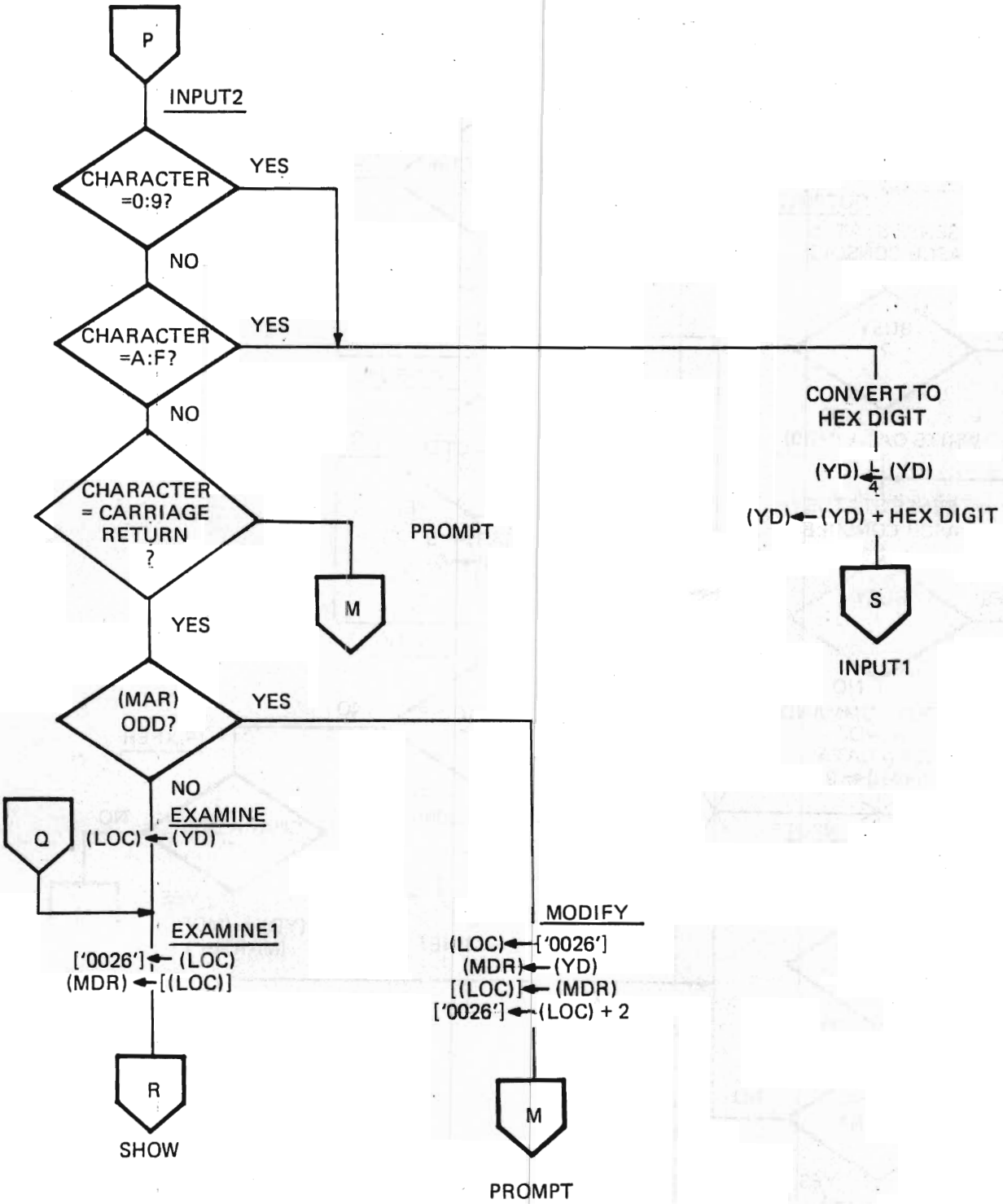


Figure 3-6. ASCII Console Support (Continued)

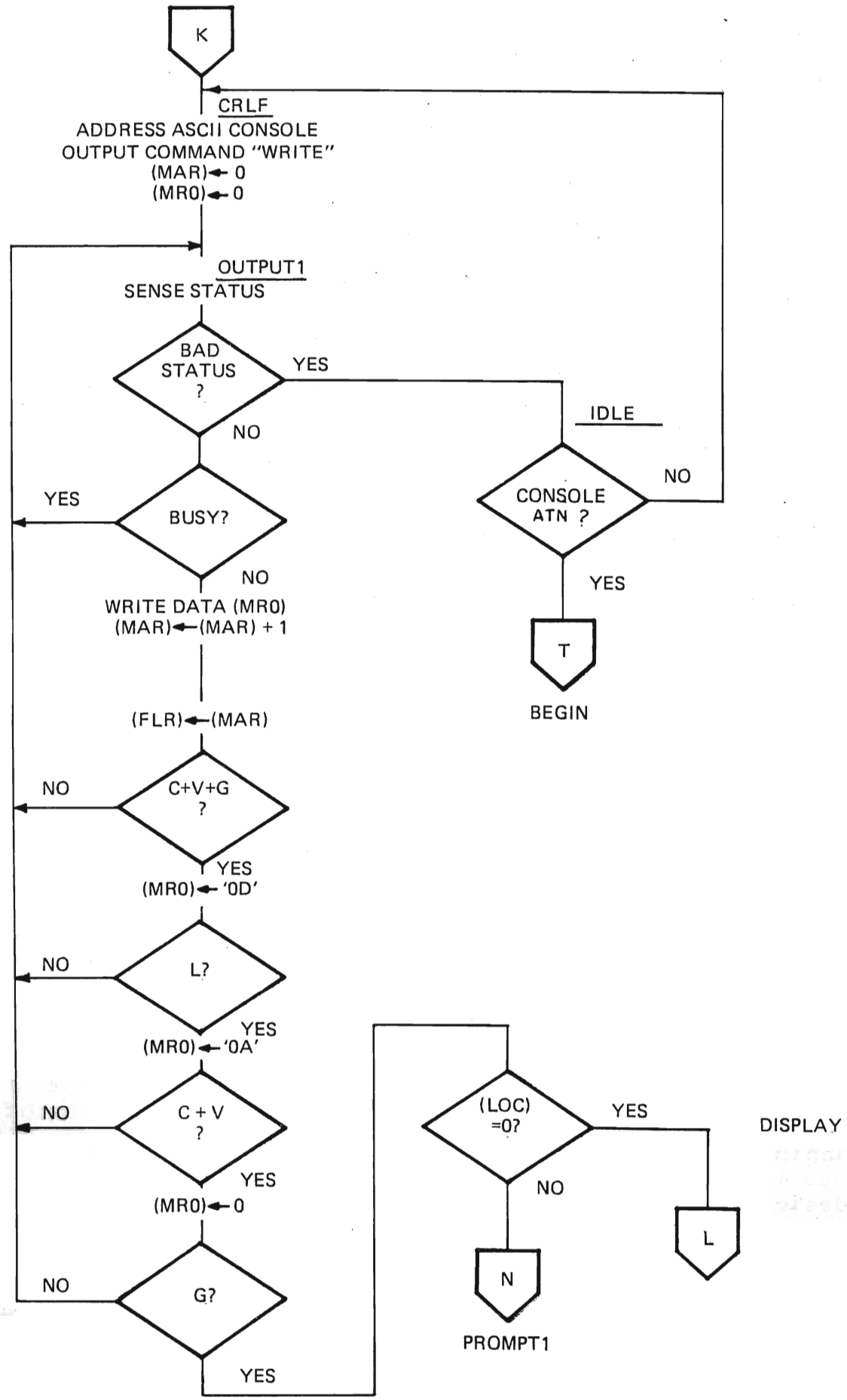


Figure 3-6. ASCII Console Support (Continued)

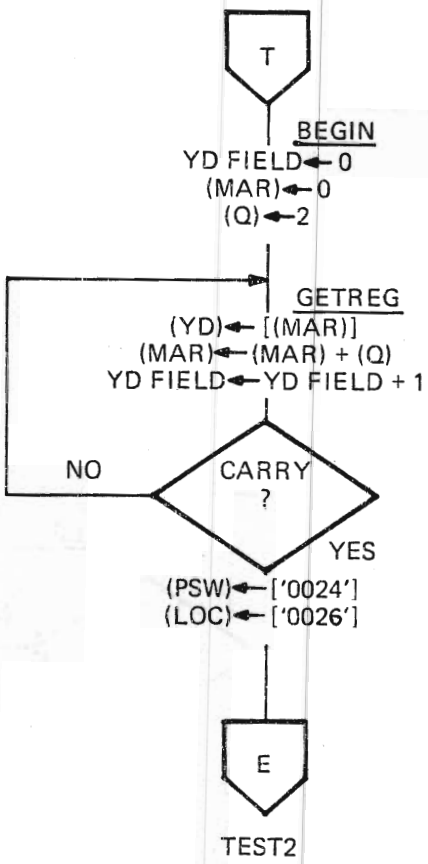


Figure 3-6. ASCII Console Support (Continued)

3.9 FUNCTIONAL DIAGRAM ANALYSIS

This paragraph relates to Functional Schematics 35-637, Sheets 1 through 12, 35-638, 35-639, and 35-640. The last character of the mnemonic symbol on INTERDATA Functional Schematics designates the logic level at the time the signal is active. For example, D050 is data line number 5 (D05). The last character (0) indicates that when D05 is active, the line is at a logical level of ZERO. Refer to the General Description, Chapter 1 for further information concerning the INTERDATA documentation system.

3.9.1 Clock Control (Sheet 12)

The clock signals CLK, DCLK, and DDCLK are outputs of J-K flip-flops which are driven by the buffered output, OSC0 of a free-running LC oscillator. The period of the square wave OSC0 is set to 60 nanoseconds by the variable Capacitor C107. TP1 and TP2, designated Disable Oscillator (DISOSC0) and External Oscillator (EXOSC0) respectively, are maintenance test points. An active DISOSC0 inhibits the oscillator to allow an external source applied to EXOSC0 to control OSC0.

The clock registers respond to the falling edge of OSC0 and generate CLK1, DCLK1, and DDCLK1 in the sequence shown in Figure 3-7. The pulse width of the clock signal is 120 nanoseconds and the period of each is 300 nanoseconds. All Processor clock signals are derived from CLK, DCLK, and DDCLK.

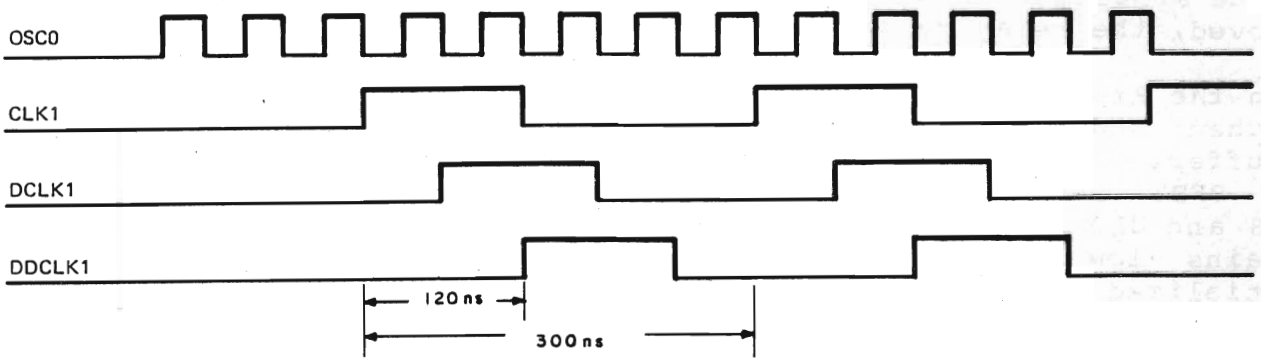


Figure 3-7. Clock Timing Nominal

Two basic Processor clocks are derived from CLK1, the Destination Clock (DESCLK) and the ROM Data Clock (CKRD). DESCLK0 is the LSI micro-processor chip clock (Sheet 4) and DESCLK1, the Flag Register Clock (Sheet 7). Figure 3-8 describes the function of the ROM Data clock.

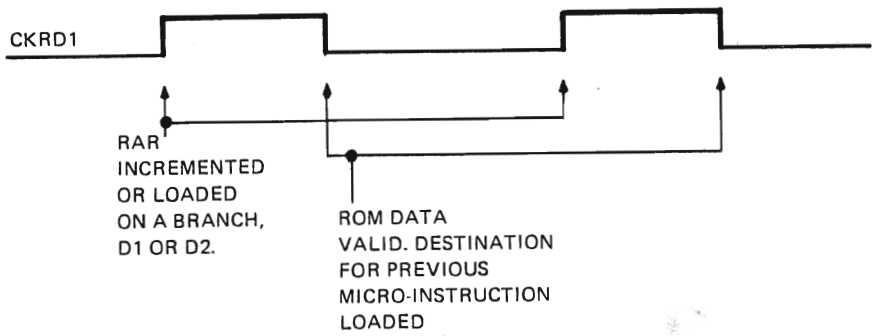


Figure 3-8. Specific Clock Functions

DESCLK and CKRD are inhibited whenever the Timing Test Point (FTIT0) is made active or during an Input/Output (IOSTOP0) operation or if the micro-instruction calls for a memory operation (MEM1) when the Column Address Select register (FCAS1) is set. DSCLK is also blocked whenever a Branch (BRANCH0) or an address modification (DSTOP0) is decoded from the micro-instruction.

3.9.2 Initialize Control (Sheet 10)

System Initialize is performed by de-energizing the System Clear (SCLR) relay. This is accomplished by:

1. Placing the processor in the OFF condition.

2. Operating the processor INIT (Initialize) switch.

3. Loss of P5 or P12.

On power up, SCLR0, a metallic contact to ground of a relay, forces SCLR0A low to insure predictable initial states of latched functions within the Processor. When P5 and P12 are within regulation the voltage built up on C108 and C109 becomes sufficient for the Darlington connected transistors Q2 and Q1 to operate the relay and remove ground from SCLR0. SCLR0A deactivates when the normally open contact of the relay makes.

If the Processor is placed in the OFF state, or P5 or P12 is removed, the relay releases and connects SCLR0 to ground.

When the Processor is initialized, Power Fail Detected (PFDT0) is latched and C108 and C109 discharge through D3 and the output of a buffer. The relay drops out and activates SCLR0 and SCLR0A. The PFDT latch is cleared by SCLR0A and the discharge path for C108 and C109 is eliminated. When the relay is energized, SCLR0 remains low and SCLR0A forces the Processor to a predictable initialized state.

3.9.3 Read Only Memory (ROM) (SH 6)

The Read Only Memory (ROM) is a high speed, solid state, non-destructive memory which holds the microprogram. The ROM is organized into two pages of 512 words; each word is 24 bits in length. Each page of ROM contains three Integrated Circuit (IC) packages arranged such that each IC holds eight bits of each word on the associated page. An additional ROM chip (512 x 8) comprises the Decoder ROM (DROM).

Each ROM IC contains two enable leads (CE1 and CE2), and a strobe lead (see Sheet 6). To enable the ROM chip CE1 must be Low and CE2 must be High. The strobe (CKRD0) is used to latch the data at the output of the ROM. The ROM contains internal latches which are used to hold the ROM Data (RD), refer to Figure 3-9 ROM timing.

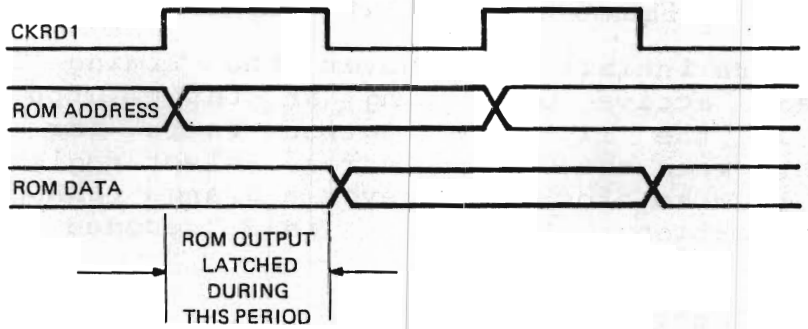


Figure 3-9. ROM Timing

3.9.3.1 Decoder ROM (DROM). The Decoder ROM (DROM) is a single integrated circuit, refer to Sheet 5. It contains 512 eight bit words. The DROM is addressed by the most significant eight bits of the Instruction Register (OP Code Field). Each of the 256 possible combinations of this decoded function may address two locations in the DROM, depending on the state of D10 (5D1), a decoded function of RD0, RD1, and RD2. When D10 is low, one of the first 256 words of the DROM is selected, corresponding to a microcode D1. Illegal instructions are decoded in the DROM.

3.9.3.2 ROM Address Register (RAR). The ROM Address Register (RAR), Sheet 5, is a 10-bit register which is loaded on the positive edge of CKRD1 from the DROM during a decode micro-operation or from the ROM data bits during a branch micro-operation. The register is arranged as a counter to allow sequential ROM addresses to be accessed. The RAR is cleared on power up to address X`100´ and the microprogram begins execution at this location. It is also cleared for Decoded Instruction Read (DIR0).

3.9.4 Processor Registers

The majority of the instructions contained in the microprogram are concerned with relocating data from one processor register to another. Most of the processor registers are general purpose registers; however, some do perform special functions. Each register is described in the following sections.

3.9.4.1 Register Stack (Sheet 8). The Register Stack consists of four MSI chips, each of which has a capacity of four 4-bit words. Each of the chip modes (read or write) has its own pair of register select lines and an enable line. Contained in the stack are the Micro Register (MR0), the Memory Address Register (MAR), the Location Counter (LOC), and the Memory Data Register (MDR). Inputs to the stack are supplied by 2:1 multiplexors from either the S Bus or the MSXX1 memory output on an unload from memory (UMEM0). RD18 and RD19 are the read register select bits and RD13 and RD14 the write register select bits. The read enable is activated by RD150 and RD171.

RD121 is active if the stack is specified as a destination. The write enable is established during CLK1 if DESTP0 is inactive. When MR0, MAR, or LOC is the destination, all 16 data inputs are stored in the selected register by the write enable. When MDR is the specified destination stack, writing is also controlled by Decode Stack High and/or Low (DSTKH0, DSTKL0). These signals are active only on a microcode specified cross shift. The high order eight bits of MDR are written when DSTKH0 is not active and the low order eight bits when DSTKL0 is not active.

The open collector outputs of the stack connect to the processor B Bus.

3.9.4.2 Instruction Register (IR). The Instruction Register (IR) is a 16-bit register which stores the user instruction currently being executed. The IR consists of three fields: the OP-code (bits 0-7), the User Destination, YD (bits 8-11), and User Source, YS (bits 12-15). The instruction to be stored in the IR is obtained from the Memory Sense (MS) lines and is loaded by the Instruction Read flip-flop (FINR0).

Two Quad D Registers store the Op code field (Sheet 5). This field serves as eight bits of the DROM address.

The YD field is contained in a 4-Bit Up-Down counter (Sheet 7). YD, User Destination, identifies one of 16 general registers located in the LSI micro-controller chips (Sheet 4) in which the result of the execution of the current user instruction is to be stored. On sheet 7, if YDP1 is specified by the micro-instruction, the YD register is incremented by one at the end of the micro-instruction. If YDM1 is specified, the YD register is decremented by one at the end of the micro-instruction. On a clear YD (CLYD0) from the micro-instruction, YD is cleared during CLK1.

YS, the User Source field, is contained in a Quad D flip-flop (Sheet 7). The second operand of the user instruction is the contents of the general register specified by YS for RR instructions. For RX or RS instructions, YS identifies the general register to be used for indexing, and for SF instructions YS is data.

3.9.4.3 Flag Register (FLR) and Condition Code (CC). The Flag Register (FLR) (Sheet 7) is a 4-bit register which contains the Carry Flag (C), the Overflow Flag (V), the Greater than Flag (G), and the Less Than Flag (L). The contents of the register, FLR 12:15 are loaded in the 4-bit condition code of the PSW (Sheet 6) at the end of each user instruction. The flags are the results of arithmetic and logical micro-instruction execution.

The FLR is cleared directly (CLFLR0)when CKRD0 is active, if an IR micro-instruction is being executed. Results of micro-instruction execution are loaded into FLR on the trailing edge of DESCLK1, under the control of a programmable logic array chip.

The FLR is loaded whenever either the FLR or Program Status Word (PSW) register is specified as a destination. On an instruction read, or after a Load PSW micro-instruction, the contents of FLR are loaded into the CC. FLR outputs are also used by the Branch Logic (Sheet 10) for conditional branches.

The C, V, G, and L outputs of the Flag Register serve as modifiers as described below and is controlled by the truth table of Table 3-7.

The Carry Flag (C) is affected by any Arithmetic Boolean, Shift or Load micro-instruction when Carry Out (CO) is specified. The Carry Flag sets on a Shift if the bit shifted from the LSI micro-controller (Sheet 4) is high, if Carry (CARRY1) from the LSI micro-controller is high on an Add, or if CARRY1 is inactive on a Subtract. In all other cases, the Carry Flag is reset.

The Overflow Flag (V) is set directly by SV0 when a false SYNC is detected on an I/O operation, and is changed on any Add or Subtract micro-instruction if F1 is specified. Overflow (OVL1) is an output of the LSI micro-controller (Sheet 4) and is only valid for Add or Subtract micro-instructions.

The Greater Than (G) and Less Than (L) Flags change on any Load, Arithmetic, or Boolean micro-instruction when Fl is specified. The G Flag is set if the result of the operation is positive or if the result is zero and either the G or L was set from a previous operation. The L Flag is set if the resulting sign is negative. Either flag is reset if these conditions are not met.

TABLE 3-7. PLA FLAG TRUTH TABLE

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_m	$\overline{I_m}$	DON'T CARE	PROD. TERM PRESENT IN F_o	PROD. TERM *NOT* PRESENT IN F_o	ACTIVE HIGH	ACTIVE LOW
H	L	– (dash)	A	● (period)	H	L
NOTE: Enter (–) for *unused* inputs of *used* P-terms.			NOTES: 1) Entries independent of output polarity. 2) Enter (A) for *unused* outputs of *used* P-terms.		NOTES: 1) Polarity programmed once only 2) Enter (H) for all *unused* outputs	

PRODUCT TERM*																ACTIVE LEVEL							
	INPUT VARIABLE															H	H	H	H	H	L	H	H
NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OUTPUT FUNCTION*							
																	7	6	5	4	3	2	1	0
0	H	–	–	–	–	–	–	–	–	–	–	–	–	–	H	–	•	•	•	•	•	•	•	A
1	–	H	H	–	–	–	–	–	–	–	–	–	–	–	–	–	•	•	•	•	•	A	•	A
2	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–	•	•	•	•	•	•	A	•
3	–	–	–	–	–	–	–	–	–	–	–	–	–	–	H	–	•	A	•	A	•	•	A	•
4	–	–	–	L	–	–	–	–	–	–	–	–	–	–	H	–	•	•	•	•	•	A	•	•
5	–	–	H	–	H	–	–	–	–	–	–	–	–	–	–	H	•	•	•	•	•	A	•	•
6	–	–	–	–	–	H	–	–	–	–	–	–	–	–	H	–	•	•	•	•	A	•	•	•
7	–	–	H	–	–	–	H	L	–	–	–	–	–	–	–	–	•	•	•	•	A	•	•	•
8	–	–	H	–	–	–	H	–	L	–	–	–	–	–	–	–	•	•	•	•	A	•	•	•
9	–	–	H	–	–	–	–	L	–	–	–	–	–	–	–	–	•	•	•	A	•	•	•	•
10	–	–	H	–	–	–	–	–	L	–	–	–	–	–	–	–	•	•	•	A	•	•	•	•
11	–	–	–	–	–	–	–	–	–	H	–	–	–	–	H	–	•	•	A	•	•	•	•	•
12	–	–	–	–	–	–	–	–	–	–	H	H	H	–	–	–	•	•	A	•	•	•	•	•
13	–	–	–	–	–	–	–	L	–	–	–	L	–	H	–	–	•	•	A	•	•	•	•	•
14	–	–	–	–	–	–	–	–	L	–	–	L	–	L	–	–	•	•	A	•	•	•	•	•
15	–	–	–	–	–	–	–	–	–	–	–	–	H	–	–	–	•	A	•	•	•	•	•	•

3.9.4.4 Shift Control. The LSI micro-controller components making up the processor (Sheet 4) have the capability of shifting 16 or 32 bits of data right or left under microprogram control. The ports on these chips associated with this capability are SLOSRI (Shift Left Out, Shift Right In), and SROSLI (Shift Right Out, Shift Left In) for shifting the general purpose register left or right. Signals QLOQRI (Q Register Left Out, Q Register Right In) and QROQLI (Q Register Right Out, Q Register Left In) are associated with a 16-bit internal extension register for double precision shifting capability. The controls for this are shown on Sheet 13. (See Table 3-8, Shift Table for Shift PLA.) For single and double precision shifts, Carry Out (CO) is specified to load the C flag. Carry In (CI) is used as a control to determine whether data is rotated or shifted by the control logic.

TABLE 3-8. SHIFT TABLE FOR SHIFT PLA

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_m	$\overline{I_m}$	DON'T CARE	PROD. TERM PRESENT IN F_p	PROD. TERM *NOT* PRESENT IN F_p	ACTIVE HIGH	ACTIVE LOW
H	L	– (dash)	A	● (period)	H	L
NOTE: Enter (–) for *unused* inputs of *used* P-terms.			NOTES: 1) Entries independent of output polarity. 2) Enter (A) for *unused* outputs of *used* P-terms.		NOTES: 1) Polarity programmed once only. 2) Enter (H) for all *unused* outputs.	

NO.	PRODUCT TERM* INPUT VARIABLE																ACTIVE LEVEL H H H H H H H H OUTPUT FUNCTION*							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	L	–	–	–	–	–	–	–	–	–	•	A	•	•	A	•	•	•
1	–	–	H	–	–	–	H	–	–	–	H	L	L	–	L	H	•	A	•	•	•	•	•	•
2	–	–	–	–	–	–	H	–	–	–	–	–	–	–	–	–	•	•	A	•	•	•	A	•
3	–	–	–	H	–	–	L	–	–	–	–	–	–	–	–	–	•	•	A	•	•	•	•	•
4	–	H	–	–	–	–	H	H	–	–	H	L	H	–	L	H	•	•	•	•	A	•	•	•
5	–	–	H	–	–	–	H	H	–	–	H	L	L	–	L	H	•	•	•	•	A	•	•	•
6	H	–	–	–	–	–	H	L	–	–	–	–	–	–	–	–	•	•	•	•	A	•	•	•
7	–	H	–	–	–	–	H	–	–	–	–	–	–	–	–	–	•	•	•	•	•	A	•	•
8	–	–	–	H	–	–	L	H	–	–	–	–	–	–	–	–	•	•	•	•	•	A	•	•
9	–	–	–	–	H	–	L	L	–	–	–	–	–	–	–	–	•	•	•	•	•	A	•	•
10	–	–	–	H	–	–	L	H	–	–	H	L	H	–	L	H	•	•	•	•	•	•	A	•
11	–	–	–	–	H	–	L	L	–	–	H	L	H	–	L	H	•	•	•	•	•	•	A	•
12	–	–	H	–	–	–	L	–	–	–	H	L	L	–	L	H	•	•	•	•	•	•	A	•
13	–	–	H	–	–	H	–	–	–	–	H	L	–	–	L	H	•	•	•	•	•	•	•	A
14	–	–	–	–	–	H	–	–	L	H	L	L	–	–	L	L	•	•	•	•	•	•	•	A
15	–	–	–	–	–	H	–	–	H	H	L	L	–	–	L	H	•	•	•	•	•	•	•	A
16	–	–	L	–	–	L	–	–	–	–	–	H	–	–	–	–	•	•	•	•	•	•	•	A
17	–	–	L	–	–	L	–	–	–	–	–	–	–	–	H	–	•	•	•	•	•	•	•	A
18	–	–	L	–	–	L	–	–	–	–	H	–	–	–	–	–	•	•	•	•	•	•	•	A
19	–	–	L	–	–	L	–	–	–	L	–	–	–	–	–	–	•	•	•	•	•	•	•	A
20	–	–	L	–	–	L	–	–	H	–	–	–	–	–	–	L	•	•	•	•	•	•	•	A
21	–	–	L	–	–	L	–	–	L	–	–	–	–	–	–	H	•	•	•	•	•	•	•	A
22	–	–	–	–	–	L	–	–	–	–	–	H	–	–	–	–	•	•	•	•	•	•	•	A
23	–	–	–	–	–	L	–	–	–	–	–	–	–	–	H	–	•	•	•	•	•	•	•	A
24	–	–	–	–	–	L	–	–	–	–	H	–	–	–	–	L	•	•	•	•	•	•	•	A
25	–	–	–	–	–	L	–	–	–	L	L	–	–	–	–	–	•	•	•	•	•	•	•	A
26	–	–	–	–	–	L	–	–	–	L	–	–	–	–	–	L	•	•	•	•	•	•	•	A
27	–	–	–	–	–	L	–	–	H	–	L	–	–	–	–	L	•	•	•	•	•	•	•	A
28	–	–	–	–	–	L	–	–	L	–	L	–	–	–	–	H	•	•	•	•	•	•	•	A
29	–	–	–	–	–	–	–	–	–	H	H	L	–	–	L	–	A	•	•	•	•	•	•	•
30	–	H	–	–	–	–	H	–	–	–	H	L	H	–	L	H	•	A	•	•	•	•	•	•
31	–	–	–	–	–	–	–	–	H	H	L	L	–	–	L	H	A	•	•	•	•	•	•	•
32	–	–	–	–	–	–	–	–	H		H	L	–	–	L	–	•	•	•	A	•	•	•	•
33	–	–	H	–	–	–	L	–	L	H	L	L	–	–	L	L	•	•	•	•	•	•	A	•
34	–	–	–	–	–	–	–	–	L	H	L	L	–	–	L	L	•	•	•	A	•	•	•	•

Table 3-9 shows the states of the shift ports of the processor.

TABLE 3-9. PROCESSOR SHIFT PORT STATUS

FUNCTION	SLISR01	QLOQRI1	SLOSRI1	QLIQRO1
Shift Left	0	Z	Z	0
Shift Right	Z	0	0	Z
Double Precision Shift Left	Z	Z	Z	0 or Z*
Double Precision Shift Right	Z	Z	0 or Z*	Z

Z = Open collector output state, equal to bits being shifted out of these ports.

* 0 or Z depends on the state of Carry In (CI).
CI = 1 for a rotate, and the port state is Z.
CI = 0 for a shift, and the port state is 0.

3.9.4.5 Processor, Data Multiplexor, and Cross Shift Multiplexor. The Processor (Sheet 4) consists of four LSI chips which form a 16-bit wide data path. 0 These chips contain an Arithmetic Logic Unit (ALU), a 16 x 16 general purpose register stack with the dual port access to the ALU, a 16-bit extension register, and logic to control shifts both single and double precision.

Data Inputs (DIXX1) for the Processor are supplied by the 2:1 cross shift multiplexors (Sheet 8) which have internal storage. The multiplexor interfaces to the B Bus, and is loaded on the trailing edge of DDCLK1. Immediate functions disable Cross Shift (CS1) and the Cross Shift Multiplexor outputs correspond directly with the B Bus bits. When cross shift is specified, CS1 is a function of MAR151.

The Data Multiplexors (Sheet 8) are ROM controlled and consist of a pair of 4:1 tri-state multiplexors and three 2:1 multiplexors.

The outputs of the Processor chips form the S Bus. FDAT0 gates S081:151 to D080:150. The transceivers for D000:070 are enabled by an I/O operation, I00, and FDAT1 gated with RD211 or the Address, AD0, signal from the microbus controller. Signals S001:071 or S081:151 are multiplexed and gated to D000:070. With AD0 inactive, the byte stored in the multiplexor by an active FDAT1 is controlled by RD231. Signals S081:151 are stored when RD231 is active, otherwise S001:071 are transmitted to the I/O Bus. An active AD0 inhibits loading the multiplexor registers which contain the eight bit address of the most recent or current I/O device serviced.

3.9.5 I/O Control

An I/O operation is initiated if I/O is the Source or Destination of a micro-instruction. The I/O control logic is shown on Sheet 9. If I/O is a source, then an Input operation is initiated or if I/O is a destination, an output operation is indicated. I/O Timing is discussed separately for input and output.

3.9.5.1 Input. Refer to Figure 3-10 for timing information. When I/O is specified as a source, unload I/O (UIO0) is decoded and IOSTOP0 goes active. On the trailing edge of the next clock (CLK1) the Control In flip-flop (FCIN) sets. On receipt of SYN0 from the selected I/O device or the detection of false SYNC, the 14 millisecond timing (15N7) times out, the SYNC flip-flop sets which deactivates IOSTOP0. On the trailing edge of the next CLK1 the destination register is loaded and both the Control In flip-flop and the SYNC flip-flop reset completing the operation.

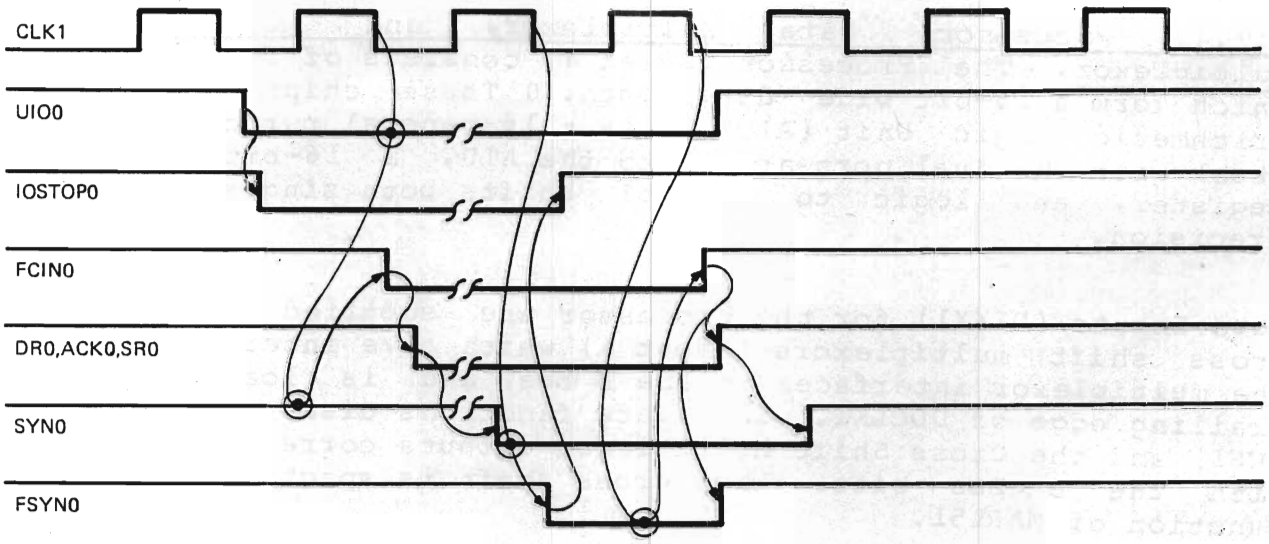


Figure 3-10. I/O Input

3.9.5.2 Output. Refer to Figure 3-11 for output timing information. When I/O is a destination Load I/O LDI00 (15J6) is detected, IOSTOP0 goes active and on the leading edge of the next CLK1 the Data flip-flop (FDAT) sets. The output of the Data flip-flop is used to gate data to the data bus, D000:160. On the trailing edge of the next DDCLK1 the Control Out flip-flop is set which activates the specified output control line. The output operation now progresses in the same manner as the I/O input operation discussed previously.

3.9.5.3 Micro Bus Operations. The Micro-Bus adapter, 35-630, is used to convert the standard Interdata Multiplexor bus to an I/O protocol similar to the Motorola 6800 or Intel 8080 microprocessor buses (Micro-Bus). Refer to functional schematic 35-638D08.

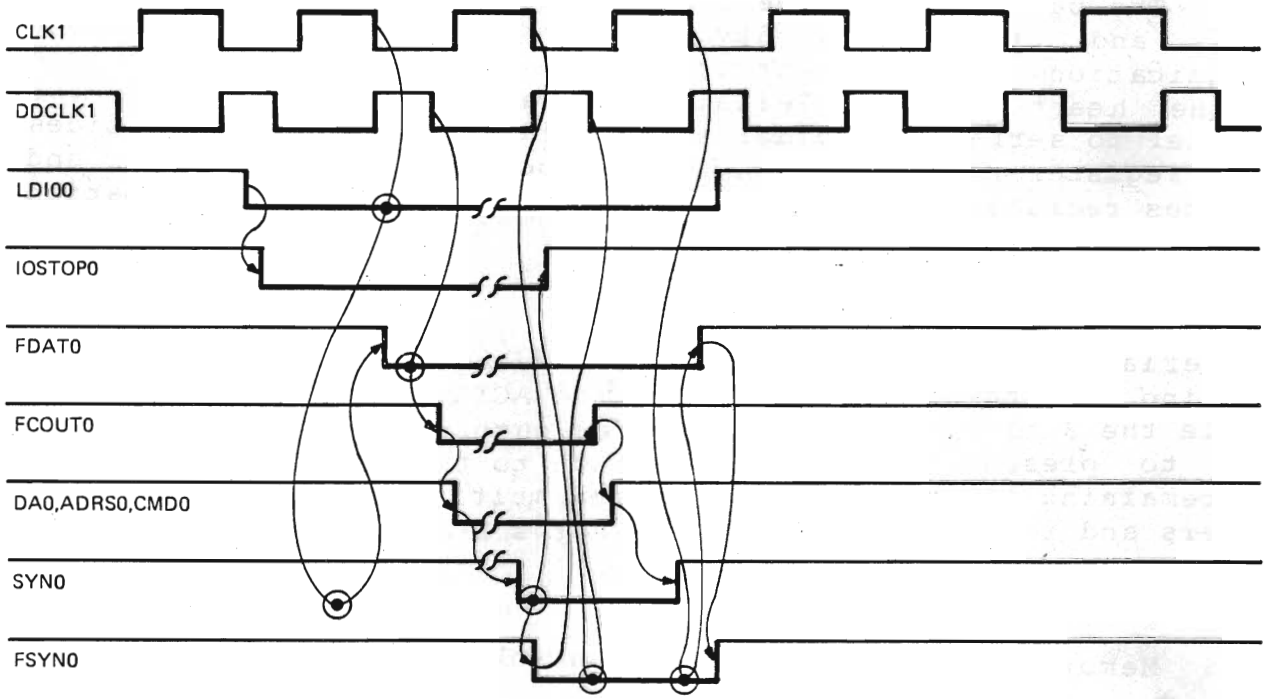


Figure 3-11. I/O Output

The decoding logic (Sheet 2) selects a group of addresses which are designated as micro-bus peripheral addresses, normally strapped for an address range of X`C0´ to X`FF´. When an address within this range is selected the Address flip-flop (2J9) become direct set. The output of this flip-flop, AD0A, enables the micro-bus adapter and indicates to the processor, AD0 (2LA), that the I/O operation to be performed is over the micro-bus.

The I/O control lines DR0, SR0, DA0, and CMD0 are gated by AD0A (3B1-3B3) and decoded to generate the proper micro-bus control lines READ0, WRITE0 Command/Data (C/D) and are then presented to the micro-bus. The gating of any of these multiplexor control lines will cause COM1 (3J3) to become active, removing the clear to the sequencer network (3F7-3K7) allowing two additional control lines to become active Valid Peripheral Address (VPA0) and SYN0 during their proper time slots.

The enable clock ENABLE1 is a free running clock with a 1.2 micro-second period, BCLK1 from the processor divided by four (3H7).

The logic for resolving the interrupt priorities on the Model 5/16 system is located on sheet 3. The interrupt priorities are as follows: the built in Serial Port, the Multiplexor bus, and finally the micro-bus.

Refer to the Model 5/16 User´s Manual, Publication 29-588, for operation and timing information on the micro-bus.

3.9.5.4 Serial Port. The logic for the Serial Port is found on Sheet 4 of the micro-bus adapter Functional Schematics, 35-658D08.

The Serial Port is a serial, 20 milliampere current loop, interface which is operational between the limits of 100 to 2400 baud. The baud rate is generated by the free running oscillator (4H9) and is normally divided by 64 by the Asynchronous Communications Interface Adapter (ACIA) (4C8) device. The ACIA is the heart of the Serial Port and is responsible for the parallel to serial and serial to parallel conversion. Besides data registers, this device contains both a command register and a status register. Refer to Appendix for further information about the ACIA.

The Serial Port is hard wired for Address X`C0´ (4D2). The decoding of this address enables the ACIA (CSF0) and is used to enable the 3 to 8 decoder (4G2). The outputs of this decoder are used to present further information to the ACIA and is used by the remaining logic to steer the data multiplexors and enable the drivers and receivers to the processor´s I/O bus.

3.9.6 Memory, Memory Timing, and Control

3.9.6.1 RAM/ROM. The 5/16 has a minimum of 8K bytes of tri-state output dynamic Random Access Memory (RAM) (Sheet 3) that can be expanded to a maximum of 64K bytes with RAM or ROM. Each memory chip is organized as a 4096 one-bit word and each word is identified by a 6-bit row address and a 6-bit column address. These addresses are multiplexed and loaded into the chip with corresponding row and column strobes. A write signal must be enabled for data to be stored in dynamic RAM. Refresh of dynamic RAM is performed by executing a memory cycle to every row within each 2-millisecond interval. The memory chips are configured to provide a 16-bit parallel data path into and from memory.

Signals AD00:50 (Sheet 3) are the multiplexed address input to the memory. The Row Address Strobe (RASX0) is enabled when AD00:50 hold the row address and the Column Address Strobe (CAS) is enabled when AD00:50 hold the column address. Chip Select (CSX0), when active, selects the memory that is to respond to the strobes and control signals. When a micro-instruction specifies Memory (LMEM1) as the destination, the B Bus is gated into MD001:MD151, and Write (WTX0) allows this data to be stored in the accessed location. On a memory read, WTX0 inactive, the contents of the accessed location outputs to MS001:151.

3.9.6.2 Memory Timing. All memory cycles (instruction read, memory read/write, or refresh) are under microprogram control. The Memory Timing flip-flops, FMEM, FREF1, FRAS, FXRAS, FCAD, FCAS (Sheet 12) are all in the reset state when no memory cycle is in progress. Signal OSC0 is the clock signal for these flip-flops, and memory timing signals are generated in synchronization with the Processor clocks. A specified instruction read, memory read, or memory write by a micro-instruction activates the Memory (MEM1) line. At the end of State 0 (Figure 3-12) of the machine cycle, the Memory flip-flop (FMEM) is toggle set by the falling edge of OSC0 and the D-input of FRAS, Row Address Strobe, and FREF, Refresh flip-flops, are enabled. If a Refresh is specified (RFRSH1), the D inputs of FRAS and FREF are enabled when CLK1 goes active. The remaining D flip-flops of Memory Timing are set successively by the rising edges of OSC0. FRAS1 controls the strobe for the Row Address and FCAS1 that of the Column Address. The Auxiliary RAS, FXRAS, delays for two OSC0 periods the setting of the Column Address flip-flop (FCA0) which selects the Column Address. FREF set Enables Refresh (ERFRSH0) which activates the Row Address strobe lines RAS.

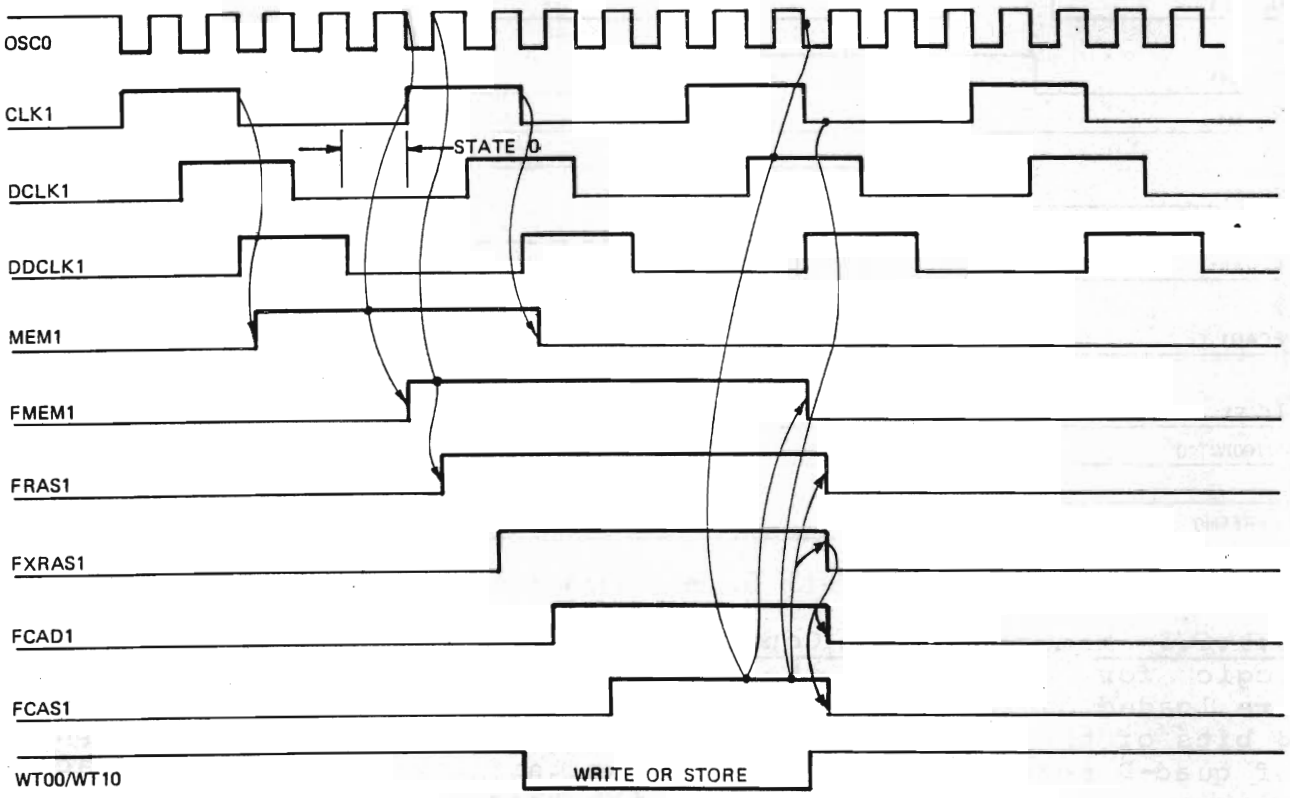


Figure 3-12. Memory Timing

The next DCLK1 after FCAS is set enables the K-input of FMEM which is reset by the first low-going edge of OSC0. This edge of OSC0 also drives CLK0 high to direct clear FRAS and FXRAS. The remaining flip-flops, FCAD and FCAS, are held cleared by FXRAS. The cleared FRAS removes the high D input of FREF which resets on a OS0 going high.

If a Memory Write (DMW0) is specified, the Write lines WT00 and WT10 (Sheet 2) are enabled on the trailing edge of CLK0. The data written is that presented in MD001:151 from the B Bus by

LMEM1 (Sheet 3). For instruction or memory read, the contents of the accessed memory location are valid on MS001:151 before the end of the CLK pulse after FCAS1 goes active.

If the micro-instruction specifies Refresh (REFRESH0) (Sheet 10) and if a Refresh is to be executed, RFRSH1 (Sheet 12) is active (Figure 3-13) rather than MEM1. FMEM does not set for refresh. The D-input of FRAS and FREF is enabled by RFRSH1 and CLK1, during which the first positive-going transition of OSC0 sets FRAS and FREF. The memory timing proceeds as described above. Note that with FMEM inactive and FREF1 active, Enable Refresh (EFRSH0) is activated.

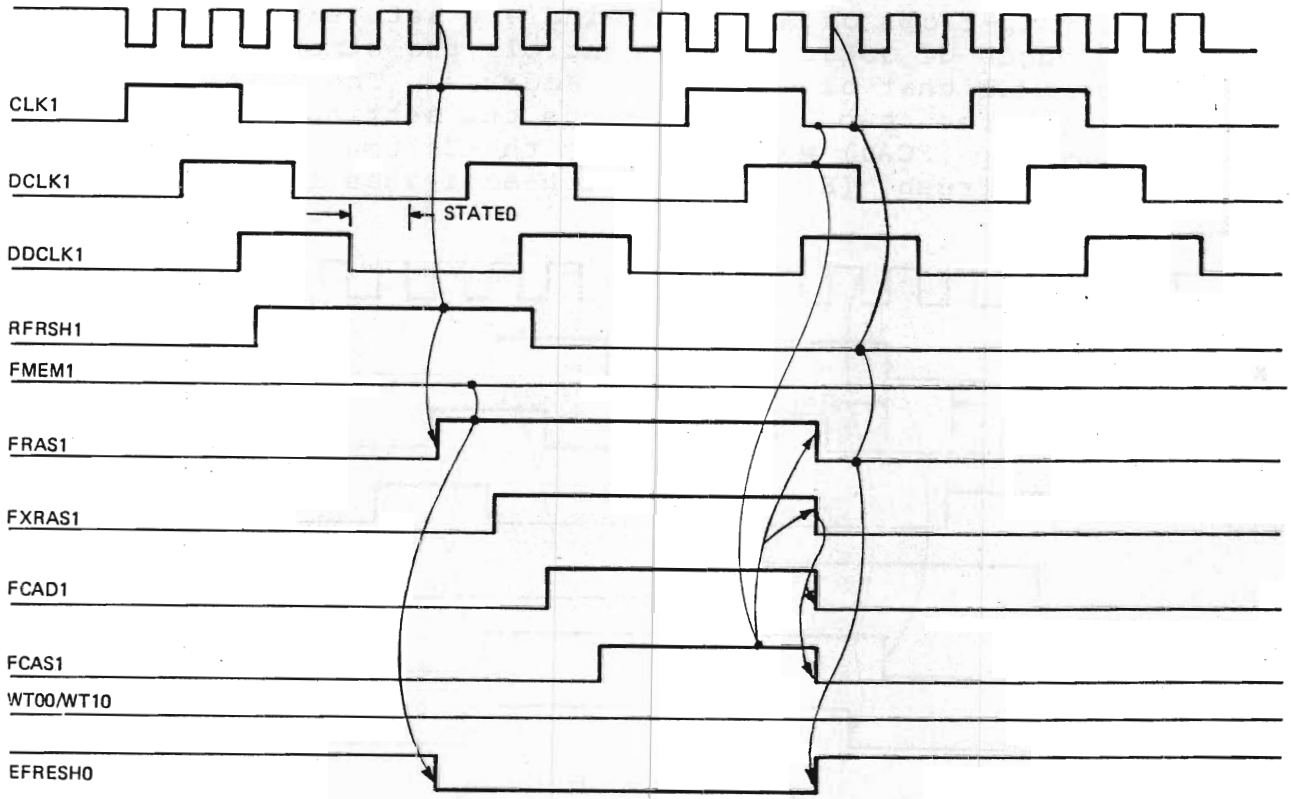


Figure 3-13. Refresh Cycle Memory Timing

3.9.6.3 Memory Address Control. Sheet 2 contains the control logic for addressing the memory. The Memory Address Registers are loaded on the trailing edge of DDCLK1. The most significant 8 bits of the memory address are loaded from B001:071 into a pair of quad-D registers, and the least significant bits are loaded either from B081:141 or from the Refresh Counters, RAD001:051 into a pair of 2:1 multiplexors with storage whose Write Select (WS) is controlled by the Refresh signal, RFRSH1. The memory row address, B091:141 or RAD001:051, of the Memory Address Registers is multiplexed with the column address, B031:B81 in the address multiplexors which are controlled by FCAD1 of the memory Timing. Memory Address Drivers buffer the output of the address multiplexors to AD00:50 for the memory. Row Address Stobe, RASX0, is decoded from the three most significant bits of the Memory Address Registers corresponding to B001:B021, FRAS1 and Enable Refresh, EFRSH0. Column Address Strobe CASX0, is a function of FCAS1 and EFRSH0. Chip Select, CSX0, is strapped to ground.

The Refresh counter is made from a pair of 4-bit counters which are incremented by the Refresh Clock RFCLK0. The Refresh Clock is a voltage-tapped buffered output of the free running 30 us oscillator.

On power up or initialize, SCLR0A directly clears the Refresh Counter, the Write flip-flop, FWT, and directly sets the Power Up (FPWRUP) and Refresh (FRFSH) flip-flops. In addition, the ROM Address Register of Sheet 5 is forced to X`000´. When SCLR0A is removed, the microprogram recognizes the FPWRUP1 generated interrupt and branches to and remains in the loop while all rows of memory are refreshed or precharged; i.e., until FPWRUP1 goes inactive. On refresh, only a row address and its strobe are transmitted to the RAM.

With FRFSH set, the rising edge of CLK0 sets the Refresh pending flip-flop (FRFCY). A decoded micro-instruction RFRESH0, I/O Stop (IOSTOP0), or an active FTIT0 enables RFRSH1. This signal enables the RAD001:051 outputs of the Refresh counters to be loaded into the Memory Address Registers on the falling edge of DDCLK1. The address of the row to be refreshed is gated through the address multiplexors and the Memory Address Drivers to AD00:50.

The Memory Timing of Sheet 12 proceeds, as described above, for a refresh cycle. The Enable Refresh signal is activated by FREF1 and FMEM0. EFRSH0 enables RASX0, disables CASX0 and direct clears FRFRSH and FRFCY. The accessed row is refreshed and the microprogram remains in the refresh loop as long as FPWRUP1 is active.

When RFCLK0 increments the Refresh counters, it also sets FRESH. CLK0 sets FRFCY and a decoded RFRESH0 initiates a refresh of the next row of RAM. The microprogram exits from the power up loop when the MSD bit of the Refresh counter goes active and resets FPWRUP.

For refresh, other than power up or initialize, a decoded RFRESH0 generates RFRSH1 only if FRFCY is set. If RFRSH1 is generated the row defined by the Refresh Counters is accessed. If RFSH1 is not activated, a refresh is not executed. In either case, whether or not RFRSH1 is active, the microprogram continues through its sequence.

If a MEM1 operation is to be performed, RFSH1 is inactive and on the trailing edge of DDCLK1 the Memory Address Registers are loaded from the B Bus, B001:151. With the Column Address flip-flop (FCAD) still reset the row address bits are steered through the address multiplexors to AD00:AD50. FMEM is set at the end of State 0 and inhibits DDCLK1 from altering the Memory Address Registers. As described previously, FRAS1 is activated and gates the decoded RASX0 lines. Two OSC0 periods later, FCAD1 goes high and selects the column address to be transmitted to AD00:AD50. FCAS1 clock gates CASX0 one OSC0 period after FCAD1.

For a memory write, DMW0, the Write flip-flop, FWT, toggles on the trailing edge of CLK0. On this edge the next micro-instruction specifies a load memory, LMEM1, which gates the B Bus, B001:151, into the RAM. Also from this CLK0 edge, for an instruction or memory read, the content of the accessed memory location is valid on MS001:151 for use on the following CLK0 trailing edge.

Note that all signals tied to A and B connectors in the schematics are for use by the extended memory option.

3.9.7 N5 Supply.

The 30 us OSC (Sheet 2) is the source of the switching signal for the N5, (-5V) switching power supply. When the output of the 30 us OSC is low, capacitors C114, 115, 116 are charged from P12 through transistor Q5, and diodes D6 and D7. A high 30 us OSC output cuts off Q5, and C114, 115, and 116 charge C 118 through Q4 and D8. The voltage across C118 causes the 5.1V zener Diode, D5, to conduct through Resistor R107 to generate N5.

Both P12 and N5 are monitored by the Over Voltage Protect circuit (Sheet 2). When P12 and N5 are in their normal operating range, Q6 and Q7 are non-conducting. D4, a 5.1V zener diode, conducts from P12 through R113 and maintains the emitter of Q6 at 5.1V. If P12 or N5 increase and drive Q6 into conduction, Q7 starts to conduct and triggers D9, a silicon control rectifier to clamp P12.

3.10 TURNKEY CONSOLE

This panel (Figure 3-11) contains the key switch (OFF, ON, LOCK), the Initialize switch (INIT), the Execute switch (EXE), and the Enable/Disable switch. In addition, it has a Power and a Fault indicator.

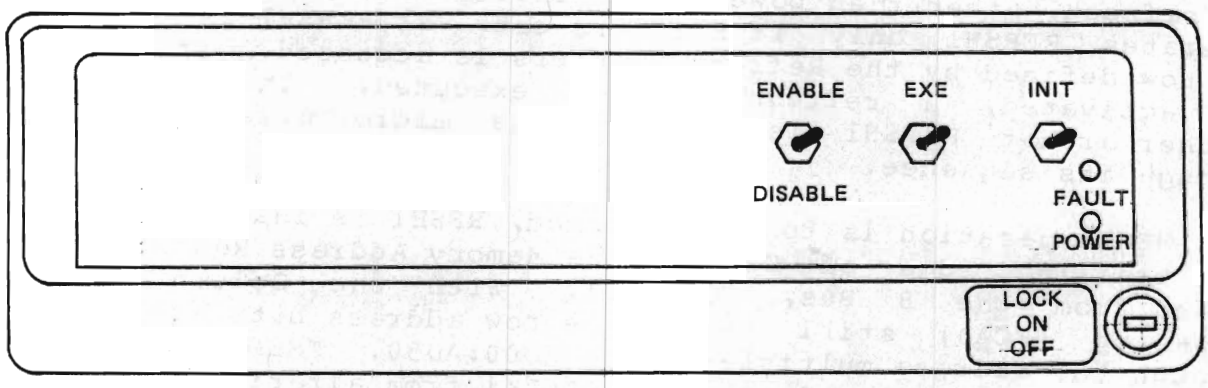


Figure 3-14. Model 5/16 Turnkey Console

In the OFF position, the key switch primary power and power indicator are OFF. (P12 volts is supplied to the CPU with the key in the OFF position. P12 is removed by placing the A.C. power switch on the power supply to the OFF position.) In the ON position, the primary power and power indicator are ON and the INIT, EXE, and ENABLE/DISABLE switches are enabled. In the LOCK position, the primary power and indicator are on but INIT and EXE are disabled.

The INIT is a momentary toggle which initializes the Processor and forces the microprogram through a power up sequence. Operation of INIT causes PFDT0 (Sheet 11) to de-energize the SCLR0 relay.

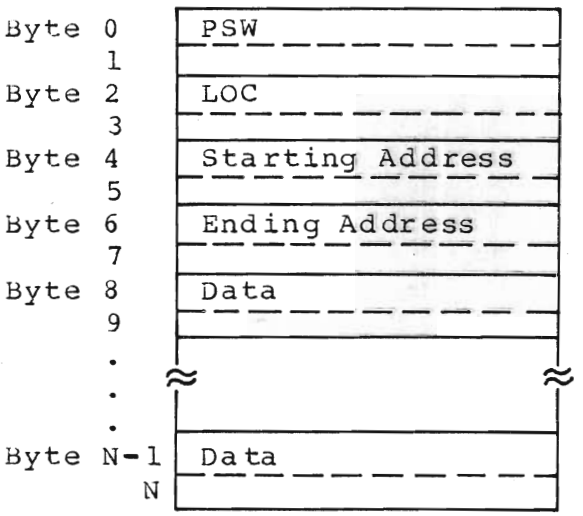
EXEC controls Set/Reset Console Attention (SCATN0, RCATN0), Sheet 12, to set/reset a flip-flop. Console Attention, (CATN1), is generated on the rising edge of CLK0 when EXE is operated. ENABLE/DISABLE controls the Special Attention flip-flop FSPATN, Sheet 12. In the ENABLE position, the clock input to FSPATN is enabled and in the DISABLE position, inhibited.

The FAULT indicator is lit if the Processor fails to pass its micro-diagnostic program. The lamp is lit by SCLR0A. Successful completion of the diagnostics, LPSW0, extinguishes it.

3.11 AUTOMATIC LOADER OPTION (Sheet 11)

The Automatic Loader Option (ALO) contains from 1K to 2K bytes of ROM which provides a means of loading a user program into RAM on power up or initialize. The ALO is a byte device connected to the I/O Multiplexor Bus.

On power up or initialize, the ALO is selected or addressed and the eleven-bit ALO address register is cleared by SCLR0A. When the ALO Enable line, ALEN1, (Sheet 10) is detected, the microprogram branches to unload the ALO. The contents of the addressed ALO ROM location are gated to the multiplexer bus (D080:150) by FCIN1 and the ALO address register is incremented when FCIN0 is deactivated. The data format of the ALO ROM is as follows:



The microprogram continues to read the ROM until all data between the starting and ending addresses are loaded into the RAM.

The ALO is deselected whenever an I/O device is addressed (ADRS0).

3.12 MAINTENANCE

This section describes maintenance procedures which may be used to check and, if necessary, adjust the Processor.

Capacitor C107 of the LC oscillator is adjusted for a CLK1 period of 300 nanoseconds. If the optional serial Port feature is equipped, adjust variable resistor R16 on the micro-bus adapter for the frequency corresponding to the Baud Rate of the device being used (CLK1-TPA). Frequency = 64 x Baud Rate. (Refer to Sheet 1 of 35-638 for example settings.

Use the 06-215 and 06-216 Model 5/16 Processor Test Parts I and II and either 06-213 or 06-214 5/16 MOS Memory Tests to perform a comprehensive test of the i/16 Processor.

CHAPTER 4
TEST AID OPERATION AND MAINTENANCE

4.1 INTRODUCTION

This chapter describes the operation and maintenance of the M49-410 Test Aid (02-276) and the associated logic in the processor. Refer to 02-276D08 for schematics of the M49-410 Test Aid.

4.2 INSTALLATION AND POWER

Refer to Chapter 2 for installation information.

4.3 GENERAL DESCRIPTION

The Test Aid consists of a switch display panel and a 17-283 logic card which attaches to the 35-637 5/16 Processor board.

The Test Aid provides the ability to examine the address of the micro-code and to stop processor clocks at option.

4.4 OPERATION

Refer to Figure 4-1 during the operating description. The 12 Light-Emitting Diodes (LEDs) numbered 4:15 display the contents of the ROM Address Register (RAR). The numbers assigned to the LEDs correspond to the ROM Address Register bits. The 12 toggle switches labelled 4:15 provide the ability to set up a match address. The Test Aid logic stops the processor clocks when the selected "match address" is in the ROM Address Register and the Address Match (ADR MATCH) switch is in the ON (up) position.

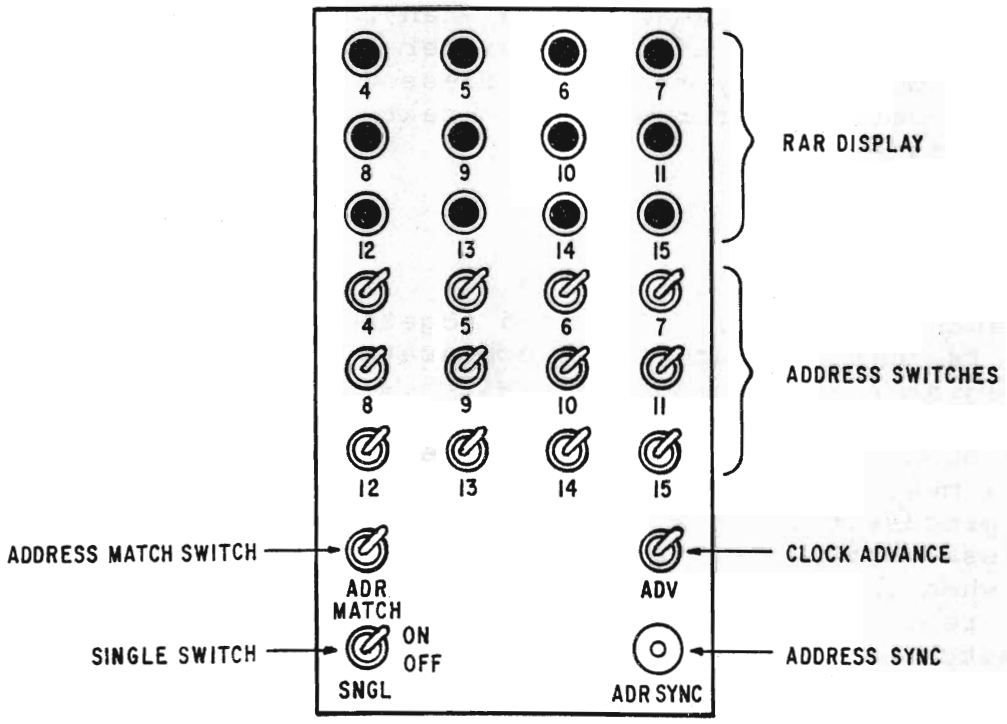


Figure 4-1. Test Aid Switch Panel

4.4.1 Address Match Switch

After selecting an address on the Address switches, place the Address Match (ADR MATCH) switch in the ON (up) position. When the ROM Address Register of the processor contains the "match address," the processor clocks are stopped on the next clock. The Address Match switch feature can also be used to interrupt and continue micro-code loops. Follow the procedure for address matching. Select an address within a micro-code loop. Once the match has been found, depressing the Clock Advance (ADV) switch once allows the micro-code to go through the loop and match on the selected address again.

4.4.2 Clock Advance Switch

The Clock Advance switch allows the processor to generate one clock each time it is depressed when the Address Match or Single (SNGL) switch is in the ON (up) position.

4.4.3 Single Switch

When the Single switch is in the ON (up) position, the processor clocks are stopped. With this switch ON, the micro-program may be executed, one micro-instruction at a time, by depressing the Clock Advance Switch.

4.4.4 Address Sync

Address Sync (ADR SYNC) is a BNC connector whose output is a low going signal that becomes active when the Address switches and the contents of the ROM Address Register compare. The contents of the ROM (specified by the ROM Address REgister) are not loaded into the ROM Data Register until the next Clock which loads the ROM Data Register.

4.4.5 Option

Pins `A´ and `B´ are normally wired together (see Figure 4-2). Pin `A´ is the output of a comparator that compares the ROM Address Register and the Address switches. When they compare, the signal on Pin A goes high (+5 VDC), causing the processor clocks to stop. Removing the wire between Pins `A´ and `B´ provides a means to bring in any high active signal on Pin `B´ to stop the processor clocks. To match on any high active signal, the Address Match switch must still be placed in the ON (up) position when a match is desired. Removing the wire between `A´ and `B´ removes the capability to stop the processor clocks on address match.

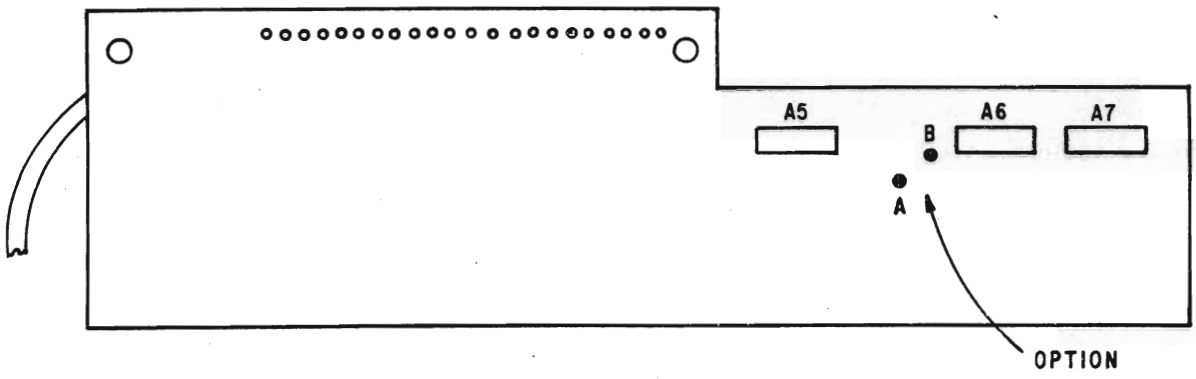


Figure 4-2. Option Connections

4.5 TEST AID MAINTENANCE

This section defines timing sequences (Figure 4-3) in the logic of the Test Aid and associated logic in the processor. Refer to the processor functional schematic and the clock control sheet for logic detail of the clock stop. See Figure 4-3.

4.6 MNEMONICS

ADRMCH1 - This signal is active when the contents of the ROM Address Register and the Address switches are equal.

ADVC0 - Flip-flop output, which goes active when the ADV switch is depressed, inactive when the ADV switch is released.

BCLK0 - Derived from the processor. This is a clock that cannot be stopped by any clock stop in the processor. BCLK0 width is typically 60 nanoseconds and the period is typically 250 nanoseconds.

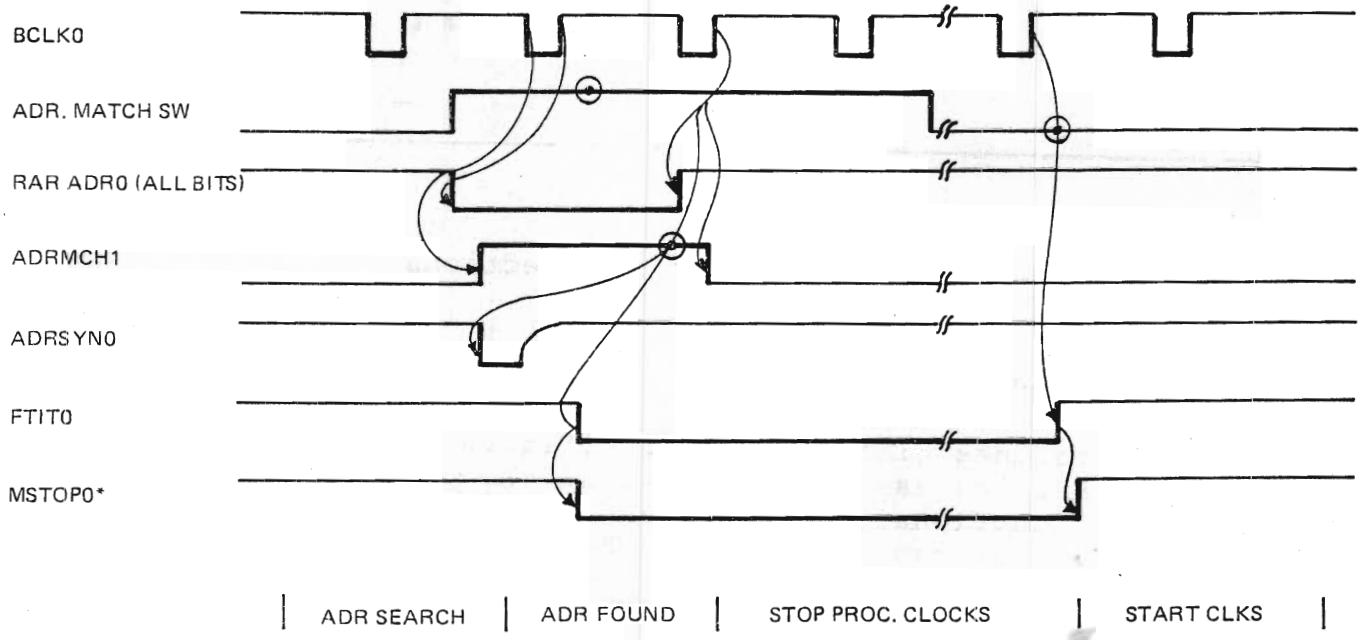
FADV0 - When active, allows FTIT0 to be inactive for one clock period. If ADVC0 and BCLK0 are active at the same time, the FADV0 flip-flop sets.

FTIT0 - This flip-flop is reset by Single switch ON, Address Match switch ON, and a match address.

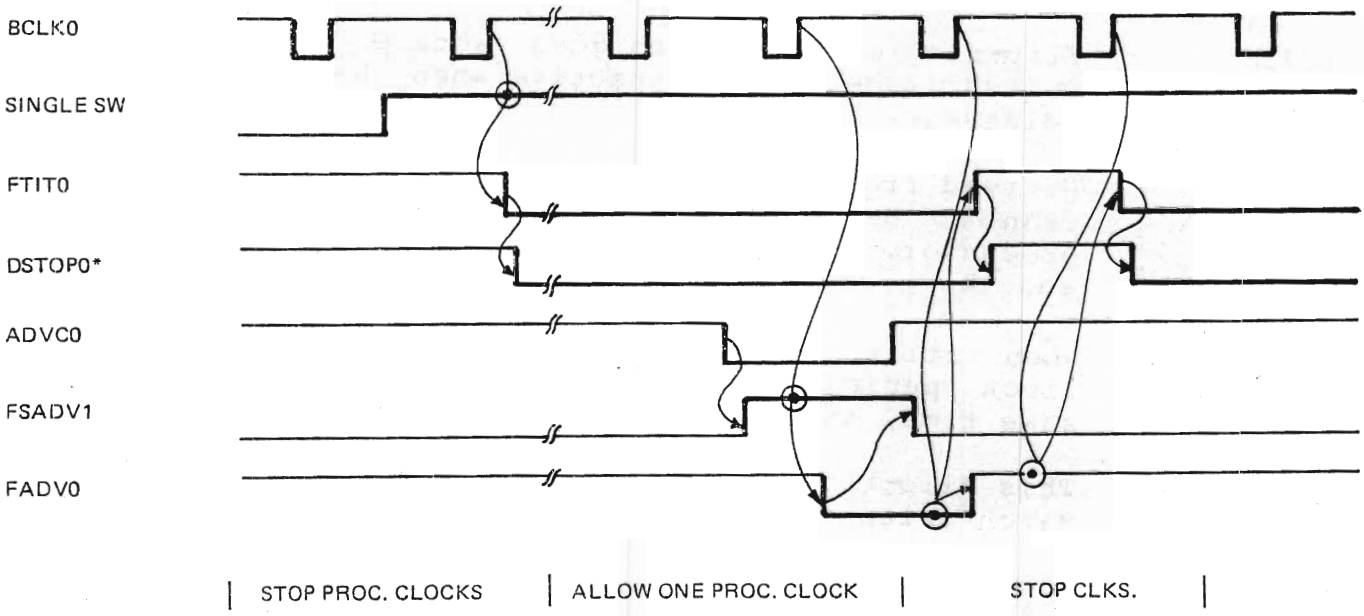
MCH04-150 - When active, indicates that a particular address switch has been selected.

RAR04 150 - ROM Address Register outputs which indicate the address of the micro-instruction to be executed on the next clock.

TIMING CHART FOR ADDRESS MATCH



TIMING CHART FOR SINGLE STEPPING



* DSTOP0 IS CLOCK STOPPING SIGNAL INTERNAL TO THE PROCESSOR
WHEN ACTIVE ALL PROCESSOR CLOCKS EXCEPT CLK1, DCLK1 AND DDCL1 ARE STOPPED.

Figure 4-3. Test Aid Timing

APPENDIX 1
GLOSSARY OF ABBREVIATIONS AND ACRONYMS

ADR	Address
ALO	Automatic Loader
ALU	Arithmetic Logic Unit
C	Carry
CC	Condition Code
DROM1	Decoder Read Only Memory 1
DROM2	Decoder Read Only Memory 2
FLR	Flag Register
G	Greater Than
IR	Instruction Register
L	Less Than Zero
LOC	Location Register
MAR	Memory Address Register
MDR	Memory Data Register
MR0	Micro Register
MS	Memory Sense
MUX	Multiplexor
OP	User Operation Code
PSW	Program Status Word
RAM	Random Access Memory
RAR	ROM Address Register
RD	ROM Data Register
RI	Register Immediate
ROM	Read Only Memory
RX	Register-to-Index
V	Overflow
YD	User Destination
YS	User Source

APPENDIX 2
MNEMONICS LIST

MNEMONIC	SIGNAL ORIGIN	SIGNAL NAME
A0	4C1	Selects YD or YS for A Port of 4-bit Slice Chip
ACK0	9D9	Acknowledge
AD00:AD60	2L5:2N5	Multiplexed Address bits for Dynamic Memory
ADRS0	9E9	Address Control Line
AMOD1	7L8	Address Modification
B0	4D1	Selects YD or YS for B Port of 4-bit Slice Chip
B001:B151	8L1:8L8	B Bus
BCLK1	12N6	Buffered CLK1
BRANCH0	10B4	Branch decoded
CAS00:CAS10	2J6	Column Address Select
CATN0	12D4	Console Attention Request Line
CKRD1	12N7	ROM Clock
CL070	11L5	Control line 7 from Multiplexor Bus
CLFLR0	10B9	Clear Flag Register
CLK0	12N5	Processor Clock
CLK1	12N5	Processor Clock
CLYD0	10G4	Clear YD
CMD0	9D9	Command Control Line
CS1	10D9	Cross Shift
CN1	7C5	Carry into ALU

MNEMONIC	SIGNAL ORIGIN	SIGNAL NAME
CO1	7B5	Decoded Carry Out
CS10:CS00	2K6	Chip Select
CSEN1	10E9	Cross Shift Enable
D10	10B4	Vector through DROM1
D20	10B4	Vector through DROM2
D000:D150	9A1:9N1	Multiplexed Input/Output Data Bus
DA0	9E9	Data Available Control Line
DACK0	9F9	DMA Acknowledge
DAMOD0	10G4	Address Modification Decoded
DCLK0	12N3	Delayed Clock
DCLK1	12K3	Delayed Processor Clock
DDCLK1	12N4	Clock Delayed from DCLK
DESCLK0	12R7	Destination Clock
DESTP0	12N8	Stop Destination Clock
DI001:DI151	4F9:4L9	Data Input to 4-bit Slice Chip
DIR0	10B4	Decoded Instruction Read
DMW0	10B4	Memory Write Decoded
DR0	9C9	Data Request Control Line
DR081:DR151	5D6	DROM Output
DSTKH0	10N3	Disable Loading High Order of MDR on Cross Shift Operations
DSTKL0	10R3	Disable Loading Low Order of MDR on Cross Shift Operations
DSTOP0	10F6	Destination Clock Stop
ERFRSH	2G6	Enable Refresh

MNEMONIC	SIGNAL ORIGIN	SIGNAL NAME
F1	7A5	Decoded Flag Operation
FAULT0	12D6	Fault, Micro Diognostic Routine not Successfully Completed
FCAD1	12J1	Column Address Flip-Flop
FCAS1	12K1	Column Address Select Flip-Flop
FCIN1	9G9	Control Input Flip-Flop
FDAT1	9J9	Data Flip-Flop to I/O Bus
FLGL0	7H6	Greater than or less than Flag Set
FLR121: FLR151	7E6:7G6	Flag Register Output
FMEM0	12D1	Memory Flip-Flop
FPWRUP1	2B6	Power Up Flip-Flop
FRAS1	12E1	Row Address Select Flip-Flop
FRFRSH0	12G1	Enable Refresh
FSPATN0	12K8	Special Attention Flip-Flop
FTIT0	12J6	Clock Stop from Test Aid
GDDCLK1	2G1	Gated DDCLK
IO0	9J9	Input/Output Operation
IO001:IO151	9B1:9R1	Input/Output Data Lines
IOSTOP0	9L9	Clock Stop for I/O
LDCC0	10C9	Load Condition Code
LDFLR1	10E6	Load Flag Register
LDIO0	10E4	Load I/O
LDPSW0	10E4	Load PSW
LMAR0	10D4	Load Memory Address Register

MNEMONIC	SIGNAL ORIGIN	SIGNAL NAME
LMDR0	10D4	Load Memory Data Register
LMEM0	10E4	Load Memory
LPSW0	10D9	Load Program Status Word
MA021:MA000	2H3	Most Significant Memory Address Register Bits
MAR151	10N3	Memory Address Register Bit 15 used for Cross Shift Operations
MEM1	10A6	Memory Operation Decoded
MD001:MD151	3D2:3S2	Memory Data Input to RAM
MS001:MS151	3D8:3S8	Readout of RAM
MSK0	6D1	Mask
NMI	12G8	Non Masked Interrupt
PSW001: PSW151	6C3:6C7	Program Status Word Bits
QLIQR01	7B5	Shift Q Left In, Shift Q Right Out
QLOQR11	7B5	Shift Q Left Out, Shift Q Right In
RAD01:RAD61	2B3:2D3	Refresh Address Bits
RAR060: RAR150	5N2:5N8	ROM Address
RAR121: RAR151	5K1	ROM Address
RAS00:RAS10	2G6	Row Address Select
RD001:RD231	6L3:6L7	ROM Output
RFCLK0	2K8	Refresh Clock
RFRESH0	10G4	Refresh decoded
RFRSH1	2G7	Refresh pending

MNEMONIC	SIGNAL ORIGIN	SIGNAL NAME
SAT0	10L4	Special Attention Decoded
SB131	9N9	Set B-Bus Bit 13 on False Sync from I/O on Status Request
SCLR0	11N9	System Clear
SHCRY1	7B5	Shifted Carry
SLISR01	7B5	Shift Left In, Shift Right Out
SLOSRI1	7C5	Shift Left Out, Shift Right In
SR0	9B9	Status Request Control Line
SV0	7F6	Set Overflow
TACK0	9C9	Transmit Acknowledge
UIO0	10J4	Unload I/O
UMDR0	10J4	Unload MDR
UMEM0	10J4	Unload Memory
WT00:WT10	2D4	Write Control Line for RAM
WT1	2D4	Write Control Line for Memory Expansion
YD01:YD31	7N8	User Destination Register Output
YDCRY0	7R5	Carry from User Destination Register
YDM10	10G4	Decrement YD
YDP10	10G4	Increment YD
YS01:YS31	7J8:7K8	User Source Register Output

```
MODEL 5/16 MICROCODE 05-064R01 A13                    PAGE   1

PROG= 05.06401     ASSEMBLED BY MICROCAL II  (32-BIT)        4/21/77

                                1          SCRAT                                                    51600020
                                2          CROSS                                                    51600030
                                3          SOCHK                                                    51600040
                                4     * COPYRIGHT INTERDATA INC.  APRIL,  1977                      51600050
                                5     *                                                             51600060
                                6     * IRA GABBERT                                                 51600070
                                7     *                                                             51600080
                                8          TARGT 5/16                                               51600090


                               10     PAGE0.1  PARTS 19-186R00F14,19-186R00F15,19-186R01F16 *     R01  51600110
                               11     PAGE2.3  PARTS 19-186R00F17,19-186R00F18,19-186R01F19 *     R01  51600120
                               12     *                                                             51600130
                               13     *                                                             51600140
                               14     * IN ALL CASES WHERE A BRANCH OR TRANSFER COULD OCCUR TO A     51600150
                               15     * LISTING PAGE OTHER THAN THE CURRENT LISTING PAGE, THE TARGET 51600160
                               16     * PAGE NUMBER IS SHOWN IN PARENTHESIS IN THE COMMENT FIELD.    51600170
                               17     *                                                             51600180
                               18     *                                   ON POWER-UP, INITIALIZE, OR ON  51600190
                               19     *                                   INSTRUCTION READ, MICROCODE     51600200
                               20     *                                   EXECUTION BEGINS AT ROM LOCATION 51600210
                               21     *                                   X'000'.                         51600220
                               22     *                                                                   51600230
 000      68 1000              23     START    BT     ATN+DMA+CATN+PWRUP,INTERUPT LEAVE IF INTERRUPT (P.13) 51600240
                               24     *                                   LOC HAS BEEN INCREMENTED BY 2   51600250
 001      28 3826              25              I      YDA&MR0,YD,D1+REFRESH LOAD YD TO ITSELF; S BUS GETS YS 51600260
                               26     *                                   MR0 = SECOND OPERAND IF RR      51600270
                               27     *                                   MR0 = INDEX REGISTER IF RI OR RX 51600280
                               28     *                                   VECTOR THROUGH DROM 1           51600290


 0002                          30     RX       EQU    *                   COMMON DROM 1 ENTRY POINT       51600310
                               31     *                                   FOR RX FORMAT INSTRUCTIONS      51600320
 002      A4 6C60              32              A      LOC,LOC,Q,MR        ADDRESS AND FETCH SECOND        51600330
                               33     *                                   HALFWORD OF INSTRUCTION. LOC    51600340
 003      04 7830              34              L      MR0,MEM             GETS LOC+2.  MR0 = A-FIELD.     51600350
 004      04 5845              35              A      MR0,MR0,X2          IF AMOD, INCREMENT MR0 BY (X2)  51600360
                               36     *                                   IF NO AMOD, MR0 IS UNCHANGED    51600370
 005      A4 7A40              37              L      MAR,MR0,MR          FETCH SECOND OPERAND            51600380
 006      44 7830              38              L      MR0,MEM,D2          COPY TO MR0, VECTOR THRU DROM 2 51600390


 0007                          40     RI       EQU    *                   COMMON DROM 1 ENTRY POINT       51600410
                               41     *                                   FOR RI FORMAT INSTRUCTIONS      51600420
 007      A4 6C60              42              A      LOC,LOC,Q,MR        ADDRESS AND FETCH SECOND        51600430
                               43     *                                   HALFWORD OF INSTRUCTION AND     51600440
 008      04 7830              44              L      MR0,MEM             INCREMENT LOC.  MR0=A-FIELD     51600450
 009      44 5845              45              A      MR0,MR0,X2,D2       PERFORM INDEXING IF SPECIFIED   51600460
                               46     *                                   VECTOR THRU DROM 2.             51600470
```

LOGICAL INSTRUCTIONS

```
 000A                          48  LIS     EQU  *          LOAD IMMEDIATE SHORT          * 24 *  51600490
 000A                          49  LHR     EQU  *          LOAD HALFWORD REGISTER        * 08 *  51600500
 000A                          50  LH      EQU  *          LOAD HALFWORD                 * 48 *  51600510
 000A                          51  LHI     EQU  *          LOAD HALFWORD IMMEDIATE       * C8 *  51600520
                               52  *                                                              51600530
 00A     0C 704E               53          A    YD,MR0,NULL,F+CO                               51600540
 00B     E4 6C60               54          A    LOC,LOC,Q,IRJ      FETCH NEXT,INCREMENT LOC    51600550
                               55  *                                                              51600560
                               56  *                  COMMON DROM1 ENTRY FOR LIS,AIS,SIS          51600570
 00C     44 7820               57  SHORT   L    MR0,YSI,D2         MR0 GETS R2 FIELD           51600580
                               58  *                                                              51600590
 000D                          59  LCS     EQU  *          LOAD COMPLEMENT SHORT         * 25 *  51600600
                               60  *                                                              51600610
 00D     44 F820               61          S    MR0,NULL,YSI,D2    2'S COMP OF N, GO TO LH     51600620
                               62  *                                                              51600630
 000E                          63  LM      EQU  *          LOAD MULTIPLE                 * 01 *  51600640
                               64  *                                                              51600650
 00E     04 6A56               65          A    MAR,MAR,Q,REFRESH  MR0=VALUE TO LOAD, BUMP MAR  R01  51600660
 00F     0C 7042               66          L    YD,MR0,YDP1        LOAD ONE, INCREMENT R1 FIELD  51600670
 010     77 01D0               67          BT   YDCARY,EXIT1       DONE WHEN LOAD R15            51600680
 011     A4 7A50               68          L    MAR,MAR,MR         FETCH NEXT                    51600690
 012     44 7830               69          L    MR0,MEM,D2         COPY TO MR0, LOOP THRU DROM2 TO LM  51600700
                               70  *                                                              51600710
                               71  *                                                              51600720
                               72  *                                                              51600730
                               73  *                                                              51600740
 013     00 0000               74          DC   0          FILLER                                 51600750
                               75  *                                                              51600760
                               76  *                  COMMON DROM 1 ENTRY POINT FOR RX            51600770
                               77  *                  FORMAT INPUT/OUTPUT INSTRUCTIONS            51600780
 014     04 3021               78  RXIO    ADR  YD         ADDRESS THE DEVICE                     51600790
                               79  *                                                              51600800
 0015                          80  RXBYTE  EQU  *          COMMON DROM ENTRY POINT FOR RX         51600810
                               81  *                       BYTE HANDLING INSTRUCTIONS             51600820
 015     A4 6C60               82          A    LOC,LOC,Q,MR       ADDRESS AND FETCH SECOND      51600830
                               83  *                       HALFWORD OF INSTRUCTION.  LOC          51600840
 016     04 7830               84          L    MR0,MEM            GETS LOC +2, MR0=A-FIELD      51600850
 017     04 5845               85          A    MR0,MR0,X2         IF AMOD, INCREMENT MR0 BY (X2)  51600860
                               86  *                       IF NO AMOD, MR0 IS UNCHANGED           51600870
 018     A4 7A40               87          L    MAR,MR0,MR         FETCH SECOND OPERAND           51600875
 019     44 7E30               88          L    MDR,MEM,D2         COPY TO MDR, VECTOR THRU DROM 2  51600876
                               89  *                                                              51600880
                               90  *                                                              51600890
 001A                          91  LB      EQU  *          LOAD BYTE.                    * 03 *  51600900
                               92  *                                                              51600910
 01A     04 78F0               93          L    MR0,MDR,CS         POSITION APPROPRIATE BYTE     51600920
                               94  *                                                              51600930
 001B                          95  LBR     EQU  *          LOAD BYTE REGISTER            * 93 *  51600940
                               96  *                                                              51600950
 01B     0C 7040               97          L    YD,MR0             LOAD LOW BYTE                 51600960
 01C     0E 51FF               98          NT   YD,'FF',YD         CLEAR HIGH BYTE               51600970
 01D     04 7410               99  EXIT1   L    FLR,PSW            NO CHANGE TO CONDITION CODE   51600980
 01F     E4 6C60              100          A    LOC,LOC,Q,IRJ      FETCH NEXT, INCREMENT LOC     51600990
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LOGICAL INSTRUCTIONS

```
 001F                          102   EXBR    EQU   *                    EXCHANGE BYTE REGISTER      * 94 *  51601010
                               103   *                                                                       51601020
 01F     4C 70C0               104           I     YD,MR0,CS+D2         GO TO EXIT1 (P.2)                   51601030
                               105   *                                                                       51601040
 0020                          106   STH     EQU   *                    STORE HALFWORD              * 40 *  51601050
                               107   *                                                                       51601060
 020     04 3E20               108           L     MDR,YD               DATA TO MDR                         51601070
 021     84 7A40               109           I     MAR,MR0,MW           EFFECTIVE ADDRESS TO MAR            51601080
 022     04 7670               110           I     MEM,MDR              DO STORE                            51601090
 023     7B 81D6               111           B     EXIT1,REFRESH        EXIT1 (P.2)                 R01     51601100
                               112   *                                                                       51601110
 0024                          113   STM     EQU   *                    STORE MULTIPLE              * 00 *  51601120
                               114   *                                                                       51601130
 024     04 3E20               115           L     MDR,YD               MDR = REGISTER TO STORE             51601140
 025     84 7A40               116           I     MAR,MR0,MW           LOAD EFFECTIVE ADDRESS              51601150
 026     04 7672               117           L     MEM,MDR,YDP1         STORE IT; BUMP R1 FIELD             51601160
 027     77 01D6               118           BT    YDCARY,EXIT1,REFRESH LEAVE IF CARRY (P.2)        R01    51601170
 028     44 6840               119           A     MR0,MR0,Q,D2         INCREMENT ADDRESS, LOOP BACK TO STM 51601180
                               120   *                                                                       51601190
 0029                          121   STB     EQU   *                    STORE BYTE                  * D2 *  51601200
                               122   *                                                                       51601210
 029     04 3820               123           L     MR0,YD               MR0=HIGH/LOW BYTE PAIR              51601220
 02A     04 7EC0               124           L     MDR,MR0,CS           PROPER BYTE TO MDR                  51601230
 02B     84 7A50               125           I     MAR,MAR,MW           LOAD EFFECTIVE ADDRESS              51601240
 02C     04 7670               126           L     MEM,MDR              DO STORE                            51601250
 02D     7B 81D6               127           B     EXIT1,REFRESH        EXIT1 (P.2)                 R01     51601260
                               128   *                                                                       51601270
 002E                          129   STBR    EQU   *                    STORE BYTE REGISTER         * 92 *  51601280
                               130   *                                                                       51601290
 02F     08 3E20               131           L     YDA&MDR,YD           YD=YD; MDR GETS YS                  51601300
 02F     04 7B01               132           LT    MAR,1                FORCE ODD BYTE SELECTION            51601310
 030     04 3EA0               133           L     MDR,YD,CS            MODIFY LS BYTE                      51601320
 031     0C 7270               134           I     YS,MDR               LOAD RESULT                         51601330
 032     7B 81D6               135           B     EXIT1,REFRESH        EXIT1 (P.2)                 R01     51601340
                               136   *                                                                       51601350
 033     04 7500               137   CR1     LI    FLR,0                FROM ARITHMETIC COMPARE             51601360
                               138   *                                                                       51601370
                               139   *                                                                       51601380
 0034                          140   CLHR    EQU   *                    COMPARE LOGICAL HW REGISTER * 05 *  51601390
 0034                          141   CLH     EQU   *                    COMPARE LOGICAL HALFWORD    * 45 *  51601400
 0034                          142   CLHI    EQU   *                    COMPARE LOGICAL HW IMMEDIATE* C5 *  51601410
                               143   *                                                                       51601420
 034     04 D64E               144           S     NULL,YD,MR0,F+CO     SUBTRACT TO COMPARE                 51601430
 035     E4 6C60               145           A     LOC,LOC,Q,IRJ        FETCH NEXT INCREMENT LOC            51601440
                               146   *                                                                       51601450
 0036                          147   CLB     EQU   *                    COMPARE LOGICAL BYTE        * D4 *  51601460
                               148   *                                                                       51601470
 036     00 76F0               149           L     Q,MDR,CS             POSITION BYTE                       51601480
 037     06 6FFF               150           NI    MDR,'FF',Q           MASK LS 8 BITS                      51601490
 038     02 57FF               151           NI    Q,'FF',YD            1ST OP BYTE TO Q                    51601500
 039     04 E67E               152           S     NULL,Q,MDR,F+CO      SUBTRACT TO COMPARE                 51601510
 03A     00 7702               153   EXIT1A  LI    Q,2                  RESTORE Q                           51601520
 03B     E4 6C60               154           A     LOC,LOC,Q,IRJ        FETCH NEXT, INCREMENT LOC           51601530
```

LOGICAL INSTRUCTIONS

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 003C                          156   NHR     EQU   *                        AND HALFWORD REGISTER        * 04 *  51601550
 003C                          157   NH      EQU   *                        AND HALFWORD                 * 44 *  51601560
 003C                          158   NHI     EQU   *                        AND HALFWORD IMMEDIATE       * C4 *  51601570
                               159   *                                                                           51601580
 003C    0E 504E               160           N     YD,MR0,YD,F+C0                                               51601590
 003D    E4 6C60               161           A     LOC,LOC,Q,IRJ                                                51601600
                               162   *                                                                           51601610
 003E                          163   OHR     EQU   *                        OR HALFWORD REGISTER         * 06 *  51601620
 003E                          164   OH      EQU   *                        OR HALFWORD                  * 46 *  51601630
 003E                          165   OHI     EQU   *                        OR HALFWORD IMMEDIATE        * C6 *  51601640
                               166   *                                                                           51601650
 003F    0D D04E               167           O     YD,MR0,YD,F+C0                                               51601660
 003F    E4 6C60               168           A     LOC,LOC,Q,IRJ                                                51601670
                               169   *                                                                           51601680
 0040                          170   XHR     EQU   *                        EXCLUSIVE-OR HW REGISTER     * 07 *  51601690
 0040                          171   XH      EQU   *                        EXCLUSIVE-OR HALFWORD        * 47 *  51601700
 0040                          172   XHI     EQU   *                        EXCLUSIVE-OR HW IMMEDIATE    * C7 *  51601710
                               173   *                                                                           51601720
 040     0F 504E               174           X     YD,MR0,YD,F+C0                                               51601730
 041     E4 6C60               175           A     LOC,LOC,Q,IRJ                                                51601740
                               176   *                                                                           51601750
 0042                          177   THI     EQU   *                        TEST HALFWORD IMMEDIATE      * C3 *  51601760
                               178   *                                                                           51601770
 042     06 564E               179           N     NULL,MR0,YD,F+C0                                             51601780
 043     E4 6C60               180           A     LOC,LOC,Q,IRJ                                                51601790
                               181   *                                                                           51601800
                               182   *                                                                           51601810
                               183   *                              COMMON DROM 1 ENTRY POINT FOR               51601820
                               184   *                              HALFWORD SHIFT INSTRUCTIONS                 51601830
 044     A4 6C60               185   SLRH    A     LOC,LOC,Q,MR     FETCH A-FIELD OF INSTRUCTION                51601840
 045     04 7830               186           I     MR0,MEM                                                      51601850
 046     04 5845               187           A     MR0,MR0,X2       PERFORM INDEXING IF SPECIFIED               51601860
 047     00 7640               188           L     Q,MR0            SHIFT COUNT TO Q REGISTER                   51601870
 048     06 690F               189           NI    MR0,'0F',Q       MASK LS 4 BITS                              51601880
 049     45 7847               190           DFCF  MR0,MR0,NULL,D2  DECREMENT WITH FLAGS                        51601890
                               191   *                              VECTOR THRU DROM2 TO SLHL OR SRHL           51601900
                               192   *                                                                           51601910
 04A     45 7827               193   SLRS    DECF  MR0,YSI,NULL,D2  MR0 GETS COUNT MINUS 1                     51601920
                               194   *                                                                           51601930
 004B                          195   SLLS    EQU   *                        SHIFT LEFT LOGICAL SHORT     * 91 *  51601940
 004B                          196   SLHL    EQU   *                        SHIFT LEFT HW LOGICAL        * CD *  51601950
                               197   *                                                                           51601960
 04B     67 0516               198           BT    L,EXIT2,REFRESH  EXIT IF COUNT MINUS (P.5)                  51601970
 04C     1D B02A               199           LSL   YD,YD,C0         PERFORM SHIFT, SET CARRY                    51601980
 04D     45 7847               200           DFCF  MR0,MR0,NULL,D2  DECREMENT COUNT, LOOP THRU DROM2            51601990
                               201   *                                                                           51602000
 004E                          202   SRLS    EQU   *                        SHIFT RIGHT LOGICAL SHORT    * 90 *  51602010
 004E                          203   SRHL    EQU   *                        SHIFT RIGHT HW LOGICAL       * CC *  51602020
                               204   *                                                                           51602030
 04F     67 0516               205           BT    L,EXIT2,REFRESH  EXIT IF COUNT MINUS (P.5)                  51602040
 04F     15 B02A               206           LSR   YD,YD,C0         PERFORM SHIFT                               51602050
 050     45 7847               207           DFCF  MR0,MR0,NULL,D2  DECREMENT COUNT, LOOP THRU DROM2            51602060
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LOGICAL INSTRUCTIONS

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                        209   *                                                    EXIT 2 FOR SLLS,SLHL,SRLS,SRHL          51602080
051     63 8550         210   EXIT2     BT     C,EXIT2A                            BRANCH IF CARRY FROM SHIFT              51602090
052     04 7500         211             LI     FLP,0                               CLEAR FLAGS                             51602100
053     04 362C         212             A      NULL,NULL,YD,F                      ADJUST G & L                            51602110
054     7B 83A0         213             B      EXIT1A                              RESTORE Q THEN EXIT (P.3)               51602120
055     04 7508         214   EXIT2A    LI     FLP,8                               CLEAR FLAGS EXCEPT CARRY                51602130
056     04 362C         215             A      NULL,NULL,YD,F                      ADJUST G & L                            51602140
057     7B 83A0         216             B      EXIT1A                              RESTORE Q THEN EXIT (P.3)               51602150

                        218   *                                                    COMMON DROM 1 ENTRY POINT FOR           51602170
                        219   *                                                    FULLWORD SHIFTS AND ROTATES             51602180
058     7B 9EA0         220   SLRF      B      SLRF1                               (P.20)                                  51602190
                        221   *                                                                                            51602200
                        222   *                                                                                            51602210
                        223   *                                                    COMMON DROM 1 ENTRY POINT FOR           51602220
059     7B A2E0         224   ATBL      B      ATBL1                               ATL AND ABL  (P.22)                     51602230
                        225   *                                                                                            51602240
                        226   *                                                    COMMON DROM 1 ENTRY POINT FOR           51602250
05A     7B A3D0         227   RTBL      B      RTBL1                               RTL AND RBL (P.22)                      51602260
                        228   *                                                                                            51602270
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BRANCH INSTRUCTIONS

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 005B                        230    BTC     EQU  *                    BRANCH ON TRUE CONDITION      * 42 *  51602290
                             231    *                                                                        51602300
 05B      73 C690            232           BF   MASK,NOBRX           NO BRANCH IF FALSE                     51602310
 05C      A4 6C60            233    BRRX   A    LOC,LOC,Q,MR         FETCH A-FIELD                          51602320
 05D      04 7C30            234           L    LOC,MEM              A-FIELD TO LOC                         51602330
 05E      04 5C65            235           A    LOC,LOC,X2           PERFORM INDEXING IF SPECIFIED          51602340
 05F      04 7410            236           L    FLR,PSW              NO CONDITION CODE CHANGE               51602350
 060      E4 6C60            237           A    LOC,LOC,Q,IRJ        FETCH NEXT INSTR, BUMP LOC             51602360
                             238    *                                                                        51602370
 0061                        239    BTCR    EQU  *                    BRANCH TRUE COND. REGISTER    * 02 *  51602380
                             240    *                                                                        51602390
 061      73 C1D6            241           BF   MASK,EXIT1,REFRESH   NO BRANCH IF FALSE (P.2)       R01    51602400
 062      04 7410            242           L    FLR,PSW              NO CONDITION, CODE CHANGE              51602410
 063      E4 6C40            243           A    LOC,MR0,Q,IRJ        FETCH NEXT INSTR, BUMP LOC             51602420
                             244    *                                                                        51602430
 0064                        245    BTBS    EQU  *                    BRANCH TRUE BACKWARD SHORT    * 20 *  51602440
 0064                        246    BTFS    EQU  *                    BRANCH TRUE FORWARD SHORT     * 21 *  51602450
                             247    *                                                                        51602460
 064      73 C1D6            248           BF   MASK,EXIT1,REFRESH   NO BRANCH IF FALSE (P.2)       R01    51602470
 065      05 6C60            249           S    LOC,LOC,Q            DECREMENT LOC BY 2                     51602480
 066      00 7620            250           L    Q,YSI                N FIELD TO Q                           51602490
 067      40 6620            251           A    Q,YSI,Q,D2           Q GETS ZX N FIELD, VECTOR THRU         51602500
                             252    *                                DROM 2 TO BBS OR BFS                   51602510
                             253    *                                                                        51602520
 0068                        254    BFC     EQU  *                    BRANCH ON FALSE CONDITION     * 43 *  51602530
                             255    *                                                                        51602540
 068      73 C5C0            256           BF   MASK,BRRX            BRANCH IF FALSE                        51602550
 069      04 7416            257    NOBRX  I    FLR,PSW,REFRESH      NO CONDITION CODE CHANGE       P01    51602560
 06A      04 6C60            258           A    LOC,LOC,Q            SKIP PASSED A-FIELD                    51602570
 06B      E4 6C60            259           A    LOC,LOC,Q,IRJ        FETCH NEXT INSTR, BUMP LOC             51602580
                             260    *                                                                        51602590
 006C                        261    BFCR    EQU  *                    BRANCH FALSE COND. REGISTER   * 03 *  51602600
                             262    *                                                                        51602610
 06C      73 81D6            263           BT   MASK,EXIT1,REFRESH   NO BRANCH IF TRUE  (P.2)       R01    51602620
 06D      04 7410            264           L    FLR,PSW              NO CONDITION CODE CHANGE               51602630
 06E      E4 6C40            265           A    LOC,MR0,Q,IRJ        FETCH NEXT INSTR, BUMP LOC             51602640
                             266    *                                                                        51602650
 006F                        267    BFBS    EQU  *                    BRANCH FALSE BACKWARD SHORT   * 22 *  51602660
 006F                        268    BFFS    EQU  *                    BRANCH FALSE FORWARD SHORT    * 23 *  51602670
                             269    *                                                                        51602680
 06F      73 81D6            270           BT   MASK,EXIT1,REFRESH   NO BRANCH IF TRUE  (P.2)       R01    51602690
 070      05 6C60            271           S    LOC,LOC,Q            DECREMENT LOC BY 2                     51602700
 071      00 7620            272           L    Q,YSI                N FIELD TO Q                           51602710
 072      40 6620            273           A    Q,YSI,Q,D2           Q GETS 2X N FIELD, VECTOR THRU         51602720
                             274    *                                DROM 2 TO BBS OR BFS                   51602730
                             275    *                                                                        51602740
 073      05 6C66            276    BBS     S    LOC,LOC,Q,REFRESH    LOC MINUS DISPLACEMENT                 51602750
 074      00 7702            277           LI   Q,2                  RESTORE Q                              51602760
 075      04 7410            278           I    FLR,PSW              NO CONDITION CODE CHANGE               51602770
 076      E4 6C60            279           A    LOC,LOC,Q,IRJ        FETCH NEXT INSTR, BUMP LOC             51602780
 077      04 6C66            280    BFS     A    LOC,LOC,Q,REFRESH    LOC PLUS DISPLACEMENT                  51602790
 078      00 7702            281           LI   Q,2                  RESTORE Q                              51602800
 079      04 7410            282           I    FLR,PSW              NO CONDITION CODE CHANGE               51602810
 07A      E4 6C60            283           A    LOC,LOC,Q,IRJ        FETCH NEXT INSTR, BUMP LOC             51602820
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BRANCH INSTRUCTIONS

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 007B                          285    BAL     EQU   *                       BRANCH AND LINK                * 41 *  51602840
 007B                          286    BALR    EQU   *                       BRANCH AND LINK REGISTER       * 01 *  51602850
                               287    *                                                                             51602860
 07B      0C 7066              288           L     YD,LOC,REFRESH          INCREMENTED LOC TO R1           R01    51602870
 07C      04 7410              289    BX     L     FLR,PSW                 NO CONDITION CODE CHANGE               51602880
 07D      E4 6C40              290           A     LOC,MR0,Q,IRJ           FETCH NEXT INSTR, BUMP LOC             51602890
                               291    *                                                                             51602900
                               292    *                                     COMMON DROM 1 ENTRY POINT FOR          51602910
 07E      A4 6C60              293    BXHL    A     LOC,LOC,Q,MR            BXH AND BXLE. FETCH A-FIELD            51602920
 07F      04 7830              294           L     MR0,MEM                                                        51602930
 080      04 5845              295           A     MR0,MR0,X2              BRANCH ADRS TO MR0                     51602940
 081      04 3E22              296           L     MDR,YD,YDP1             MDR GETS INDEX REGISTER                51602950
 082      00 3622              297           L     Q,YD,YDP1               Q HAS INCREMENT VALUE                  51602960
 083      00 6670              298           A     Q,MDR,Q                 INDEX PLUS INCREMENT                   51602970
 084      04 3A23              299           L     MAR,YD,YDM1             COMPARAND TO MAR                       51602980
 085      04 7843              300           L     MR0,MR0,YDM1            NOP..POINTING BACK TO R1               51602990
 086      0C 2020              301           L     YD,Q                                                           51603000
 087      45 665A              302           S     NULL,MAR,Q,C0+D2        COMPARAND MINUS INDEX..SET CARRY       51603010
                               303    *                                     VECTOR THROUGH DROM 2                  51603020
                               304    *                                                                            51603030
 0088                          305    BXH     EQU   *                       BRANCH ON INDEX HIGH           * C0 *  51603040
                               306    *                                                                            51603050
 088      00 7702              307           LI    Q,2                     RESTORE Q                              51603060
 089      63 C1D6              308           BF    C,EXIT1,REFRESH         NO BRANCH IF NOT LESS (P,2)            51603070
 08A      7B 87C0              309           B     BX                      TAKE BRANCH                            51603080
                               310    *                                                                            51603090
 008B                          311    BXLE    EQU   *                       BRANCH INDEX LOW OR EQUAL      * C1 *  51603100
                               312    *                                                                            51603110
 08B      00 7702              313           LI    Q,2                     RESTORE Q                              51603120
 08C      63 81D6              314           BT    C,EXIT1,REFRESH         NO BRANCH IF LESS (P,2)                51603130
 08D      7B 87C0              315           B     BX                      TAKE BRANCH                            51603140
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ARITHMETIC INSTRUCTIONS

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                                317   ACHR    EQU   *                ADD WITH CARRY HW REGISTER    * 0E *  51603160
                                318   ACH     EQU   *                ADD WITH CARRY HALFWORD       * 4E *  51603170
                                319   *                                                                    51603180
08F     G4 7410                 320           L     FLR,PSW          PROPOGATE USER'S FLAGS                51603190
                                321   *                                                                    51603200
                                322   AHR     EQU   *                ADD HALFWORD REGISTER         * 0A *  51603210
                                323   AH      EQU   *                ADD HALFWORD                  * 4A *  51603220
                                324   AHI     EQU   *                ADD HALFWORD IMMEDIATE        * CA *  51603230
                                325   AIS     EQU   *                ADD IMMEDIATE SHORT           * 26 *  51603240
                                326   *                                                                    51603250
08F     0C 504F                 327           A     YD,MR0,YD,F+CI+CO                                      51603260
090     E4 6C60                 328           A     LOC,LOC,Q,IRJ                                          51603270
                                329   *                                                                    51603280
0091                            330   AHM     EQU   *                ADD HALFWORD TO MEMORY        * 61 *  51603290
                                331   *                                                                    51603300
091     04 584E                 332           A     MR0,MR0,YD,F+CO  RESULT TO MR0                         51603310
092     84 7A50                 333           I     MAR,MAR,MW       START WRITE                           51603320
093     04 7640                 334           L     MEM,MR0          STORE RESULT                          51603330
094     E4 6C60                 335           A     LOC,LOC,Q,IRJ                                          51603340
                                336   *                                                                    51603350
0095                            337   SCHR    EQU   *                SUBTRACT/CARRY HW REGISTER    * 0F *  51603360
0095                            338   SCH     EQU   *                SUBTRACT WITH CARRY HALFWORD  * 4F *  51603370
                                339   *                                                                    51603380
095     04 7410                 340           L     FLR,PSW          PROPOGATE USER'S FLAGS                51603390
                                341   *                                                                    51603400
0096                            342   SHR     EQU   *                SUBTRACT HALFWORD REGISTER    * 0B *  51603410
0096                            343   SH      EQU   *                SUBTRACT HALFWORD             * 4B *  51603420
0096                            344   SHI     EQU   *                SUBTRACT HALFWORD IMMEDIATE   * CB *  51603430
0096                            345   SIS     EQU   *                SUBTRACT IMMEDIATE SHORT      * 27 *  51603440
                                346   *                                                                    51603450
096     0C D04F                 347           S     YD,YD,MR0,F+CI+CO                                      51603460
097     E4 6C60                 348           A     LOC,LOC,Q,IRJ                                          51603470
                                349   *                                                                    51603480
0098                            350   CHR     EQU   *                COMPARE HALFWORD REGISTER     * 09 *  51603490
0098                            351   CH      EQU   *                COMPARE HALFWORD              * 49 *  51603500
0098                            352   CHI     EQU   *                COMPARE HALFWORD IMMEDIATE    * C9 *  51603510
                                353   *                                                                    51603520
098     07 564C                 354           X     NULL,MR0,YD,F    COMPARE SIGNS                         51603530
099     67 4336                 355           BF    L,CR1,REFRESH    BRANCH IF ALIKE (P.3)          R01    51603540
09A     1D B02A                 356           LSL   YD,YD,CO         CARRY=1ST OP SIGN                     51603550
09B     15 R029                 357           LSR   YD,YD,CI         RESTORE R1                            51603560
09C     04 362C                 358           A     NULL,NULL,YD,F   SET G OR L                           51603570
09D     E4 6C60                 359           A     LOC,LOC,Q,IRJ                                          51603580
                                360   *                                                                    51603590
009E                            361   MHR     EQU   *                MULTIPLY HALFWORD REGISTER    * 06 *  51603600
009E                            362   MH      EQU   *                MULTIPLY HALFWORD             * 4C *  51603610
                                363   *                                                                    51603620
09E     7B B000                 364           B     MH1              (P.29)                                51603630
                                365   *                                                                    51603640
009F                            366   MHUR    EQU   *                MULTIPLY HW UNSIGNED REGISTER* 9C *  51603650
009F                            367   MHU     EQU   *                MULTIPLY HALFWORD UNSIGNED    * DC *  51603660
                                368   *                                                                    51603670
09F     7B B1C0                 369           B     MHU1             (P.30)                                51603680
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ARITHMETIC INSTRUCTIONS

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 00A0                          371   DHR     EQU   *                 DIVIDE HALFWORD REGISTER     * 0D *  51603700
 00A0                          372   DH      EQU   *                 DIVIDE HALFWORD              * 4D *  51603710
                               373   *                                                                    51603720
 00A0     7B B260              374         B       DH1               (P.30)                               51603730
                               375   *                                                                    51603740
                               376   *                               COMMON DROM1 ENTRY FOR               51603750
 00A1     A4 6C60              377   SLRHA   A       LOC,LOC,Q,MR      SLHA, SRHA.  FETCH A FIELD         51603760
 00A2     04 7830              378         L       MR0,MEM                                                51603770
 00A3     04 5845              379         A       MR0,MR0,X2        PERFORM INDEXING IF SPECIFIED        51603780
 00A4     00 7640              380         L       Q,MR0             SHIFT COUNT TO Q REGISTER            51603790
 00A5     04 7B80              381         LT      MAR,'80'                                               51603800
 00A6     06 5ADA              382         N       MAR,MAR,YD,CS+CO  MAR = SIGN BIT OF R1                 51603810
 00A7     1D B020              383         LSL     YD,YD             PRESHIFT R1                          51603820
 00A8     06 690F              384         NI      MR0,'0F',Q        MASK 4-BIT SHIFT COUNT               51603830
 00A9     45 7847              385         DECF    MR0,MR0,NULL,D2   DECREMENT WITH FLAGS               51603840
                               386   *               VECTOR THRU DROM2 TO SLHA OR SRHA                    51603850
                               387   *                                                                    51603860
                               388   *                                                                    51603870
 00AA                          389   SLHA    EQU   *                 SHIFT LEFT HW ARITHMETIC     * CF *  51603880
                               390   *                                                                    51603890
 00AA     67 0B16              391         BT      L,EXIT4,REFRESH   EXIT IF COUNT MINUS                  51603900
 00AB     1D B02A              392         LSL     YD,YD,CO          DO SHIFT LEFT                        51603910
 00AC     45 7847              393         DECF    MR0,MR0,NULL,D2   DECREMENT COUNT, LOOP THRU DROM2    51603920
                               394   *                                                                    51603930
                               395   *                                                                    51603940
 00AD                          396   SRHA    EQU   *                 SHIFT RIGHT HW ARITHMETIC    * CE *  51603950
                               397   *                                                                    51603960
 00AD     67 0BA6              398         BT      L,EXIT5,REFRESH   EXIT IF COUNT MINUS                  51603970
 00AF     15 B02A              399         LSR     YD,YD,CO          DO SHIFT RIGHT                       51603980
 00AF     0D D050              400         O       YD,MAR,YD         PROPOGATE SIGN BIT                   51603990
 00B0     45 7847              401         DECF    MR0,MR0,NULL,D2   DECREMENT COUNT, LOOP THRU DROM2    51604000
                               402   *                                                                    51604010
                               403   *                                                                    51604020
 00B1     15 B020              404   EXIT4   LSR     YD,YD             COMPENSATE FOR PRE-SHIFT             51604030
 00B2     00 7702              405   EXIT4.5 LT      Q,2               RESTORE Q REGISTER                   51604040
 00B3     63 8B70              406         BT      C,EXIT4A          BRANCH IF SHIFTED CARRY              51604050
 00B4     04 7500              407         LT      FLR,0             CLEAR FLAGS                          51604060
 00B5     0D D05C              408         O       YD,MAR,YD,F       INSERT SIGN BIT, SET FLAGS           51604070
 00B6     E4 6C60              409         A       LOC,LOC,Q,IRJ                                          51604080
 00B7     04 7508              410   EXIT4A  LT      FLR,8             CLEAR FLAGS EXCEPT FOR CARRY         51604090
 00B8     0D D05C              411         O       YD,MAR,YD,F       INSERT SIGN BIT, SET FLAGS           51604100
 00B9     E4 6C60              412         A       LOC,LOC,Q,IRJ                                          51604110
 00BA     15 B02A              413   EXIT5   LSR     YD,YD,CO          COMPENSATE PRE-SHIFT, SET CARRY      51604120
 00BB     7B 8B20              414         B       EXIT4.5                                                51604130
                               415   *                                                                    51604140
                               416   *               COMMON DROM 1 ENTRY FOR                              51604150
 00BC     7B A0C0              417   SLRA    B       SLRA1             SLA & SRA  (P.21)                    51604160
```

STATUS SWITCHING INSTRUCTIONS

```
 00BD                    419   LPSW    EQU  *                    LOAD PROGRAM STATUS WORD      * C2 *  51604180
                         420   *                                                                       51604190
 0BD     04 7240         421           L    PSW,MR0              LOAD NEW PSW                         51604200
 0BE     04 6A50         422           A    MAR,MAR,Q            INCREMENT MAR                        51604210
 0BF     A4 7A50         423           L    MAR,MAR,MR           FETCH NEW LOC                        51604220
 0C0     04 7C30         424           L    LOC,MEM              LOAD IT                              51604230
 0C1     7B 9296         425           B    TEST1,REFRESH        (P,14)                               51604240
                         426   *                                                                       51604250
 00C2                    427   EPSR    EQU  *                    EXCHANGE PSW REGISTER        * 95 *  51604260
                         428   *                                                                       51604270
 0C2     0C 7010         429           L    YD,PSW               PSW TO R1                            51604280
 0C3     08 3220         430           L    YDA&PSW,YD           YD GETS YD, PSW GETS YS              51604290
 0C4     7B 9296         431           B    TEST1,REFRESH        (P,14)                               51604300
 0C5     00 0000         432           DC   0                    FILLER                               51604310
                         433   *                                                                       51604320
 00C6                    434   SINT    EQU  *                    SIMULATE INTERRUPT           * E2 *  51604330
                         435   *                                                                       51604340
 0C6     00 7640         436           L    Q,MR0                                                     51604350
 0C7     06 69FF         437           NI   MR0,'FF',Q           MASK 8-BIT DEVICE NUMBER             51604360
 0C8     7B 9100         438           B    AUTOIO1              AUTOMATIC I/O SERVICE (P,13)         51604370
                         439   *                                                                       51604380
 00C9                    440   SVC     EQU  *                    SUPERVISOR CALL              * E1 *  51604390
                         441   *                                                                       51604400
 0C9     7B A920         442           B    SVC1                 (P,25)                               51604410
```

INPUT/OUTPUT INSTRUCTIONS

```
 00CA                    444    ACKR    EQU   *                    ACKNOWLEDGE INTERRUPT RR      * 9F *  51604430
                         445    *                                                                         51604440
 0CA     0C 7001         446            ACK   YD                   ACKNOWLEGE INTERRUPT                  51604450
                         447    *                                                                         51604460
                         448    *                                   COMMON DROM 1 ENTRYPOINT              51604470
 0CB     44 3021         449    RRIO    ADR   YD,D2                ADDRESS THE DIVICE                    51604480
                         450    *                                   VECTOR THROUGH DROM 2                 51604490
 0CC     0C 7001         451    ACK     ACK   YD                   ACKNOWLEDGE INTERRUPT         * DF *  51604500
 0CD     04 3021         452            ADR   YD                   ADDRESS THE DEVICE                    51604510
                         453    *                                                                         51604515
 00CE                    454    SS      EQU   *                    SENSE STATUS                  * DE *  51604520
                         455    *                                                                         51604530
 0CE     04 7E82         456            SS    MDR,CS               STATUS BYTE TO MDR                    51604540
 0CF     84 7A50         457            L     MAR,MAR,MW           START MEMORY WRITE                    51604550
 0D0     04 7670         458            L     MEM,MDR                                                    51604560
 0D1     04 74F0         459            L     FLR,MDR,CS           LS 4 BITS TO FLR                      51604570
 0D2     E4 6C60         460            A     LOC,LOC,Q,IRJ        FETCH NEXT INSTR. BUMP LOC            51604580
                         461    *                                                                         51604600
 00D3                    462    SSR     EQU   *                    SENSE STATUS REGISTER         * 9D *  51604610
                         463    *                                                                         51604620
 0D3     00 7602         464            SS    Q                    STATUS BYTE TO Q REGISTER             51604630
 0D4     04 2420         465            L     FLR,Q                LS 4 BITS TO FLAG REGISTER            51604640
 0D5     7B 8F10         466            B     RRINPUT              (P.12)                                51604650
                         467    *                                                                         51604660
 00D6                    468    OC      EQU   *                    OUTPUT COMMAND                * DE *  51604670
                         469    *                                                                         51604680
 0D6     04 78F0         470            L     MR0,MDR,CS           GET PROPER BYTE                       51604690
                         471    *                                                                         51604700
 00D7                    472    OCR     EQU   *                    OUTPUT COMMAND REGISTER       * 9F *  51604710
                         473    *                                                                         51604720
 0D7     04 7042         474            OC    MR0                  OUTPUT                                51604730
 0D8     04 7840         475            L     MR0,MR0              NOP                                   51604740
 0D9     04 7840         476            L     MR0,MR0              NOP                                   51604750
 0DA     E4 6C60         477            A     LOC,LOC,Q,IRJ                                              51604760
                         478    *                                                                         51604770
 00DB                    479    RD      EQU   *                    READ DATA                     * DB *  51604780
                         480    *                                                                         51604790
 0DB     04 7E84         481            RD    MDR,CS               DATA BYTE TO MDR                      51604800
 0DC     84 7A50         482            L     MAR,MAR,MW           START MEMORY WRITE                    51604810
 0DD     04 7670         483            L     MEM,MDR              STORE                                 51604820
 0DE     E4 6C60         484            A     LOC,LOC,Q,IRJ                                              51604830
                         485    *                                                                         51604840
 00DF                    486    RH      EQU   *                    READ HALFWORD                 * D9 *  51604850
                         487    *                                                                         51604860
 0DF     7D EE00         488            BF    HWIO,RHB             BRANCH IF HW NOT ACTIVE (P.28)        51604870
 0E0     04 7804         489            RD    MR0                  INPUT HALFWORD                        51604880
 0E1     84 7A50         490            L     MAR,MAR,MW                                                 51604890
 0E2     04 7640         491            L     MEM,MR0                                                    51604900
 0E3     E4 6C60         492            A     LOC,LOC,Q,IRJ                                              51604910
```

INPUT/OUTPUT INSTRUCTIONS

```
 00E4                    494   RHR     EQU   *                 READ HALFWORD REGISTER      * 99 *  51604930
                         495   *                                                                     51604940
0E4     7B AE60          496           B     RHP1              (P.28)                               51604950
                         497   *                                                                     51604960
 00E5                    498   RDR     EQU   *                 READ DATA REGISTER          * 9B *  51604970
                         499   *                                                                     51604980
0E5     00 7604          500           RD    Q                 DATA BYTE TO Q REGISTER              51604990
0E6     7B 8F10          501           B     RRINPUT                                                51605000
                         502   *                                                                     51605010
 00E7                    503   WD      EQU   *                 WRITE DATA                  * DA *  51605020
                         504   *                                                                     51605030
0E7     04 78F0          505           L     MR0,MDR,CS        PROPER BYTE TO MR0                   51605040
0E8     04 7044          506           WD    MR0               OUTPUT                               51605050
0E9     E4 6C60          507           A     LOC,LOC,Q,IRJ                                          51605060
                         508   *                                                                     51605070
 00EA                    509   WH      EQU   *                 WRITE HALFWORD              * D8 *  51605080
                         510   *                                                                     51605090
0EA     04 7870          511           L     MR0,MDR           DATA BYTES TO MR0                    51605100
                         512   *                                                                     51605110
 00EB                    513   WHR     EQU   *                 WRITE HALFWORD REGISTER     * 98 *  51605120
                         514   *                                                                     51605130
0EB     7D EED0          515           BF    HWIO,WHB          BRANCH IF HW NOT ACTIVE (P.28)       51605140
                         516   *                                                                     51605150
 00EC                    517   WDR     EQU   *                 WRITE DATA REGISTER         * 9A *  51605160
                         518   *                                                                     51605170
0EC     04 7044          519           WD    MR0               OUTPUT                               51605180
0ED     E4 6C60          520           A     LOC,LOC,Q,IRJ                                          51605190
                         521   *                                                                     51605200
 00EE                    522   RB      EQU   *                 READ BLOCK                  * D7 *  51605210
 00EE                    523   WB      EQU   *                 WRITE BLOCK                 * D6 *  51605220
                         524   *                                                                     51605230
0EE     7B AC20          525           B     RWBRX             (P.27)                               51605240
                         526   *                                                                     51605250
 00EF                    527   RBR     EQU   *                 READ BLOCK REGISTER         * 97 *  51605260
 00EF                    528   WBR     EQU   *                 WRITE BLOCK REGISTER        * 96 *  51605270
                         529   *                                                                     51605280
0EF     7B ABA0          530           B     RWBRR             (P.27)                               51605290
                         531   *                                                                     51605300
 00F0                    532   AL      EQU   *                 AUTOLOAD                    * D5 *  51605310
                         533   *                                                                     51605320
0F0     7B AA60          534           B     AL1               (P.26)                               51605330
                         535   *                                                                     51605340
0F1     0E 63FF          536   RRINPUT NI    YS,'FF',Q         MASK LS 8 BITS TO R2                 51605350
0F2     00 7702          537           LI    Q,2                                                    51605360
0F3     E4 6C60          538           A     LOC,LOC,Q,IRJ                                          51605370
                         539   *                                                                     51605380
                         540   *                                                                     51605390
                         541   * I N T E R R U P T A B L E   W A I T   L O O P                       51605400
                         542   *                                                                     51605410
0F4     68 9020          543   WAIT    BT    DMA+ATN+CATN,INTRPT1 (P.13)                          51605420
0F5     7B 8F46          544           B     WAIT,REFRESH                                           51605430
```

INTERRUPT SUPPORT

```
0FE                     546             ORG   '0FE'           BREAKPOINT                          * 88 *  51605450
0FE     7F 1E50         547             DC    '7F1E50'        BT   OPT,RESET  (P.19)                      51605460
0FF     7B 91E0         548   ILLEGAL   B     ILLEGAL1        (P.14)                                      51605470
                        549   *                                                                           51605480
                        550   *                                                                           51605490
                        551   *                                                                           51605500
100     6F 1060         552   INTERUPT  BT    PWRUP,INITIAL                                               51605510
101     05 6C60         553             S     LOC,LOC,Q       DECREMENT LOC                               51605520
102     6E 9E56         554   INTRPT1   BT    CATN,RESET,REFRESH  CONSOLE INTERRUPT (P.19)                 51605530
103     6D 93A0         555             BT    DMA,DMAATN      BRANCH IF DMA (P.15)                        51605540
104     6B 9090         556             BT    ATN,IOATN       I/O INTERRUPT                               51605550
105     7B 9290         557             B     TEST1           IGNORE SPURIOUS INTERRUPT (P.14)            51605560


                        559   *                               INITIALIZE OR POWER UP                      51605580
                        560   *                                                                           51605590
106     04 7846         561   INITIAL   L     MR0,MR0,REFRESH REFRESH LOOP, PWRUP REMAINS ACTIVE          51605600
107     6F 1060         562             BT    PWRUP,*-1       UNTIL REFRESH ALL 64 COLUMNS                51605610
108     7B B7E0         563             B     SELFTEST        DO MINOR DIAGNOSTIC                         51605620


0109                    565   IOATN     EQU   *                                                           51605640
                        566   *                                                                           51605650
109     04 7B40         567             LT    MAR,'40'        PRESET MAR                                  51605660
10A     04 7490         568             L     FLR,PSW,CS      TEST PSW BIT 4 IF RESET                     51605670
10B     63 D200         569             BF    C,GENSWP        PERFORM PSW SWAP (P.14)                     51605680
                        570   *                               IF SET, TAKE IMMEDIATE INTERRUPT            51605690
10C     7E D0F0         571             BF    SPATN,AUTOIO    SKIP IF NOT SPECIAL ATTENTION               51605700
10D     04 7907         572             LT    MR0,X'07'       ASSUME FIXED ADRS FOR SPATN                 51605710
10F     7B 9100         573             B     AUTOI01                                                     51605720
                        574   *                                                                           51605730
10F     04 7801         575   AUTOIO    ACK   MR0             ACKNOWLEDGE INTERRUPT.                      51605740
                        576   *                               MR0=DEVICE NUMBER                           51605750
110     00 7640         577   AUTOI01   L     Q,MR0                                                       51605760
111     00 6840         578             A     MR0&Q,MR0,Q     2X DEVICE NUMBER                            51605770
112     04 6BD0         579             AT    MAR,'D0',Q      PLUS 'D0' FORMS ADDRESS OF                  51605780
113     00 7702         580             LT    Q,2             A HALFWORD ENTRY IN THE SERVICE             51605790
114     A4 7A50         581             L     MAR,MAR,MR      POINTER TABLE.  USE ENTRY AS                51605800
115     04 7A30         582             L     MAR,MEM         INTERRUPT SERVICE ROUTINE ADRS              51605810
116     84 6A50         583             A     MAR,MAR,Q,MW                                                51605820
117     04 7610         584             L     MEM,PSW         FIRST STORE OLD PSW                         51605830
118     84 6A50         585             A     MAR,MAR,Q,MW                                                51605840
119     04 7660         586             L     MEM,LOC         STORE OLD LOC                               51605850
11A     A4 6C50         587             A     LOC,MAR,Q,MR    FETCH NEW PSW, SET NEW LOC                  51605860
11B     04 7830         588             L     MR0,MEM         PASS NEW PSW THROUGH MR0                    51605870
11C     04 7240         589             L     PSW,MR0         LOAD NEW PSW                                51605880
11D     7B 81D6         590             B     EXIT1,REFRESH   FETCH INSTRUCTION (P.3)        R01          51605A90
```

INTERRUPT SUPPORT

```
11F   05 6C60   592  ILEGAL1  S   LOC,LOC,Q          DECREMENT LOC                          51605910
11F   04 7B30   593           LI  MAR,'30'           ADRS OF OLD PSW                        51605920


                595  * GENERAL PSW SWAP ROUTINE...MAR=ADRS OF OLD PSW                       51605940
                596  *                                                                      51605950
120   84 6A50   597  GENSWP   A   MAR,MAR,Q,MW                                             51605960
121   04 7610   598           I   MEM,PSW            STORE OLD PSW                          51605970
122   84 6A50   599           A   MAR,MAR,Q,MW                                             51605980
123   04 7660   600           I   MEM,LOC            STORE OLD LOC                          51605990
124   A4 6A50   601           A   MAR,MAR,Q,MR                                             51606000
125   04 7830   602           L   MR0,MEM            PASS NEW PSW THROUGH MR0               51606010
126   04 7240   603           I   PSW,MR0                                                  51606020
127   A4 7A50   604           I   MAR,MAR,MR                                               51606030
128   04 7C30   605           L   LOC,MEM            LOAD NEW LOC                           51606040
129   04 7490   606  TEST1    I   FLR,PSW,CS         TEST PSW BIT 6                         51606050
12A   66 D366   607           BF  G,TEST2,REFRESH    QUEUE SERVICE NOT ENABLED      R01     51606060
12B   6E 9E50   608  QUENBL   BT  CATN,RESET        LEAVE IF CONSOLE ATTENTION (P.19)      51606070
12C   A4 7B80   609           LI  MAR,'80',MR        FETCH ADDRESS OF SYSTEM QUEUE          51606080
12D   04 7A30   610           L   MAR,MEM                                                  51606090
12E   A4 7A50   611           I   MAR,MAR,MR         FETCH QUEUE PARAMETERS                 51606100
12F   04 7E30   612           I   MDR,MEM                                                  51606110
130   04 7500   613           LI  FLR,0                                                    51606120
131   06 2EA0   614           N   MDR,NULL,Q,CS      RESULT ZERO, CLEAR HIGH BYTE           51606130
132   05 F67C   615           O   NULL,MDR,NULL,F    TEST NO. USED TALLY                    51606140
133   66 D366   616           BF  G,TEST2,REFRESH    CONTINUE IF TALLY IS ZERO              51606150
134   04 7B82   617           LI  MAR,'82'                                                 51606160
135   7B 9200   618           B   GENSWP             TAKE QUEUE SERVICE INTERRUPT           51606170


136   04 7500   620  TEST2    LI  FLR,0                                                    51606190
137   05 F61C   621           O   NULL,PSW,NULL,F    TEST WAIT BIT OF PSW                   51606200
138   67 0F40   622           BT  L,WAIT             TO WAIT IF SET (P.12)                  51606210
139   7B 8106   623           B   EXIT1,REFRESH      (P.2)                                  51606220
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INTERRUPT SUPPORT

```
                        625   *              D M A   A T T E N T I O N                                  51606240
                        626   *                                                                         51606250
13A     04 79C0         627   DMAATN   LI     MR0,'C0'                                                  51606260
13B     04 7041         628            ABR    MR0                  ADDRESS MICRO I/O                    51606264
13C     04 7A09         629            DACK   MAR                  PRIME DMA                            51606266
13D     04 7A09         630            DACK   MAR                  COLLECT MEMORY ADDRESS               51606270
13F     04 7450         631            L      FLR,MAR                                                   51606280
13F     67 1450         632            BT     L,DMA.RD             READ IF ODD ADDRESS                  51606290
                        633   *                                     ELSE WRITE                           51606300


140     A4 6A50         635   DMA.WRT  A      MAR,MAR,Q,MR         FETCH DATA FROM MEMORY               51606320
141     04 7830         636            I      MR0,MEM                                                   51606330
142     04 7044         637            WD     MR0                  OUTPUT TO DMA DEVICE                 51606340
143     6D 9406         638            BT     DMA,DMA.WRT,REFRESH  LOOP IF DMA LINE STILL ACTIVE        51606350
144     7B 9360         639            B      TEST2                (P,14)                               51606360
                        640   *                                                                         51606370


145     04 7E04         642   DMA.RD   RD     MDR                  READ DATA FROM DMA DEVICE            51606390
146     84 6A50         643            A      MAR,MAR,Q,MW                                              51606400
147     04 7670         644            L      MEM,MDR              STORE IN MEMORY                      51606410
148     6D 9456         645            BT     DMA,DMA,RD,REFRESH   LOOP IF DMA LINE IS STILL ACTIVE    51606420
149     7B 9360         646            B      TEST2                (P,14)                               51606430
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ASCII CONSOLE SUPPORT

```
00C0                    648   DEVICE   EQU   'C0'              ASCII CONSOLE DEVICE NUMBER          51606450
0022                    649   COMAND1  EQU   '22'              "WRITE" COMMAND                      51606460
0082                    650   COMAND2  EQU   '82'              "READ" COMMAND                       51606470
                        651   *                                                                       51606480
                        652   *                                                                       51606490
14A     04 797F         653   CONSER   LT    MR0,'7F'                                               51606500
14B     00 76C0         654            L     Q,MR0,CS                                               51606510
14C     01 E7FF         655            OT    Q,'FF',Q          Q='7FFF'                             51606520
14D     06 6210         656            N     PSW,PSW,Q         CLEAR WAIT BIT IN PSW                51606530
14F     84 7B24         657            LT    MAR,'24',MW                                            51606540
14F     04 7610         658            L     MEM,PSW           SAVE CURRENT PSW                     51606550
150     84 7B26         659            LT    MAR,'26',MW                                            51606560
151     04 7661         660            L     MEM,LOC,CLRYD     SAVE CURRENT LOC                     51606570
152     04 7B00         661            LT    MAR,0             ADDRESS ZERO                         51606580
153     00 7702         662            LT    Q,2                                                    51606590
154     04 3E20         663   STRREG   L     MDR,YD            MDR = REGISTER TO STORE              51606600
155     84 6A50         664            A     MAR,MAR,Q,MW      STORE ALL GENERAL REGISTERS          51606610
156     04 7672         665            L     MEM,MDR,YDP1      AT LOCATIONS '0000' THRU '001F'      51606620
157     77 5546         666            BF    YDCARY,STRREG,REFRESH *                        R01     51606630
158     04 7E60         667            L     MDR,LOC           MDR = DATA TO DISPLAY                51606640
159     04 7D00         668   SHOW     LT    LOC,0             LOC = RETURN QUEUE                   51606650
15A     78 9CF0         669            B     CRLF              SUBROUTINE CRLF TO SET UP DEVICE     51606660
                        670   *                               DO CARRIAGE RETURN,LINE FEED (P.19)  51606670
                        671   *                               CONTROL RETURNS TO "DISPLAY"         51606680
                        672   *                                                                      51606690
15B     04 7B00         673   DISPLAY  LT    MAR,0                                                  51606700
15C     0C 7070         674   NEXTCHAR L     YD,MDR            COPY DATA TO OUTPUT INTO YD          51606710
15D     1D B02B         675            LSL   YD,YD,CI+C0       ROTATE LEFT 4 BIT POSITIONS          51606720
15E     1D B02B         676            LSL   YD,YD,CI+C0                                            51606730
15F     1D B02B         677            LSL   YD,YD,CI+C0                                            51606740
160     1D B02B         678            LSL   YD,YD,CI+C0                                            51606750
161     04 3E26         679            L     MDR,YD,REFRESH    PUT BACK IN MDR              R01     51606760
162     06 590F         680            NI    MR0,'0F',YD       ISOLATE HEX DIGIT                    51606770
163     0C 7130         681            LT    YD,X'30'          CONVERT TO ASCII                     51606780
164     0C 5040         682            A     YD,MR0,YD                                              51606790
165     04 3420         683            L     FLR,YD                                                 51606800
166     63 D6A0         684            BF    C,OKASCII         VALID 0:7                            51606810
167     65 9690         685            BT    V,ADJUST                                               51606820
168     66 D6A0         686            BF    G,OKASCII         VALID 8 OR 9                         51606830
169     0C 5107         687   ADJUST   AI    YD,'07',YD        ADJUST A:F                           51606840
16A     04 7402         688   OKASCII  SS    FLR                                                    51606850
16B     60 16A6         689            BT    C+V+G+L,*-1,REFRESH                                    51606860
16C     04 3024         690            WD    YD                OUTPUT HEX CHARACTER                 51606870
16D     04 7A54         691            INC   MAR,MAR,NULL      BUMP STATE REGISTER                  51606880
16F     04 7450         692            T     FLR,MAR           TEST                                 51606890
16F     65 D5C0         693            BF    V,NEXTCHAR        LOOP UNTIL EQUAL TO 4                51606900
                        694   *                                                                      51606910
                        695   *                               MDR CONTAINS HALFWORD JUST OUTPUT    51606920
```

ASCII CONSOLE SUPPORT

```
170  04 7D01   697  PROMPT   LI   LOC,1              LOC = RETURN QUEUE                          51606940
171  7B 9CF0   698           B    CRLF               SET-UP DEVICE, DO CR AND LF (P.19)          51606950
               699  *                                CONTROL RETURNS TO "PROMPT1"                51606960
               700  *                                                                            51606970
               701  *                                                                            51606980
172  04 792A   702  PROMPT1  LI   MR0,C'*'           ASTERISK PROMPT CHARACTER                   51606990
173  04 7402   703  OUTPUT2  SS   FLR                                                            51607000
174  63 9736   704           BT   C,OUTPUT2,REFRESH                                             51607010
175  04 7044   705           WD   MR0                OUTPUT CHARACTER                            51607020
176  04 7402   706           SS   FLR                                                           51607030
177  63 9766   707           BT   C,*-1,REFRESH      WAIT FOR LAST CHARACTER                     51607040
178  04 7982   708           LI   MR0,COMAND2                                                   51607050
179  04 7042   709           OC   MR0                SWITCH TO READ MODE                         51607060
17A  04 7804   710           RD   MR0                FORCE BUSY                                  51607070
17B  04 7B00   711           LI   MAR,0              CLEAR STATE REGISTER                        51607080
17C  04 7402   712  INPUT1   SS   FLR                                                           51607090
17D  6E AF10   713           BT   CATN,BEGIN         IF HANG UP DUE TO BAD STATUS FROM           51607100
               714  *                                THE ASCII CONSOLE, DEPRESSING THE           51607110
               715  *                                EXECUTE SWITCH CAUSES EXIT.  THE            51607120
               716  *                                PROCESSOR ENTERS THE RUN MODE AT            51607130
               717  *                                THE ADDRESS SPECIFIED BY LOC.               51607140
17F  60 17C6   718           BT   C+V+G+L,INPUT1,REFRESH WAIT FOR INPUT                         51607150
180  00 7604   719           RD   Q                  INPUT CHARACTER                             51607160
181  04 2024   720           WD   Q                  ECHO BACK                                   51607170
182  04 7456   721           L    FLR,MAR,REFRESH    TEST STATE                                  51607180
183  06 697F   722           NI   MR0,'7F',Q         REMOVE PARITY BIT                           51607190
184  60 1A40   723           BT   C+V+G+L,INPUT2                                                51607200
185  00 772A   724           LI   Q,C'*'                                                        51607210
186  07 664C   725           X    NULL,MR0,Q,F       ASTERISK?                                   51607220
187  66 6F10   726           BF   G+L,BEGIN          YES, START EXECUTION (P.28)                 51607230
188  04 7500   727           LI   FLR,0                                                         51607240
189  00 7740   728           LI   Q,C'@'                                                        51607250
18A  07 664C   729           X    NULL,MR0,Q,F       CHARACTER = @ ?                             51607260
18B  66 98E6   730           BT   G,IF.EQUAL,REFRESH NO, BRANCH                                 51607270
18C  04 7B04   731           LI   MAR,4              SET STATE = 4   EXAMINE                     51607280
18D  0C 7100   732  INPUT1A  LI   YD,0               CLEAR ACCUMULATOR                           51607290
18E  7B 97C0   733           B    INPUT1             GO FOR HEX NUMBER NOW                       51607300
18F  04 7500   734  IF.EQUAL LI   FLR,0                                                         51607310
190  00 773D   735           LI   Q,C'='                                                        51607320
191  07 664C   736           X    NULL,MR0,Q,F       EQUAL SIGN ?                                51607330
192  66 9946   737           BT   G,IF.PLUS,REFRESH  NO, BRANCH                                 51607340
193  04 7B05   738           LI   MAR,5              SET STATE = 5   MODIFY                      51607350
194  7B 98C0   739           B    INPUT1A                                                       51607360
195  04 7500   740  IF.PLUS  LI   FLR,0                                                         51607370
196  00 772B   741           LI   Q,C'+'                                                        51607380
197  07 664C   742           X    NULL,MR0,Q,F       PLUS SIGN?                                  51607390
198  66 99D0   743           BT   G,IF.XFER          NO, BRANCH (P.18)                           51607400
199  00 7702   744           LI   Q,2                                                           51607410
19A  A4 7B26   745           LI   MAR,'26',MR                                                   51607420
19B  04 7C30   746           L    LOC,MEM            FETCH LOC                                   51607430
19C  04 6C66   747           A    LOC,LOC,Q,REFRESH  INCREMENT LOC                    R01    51607440
19D  7B 9BF0   748           B    EXAMINE1           SHOW CONTENTS OF NEXT CELL                  51607450
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ASCII CONSOLE SUPPORT

```
19D  04 7500        750  IF.XFER  LI   FLR,0                                          51607470
19E  00 773F        751           LI   Q,C'?'                                        51607480
19F  07 664C        752           X    NULL,MR0,Q,F      CHARACTER = QUESTION MARK ?  51607490
1A0  66 9700        753           BT   G,PROMPT          RESTART IF NO (P.17)         51607500
1A1  0C 7070        754           L    YD,MDR            MDR CONTAINS LAST HALFWORD   51607510
1A2  04 7B04        755           LI   MAR,4             DISPLAYED.  USE AS NEW ADDRESS 51607520
1A3  7B 97C0        756           B    INPUT1            FOR EXAMINE (P.17)           51607530
                    757  *                                                            51607540
                    758  *                                                            51607550
1A4  00 7730        759  INPUT2   LI   Q,X'30'                                       51607560
1A5  05 684A        760           S    MR0,MR0,Q,CO      SUBTRACT '30' FROM CHARACTER 51607570
1A6  63 9B80        761           BT   C,NOT.HEX         NOT VALID                    51607580
1A7  00 770A        762           LI   Q,X'0A'                                       51607590
1A8  05 664A        763           S    NULL,MR0,Q,CO                                 51607600
1A9  63 9B20        764           BT   C,NUMERIC         VALID 0:9                    51607610
1AA  00 7711        765           LI   Q,X'11'                                       51607620
1AB  05 664A        766           S    NULL,MR0,Q,CO                                 51607630
1AC  63 9B86        767           BT   C,NOT.HEX,REFRESH BAD HEX                 R01 51607640
1AD  00 7707        768           LI   Q,X'07'                                       51607650
1AE  05 6840        769           S    MR0,MR0,Q         ADJUST A THROUGH F           51607660
1AF  00 7710        770           LI   Q,X'10'                                       51607670
1B0  05 664A        771           S    NULL,MR0,Q,CO                                 51607680
1B1  63 DB80        772           BF   C,NOT.HEX                                     51607690
                    773  *                              MR0 = NEW HEX DIGIT          51607700
1B2  1D B020        774  NUMERIC  LSL  YD,YD             YD USED AS HEX ACCUMULATOR   51607710
1B3  1D B020        775           LSL  YD,YD             SHIFT IT LEFT 4              51607720
1B4  1D B020        776           LSL  YD,YD                                         51607730
1B5  1D B020        777           LSL  YD,YD                                         51607740
1B6  0D D040        778           O    YD,MR0,YD         OR IN HEX DIGIT              51607750
1B7  7B 97C0        779           B    INPUT1            GO FOR NEXT CHARACTER (P.17) 51607760
                    780  *                                                            51607770
1B8  04 7500        781  NOT.HEX  LI   FLR,0                                         51607780
1B9  00 7723        782           LI   Q,'23'            = '30' - '0D'                51607790
1BA  04 664C        783           A    NULL,MR0,Q,F      CARRIAGE RETURN?             51607800
1BB  66 9700        784           BT   G,PROMPT          NO, RE-ISSUE PROMPT (P.17)   51607810
                    785  *                              YES, END OF HEX INPUT        51607820
1BC  04 7450        786           L    FLR,MAR           TEST STATE                   51607830
1BD  67 1C40        787           BT   L,MODIFY                                      51607840
                    788  *                                                            51607850
                    789  *                                                            51607860
1BE  04 3C20        790  EXAMINE  L    LOC,YD            SELECT ADDRESS               51607870
1BF  84 7B26        791  EXAMINE1 LI   MAR,'26',MW                                  51607880
1C0  04 7660        792           L    MEM,LOC           SAVE NEW ADDRESS             51607890
1C1  A4 7A60        793           L    MAR,LOC,MR        READ CONTENTS                51607900
1C2  04 7E30        794           L    MDR,MEM           DATA TO MDR                  51607910
1C3  7B 9590        795           B    SHOW              (P.16)                       51607920
                    796  *                                                            51607930
1C4  A4 7B26        797  MODIFY   LI   MAR,'26',MR                                  51607940
1C5  04 7C30        798           L    LOC,MEM           FETCH LOCATION COUNTER       51607950
1C6  04 3E20        799           L    MDR,YD            MDR = DATA TO STORE          51607960
1C7  84 7A60        800           L    MAR,LOC,MW                                    51607970
1C8  04 7670        801           L    MEM,MDR           DO MEMORY WRITE              51607980
1C9  00 7702        802           LI   Q,2                                           51607990
1CA  04 6C60        803           A    LOC,LOC,Q         INCREMENT LOC                51608000
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ASCII CONSOLE SUPPORT

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1CB   84 7B26    804          LI    MAR,'26',MW                                  51608010
1CC   04 7660    805          I     MEM,LOC          STORE LOC                   51608020
1CD   7B 9700    806          B     PROMPT           NEXT COMMAND (P.17)         51608030
                 807  *                                                         51608040


                 809  *        S U B R O U T I N E   C R L F                     51608060
                 810  *                                                         51608070
1CE   6E AF10    811  IDLE     BT    CATN,BEGIN       EXIT IF NO CONSOLE (P.2A)   51608080
1CF   04 79C0    812  CRLF     LI    MR0,DEVICE       LOAD CONSOLE DEVICE NUMBER  51608090
1D0   04 7041    813          AOR   MR0              ADDRESS THE DEVICE          51608100
1D1   04 7922    814          LI    MR0,COMAND1                                  51608110
1D2   04 7042    815          OC    MR0              ISSUE FIRST OUTPUT COMMAND  51608120
                 816  *                                                         51608130
                 817  *                                                         51608140
1D3   04 7B00    818          LI    MAR,0            SET STATE 0                 51608150
1D4   04 7900    819          LI    MR0,0            FOR STATES 0 & 1, OUTPUT NULLS 51608160
1D5   04 7402    820  OUTPUT1  SS    FLR                                          51608170
1D6   65 1CE6    821          BT    V+L,IDLE,REFRESH RE-TRY IF BAD STATUS        51608180
1D7   63 9D50    822          BT    C,OUTPUT1        LOOP ON BUSY                51608190
1D8   04 7044    823          WD    MR0                                          51608200
1D9   04 7A54    824          INC   MAR,MAR,NULL                                 51608210
1DA   04 7450    825          I     FLR,MAR          CHECK STATE                 51608220
1DB   60 DD50    826          BF    C+V+G,OUTPUT1    LOOP BACK FOR STATE 1       51608230
1DC   04 790D    827          LI    MR0,X'0D'                                    51608240
1DD   67 5D50    828          BF    L,OUTPUT1        STATE 2: OUTPUT CARRIAGE RETURN 51608250
1DE   04 790A    829          LI    MR0,X'0A'                                    51608260
1DF   61 DD50    830          BF    C+V,OUTPUT1      STATE 3: OUTPUT LINE FEED   51608270
1E0   04 7900    831          LI    MR0,0                                        51608280
1E1   66 DD50    832          BF    G,OUTPUT1        STATES 4 & 5, OUTPUT NULLS  51608290
1E2   04 7460    833          L     FLR,LOC          TEST RETURN QUEUE           51608300
1E3   60 55B0    834          BF    C+V+G+L,DISPLAY  TO DISPLAY IF ZERO (P.16)   51608310
1E4   7B 9720    835          B     PROMPT1          ELSE, GO TO PROMPT1 (P.17)  51608320


1E5   04 79C0    837  RESET    LI    MR0,DEVICE                                   51608340
1E6   04 7041    838          AOR   MR0              ADDRESS THE ASCII CONSOLE   51608350
1E7   04 7903    839          LI    MR0,3                                        51608360
1E8   04 7042    840          OC    MR0              ISSUE RESET COMMAND         51608370
1E9   7B A900    841          B     DELAY1           (P.24)                      51608380
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SHIFT INSTRUCTIONS

```
1EA     A4 6C60     843  SLRF1   A     LOC,LOC,Q,MR        FETCH A-FIELD                          51608420
1EB     04 7832     844          L     MR0,MEM,YDP1                                               51608430
1EC     04 5845     845          A     MR0,MR0,X2          PERFORM INDEXING IF SPECIFIED          51608440
1ED     00 7640     846          I     Q,MR0               SHIFT COUNT TO Q REGISTER              51608450
1EE     06 691F     847          NI    MR0,'1F',Q          MASK LS 5 BITS                         51608460
1EF     00 3623     848          L     Q,YD,YDM1                                                  51608470
1F0     45 7847     849          DFCE  MR0,MR0,NULL,D2     DECREMENT WITH FLAGS...VECTOR          51608480
                    850  *                                THRU DROM2 TO SLL,SRL,RLL OR RRL       51608490
                    851  *                                                                       51608500
                    852  *                                                                       51608510
 01F1               853  SLL     EQU   *                   SHIFT LEFT LOGICAL          * ED *     51608520
                    854  *                                                                       51608530
1F1     67 2006     855          BT    L,EXIT3,REFRESH     EXIT IF COUNT MINUS                    51608540
                    856  *                                Q CONTAINS LS 16 BITS                  51608550
1F2     19 B02A     857          ISL   YD&Q,YD,C0          SHIFT LEFT YD AND Q                    51608560
1F3     45 7847     858          DFCE  MR0,MR0,NULL,D2     DECREMENT COUNT, LOOP THRU DROM2       51608570
                    859  *                                                                       51608580
 01F4               860  SRL     EQU   *                   SHIFT RIGHT LOGICAL         * EC *     51608590
                    861  *                                                                       51608600
1F4     67 2006     862          BT    L,EXIT3,REFRESH     EXIT IF COUNT MINUS                    51608610
1F5     11 B02A     863          ISR   YD&Q,YD,C0          SHIFT RIGHT YD AND Q                   51608620
1F6     45 7847     864          DFCE  MR0,MR0,NULL,D2     DECREMENT COUNT, LOOP THRU DROM2       51608630
                    865  *                                                                       51608640
 01F7               866  RLL     EQU   *                   ROTATE LEFT LOGICAL         * EB *     51608650
                    867  *                                                                       51608660
1F7     67 1FF6     868          BT    L,EXIT3.1,REFRESH   EXIT IF COUNT MINUS                    51608670
1F8     19 B02B     869          ISL   YD&Q,YD,CI+C0       ROTATE LEFT YD AND Q                   51608680
1F9     45 7847     870          DFCE  MR0,MR0,NULL,D2     DECREMENT COUNT, LOOP THRU DROM2       51608690
                    871  *                                                                       51608700
 01FA               872  RRL     EQU   *                   ROTATE RIGHT LOGICAL        * EA *     51608710
                    873  *                                                                       51608720
1FA     67 1FF6     874          BT    L,EXIT3.1,REFRESH   EXIT IF COUNT MINUS                    51608730
1FB     11 B02B     875          ISR   YD&Q,YD,CI+C0       ROTATE RIGHT YD AND Q                  51608740
1FC     45 7847     876          DFCE  MR0,MR0,NULL,D2     DECREMENT COUNT, LOOP THRU DROM2       51608750
                    877  *                                                                       51608760
1FD                 878          ORG   '1FF'                                                     51608770
1FF     04 784A     879  EXIT3.1 L     MR0,MR0,C0          CLEAR CARRY FLAG                       51608780
                    880  *                                EXIT 3 FOR SLL,SRL,RLL,RRL             51608790
                    881  *                                                                       51608800
200     04 2822     882  EXIT3   L     MR0,Q,YDP1          LS 16 BITS TO MR0                      51608810
201     63 A070     883          BT    C,EXIT3A            BRANCH IF CARRY FROM SHIFT             51608820
202     04 7500     884          LT    FLR,0               CLEAR FLAGS                            51608830
203     0C 704C     885          L     YD,MR0,F            LOAD LS 16 BITS, ADJUST FLAGS          51608840
204     04 7843     886          L     MR0,MR0,YDM1        POINTING TO R1                         51608850
205     0C 302C     887          L     YD,YD,F             LOAD MS 16 BITS, ACCUMULATE FLAGS      51608860
206     7B 83A0     888          B     EXIT1A              (P.3)                                  51608870
207     04 7508     889  EXIT3A  LT    FLR,8               CLEAR FLAGS EXCEPT CARRY               51608880
208     0C 704C     890          L     YD,MR0,F            LOAD LS 16 BITS, ADJUST FLAGS          51608890
209     04 7843     891          L     MR0,MR0,YDM1        POINTING TO R1                         51608900
20A     0C 302C     892          L     YD,YD,F             LOAD MS 16 BITS ADJUST G & L           51608910
20B     7B 83A0     893          B     EXIT1A              (P.3)                                  51608920
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SHIFT INSTRUCTIONS

```
20C     A4 6C60     895   SLRA1   A     LOC,LOC,Q,MR      FETCH A-FIELD                          51608940
20D     04 7830     896           L     MR0,MEM                                                  51608950
20F     04 5845     897           A     MR0,MR0,X2        PERFORM INDEXING IF SPECIFIED          51608960
20F     00 7640     898           L     Q,MR0                                                    51608970
210     06 691F     899           NI    MR0,'1F',0        MASK LS 5 BITS                         51608980
211     04 7B80     900           LI    MAR,'80'                                                 51608990
212     04 7ADA     901           L     MAR,MAR,CS+C0     MAR=X'8000'...RESET CARRY              51609000
213     06 5A52     902           N     MAR,MAR,YD,YDP1   MAR = SIGN BIT OF R1                  51609010
214     00 3623     903           L     Q,YD,YDM1         Q=LS 16 BITS, POINT TO R1              51609020
215     19 B020     904           LSL   YD&Q,YD           PRESHIFT                               51609030
216     45 7847     905           DECF  MR0,MR0,NULL,D2   DECREMENT COUNT, JUMP THRU DROM2       51609040
                    906   *                                                                      51609050
                    907   *                                                                      51609060
                    908   *                                                                      51609070
 0217               909   SLA     EQU   *                 SHIFT LEFT ARITHMETIC        * EF *  51609080
                    910   *                                                                      51609090
217     67 21E6     911           BT    L,EXIT6,REFRESH   EXIT IF COUNT MINUS                   51609100
218     19 B02A     912           LSL   YD&Q,YD,C0        SHIFT LEFT YD AND Q                    51609110
219     45 7847     913           DECF  MR0,MR0,NULL,D2   DECREMENT COUNT, LOOP THRU DROM2       51609120
                    914   *                                                                      51609130
 021A               915   SRA     EQU   *                 SHIFT RIGHT ARITHMETIC       * EE *  51609140
                    916   *                                                                      51609150
21A     67 22C6     917           BT    L,EXIT7,REFRESH   EXIT IF COUNT MINUS                   51609160
21B     11 B020     918           LSR   YD&Q,YD           SHIFT RIGHT YD AND Q                   51609170
21C     0D D050     919           O     YD,MAR,YD         PROPOGATE SIGN                         51609180
21D     45 7847     920           DECF  MR0,MR0,NULL,D2   DECREMENT COUNT, LOOP THRU DROM2       51609190
                    921   *                                                                      51609200
                    922   *                                                                      51609210
                    923   *                                                                      51609220
21E     11 B020     924   EXIT6   LSR   YD&Q,YD           COMPENSATE PRE-SHIFT                   51609230
21F     63 A262     925   EXIT6,7 BT    C,EXIT6A,YDP1     BRANCH IF CARRY                        51609240
220     04 7500     926           LI    FLR,0             CLEAR FLAGS                            51609250
221     0D A02C     927   EXIT7B  O     YD,NULL,Q,F       LOAD R1+1, SET FLAGS                   51609260
222     04 7843     928           L     MR0,MR0,YDM1      POINTING TO R1                         51609270
223     0D D05C     929           O     YD,MAR,YD,F       INSERT SIGN BIT, SET FLAGS             51609280
224     00 7702     930           LI    Q,2               RESTORE Q                              51609290
225     E4 6C60     931           A     LOC,LOC,Q,IRJ                                            51609300
226     04 7508     932   EXIT6A  LI    FLR,8             CLEAR FLAGS EXCEPT CARRY               51609310
227     0D A02C     933           O     YD,NULL,Q,F       LOAD R1+1, SET FLAGS                   51609320
228     04 7843     934           L     MR0,MR0,YDM1      POINTING TO R1                         51609330
229     0D D05C     935           O     YD,MAR,YD,F       INSERT SIGN, SET FLAGS                 51609340
22A     00 7702     936           LI    Q,2               RESTORE Q REGISTER                     51609350
22B     E4 6C60     937           A     LOC,LOC,Q,IRJ                                            51609360
                    938   *                                                                      51609370
22C     11 B02A     939   EXIT7   LSR   YD&Q,YD,C0        COMPENSATE PRESHIFT                    51609380
22D     7B A1F0     940           B     EXIT6,7                                                  51609390
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LIST PROCESSING INSTRUCTIONS

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22F  A4 6C60   942  ATBL1  A    LOC,LOC,Q,MR      FETCH A-FIELD OF INSTRUCTION          51609410
22F  04 7830   943         L    MR0,MEM                                                 51609420
230  04 5845   944         A    MR0,MR0,X2        PERFORM INDEXING IF SPECIFIED         51609430
231  A4 7A40   945         L    MAR,MR0,MR        FETCH MAX.SLOT/NO.USED                51609440
232  04 7E30   946         L    MDR,MEM                                                 51609450
               947  *                             MDR = MAX.SLOT/NO.USED                51609460
233  00 76F0   948         L    Q,MDR,CS          Q  = NO. USED / MAX.SLOT              51609470
234  04 E67A   949         S    NULL,Q,MDR,CO     NO.USED MINUS MAX SLOT                51609480
235  63 E4E6   950         BF   C,LSTOVF,REFRESH  OVERFLOW IF NO CARRY          R01    51609490
236  06 69FF   951         NI   MR0,'FF',Q        MR0=    0     / MAX.SLOT             51609500
237  04 7E74   952         INC  MDR,MDR,NULL      INCREMENT NO.USED TALLY               51609510
238  00 7702   953         LI   Q,2                                                     51609520
239  84 6A50   954         A    MAR,MAR,Q,MW      RE-WRITE MAX.SLOT/NO. USED            51609530
23A  04 7670   955         L    MEM,MDR           INCREMENT MAR                         51609540
23B  A4 7A50   956         L    MAR,MAR,MR        FETCH CUR.TOP/NEXT BOT                51609550
23C  44 7E30   957         L    MDR,MEM,D2        THRU DROM2 TO ATL OR ABL (P.23)       51609560

23D  A4 6C60   959  RTBL1  A    LOC,LOC,Q,MR      FETCH A-FIELD OF INSTRUCTION          51609580
23F  04 7830   960         L    MR0,MEM                                                 51609590
23F  04 5845   961         A    MR0,MR0,X2        PERFORM INDEXING IF SPECIFIED         51609600
240  A4 7A40   962         L    MAR,MR0,MR        FETCH MAX. SLOT/NO. USED              51609610
241  04 7E30   963         L    MDR,MEM                                                 51609620
               964  *                             MDR = MAX.SLOT/NO.USED                51609630
242  00 7670   965         L    Q,MDR             COPY TO Q                             51609640
243  02 67FF   966         NI   Q,'FF',Q          NUMBER USED TALLY                     51609650
244  00 A627   967         DFC= Q,Q,NULL          DECREMENT & TEST                      51609660
245  67 24E6   968         RT   L,LSTOVF,REFRESH  DECREMENT NO. USED           R01    51609670
246  05 7E74   969         DEC  MDR,MDR,NULL      FLAGS INDICATE ZERO OR GREATER        51609680
247  00 76F0   970         L    Q,MDR,CS          FOR EMPTY NOW OR NOT EMPTY            51609690
248  06 69FF   971         NI   MR0,'FF',Q        MR0=MAX.SLOT                          51609700
249  00 7702   972         LI   Q,2                                                     51609710
24A  84 6A50   973         A    MAR,MAR,Q,MW      RE-WRITE MAX.SLOT/NO.USED             51609720
24B  04 7670   974         L    MEM,MDR           INCREMENT MAR                         51609730
24C  A4 7A50   975         L    MAR,MAR,MR        FETCH CURRENT TOP/NEXT BOTTOM         51609740
24D  44 7E30   976         L    MDR,MEM,D2        THRU DROM2 TO RTL OR RBL (P.24)       51609750
               977  *                                                                   51609760
               978  *                                                                   51609770
24F  04 7504   979  LSTOVF LI   FLR,4             SET V FLAG                            51609780
24F  00 7702   980         LI   Q,2               PRESET Q = CONSTANT 2                 51609790
250  E4 6C60   981         A    LOC,LOC,Q,IRJ     FETCH NEXT INSTRUCTION                51609800
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LIST PROCESSING INSTRUCTIONS

```
 0251                    983  ATL     EQU  *                ADD TO TOP OF LIST          * 64 *  51609820
                         984  *                                                                   51609830
251      00 76F0        985  ATL1    L    Q,MDR,CS         Q = CURRENT TOP POINTER               51609840
252      02 67FF        986          NI   Q,'FF',Q                                              51609850
253      00 262C        987          L    Q,Q,F            TEST IF ZERO                         51609860
254      66 E560        988          BF   G,ATL2           NO WRAP IF NOT ZERO                  51609870
255      04 2820        989          L    MR0,Q            LIST WRAP, SET NEW CURRENT TOP       51609880
256      05 7844        990  ATL2    DEC  MR0,MR0,NULL     POINTER EQUAL TO MAX.SLOT -1         51609890
257      04 7EC0        991          L    MDR,MR0,CS       INSERT NEW POINTER                   51609900
258      84 7A50        992          L    MAR,MAR,MW       STORE IT                             51609910
259      04 7670        993          L    MEM,MDR                                               51609920
25A      00 7640        994          L    Q,MR0            USE NEW VALUE FOR CURRENT TOP        51609930
25B      04 6901        995  ADDIT   AI   MR0,'1',Q         Q CONTAINS TARGET SLOT NUMBER        51609940
25C      00 6844        996          INC  MR0&Q,MR0,Q      FORM 2Q+2                            51609950
25D      04 6A56        997          A    MAR,MAR,Q,REFRESH ADD TO MEMORY ADDRESS          R01 51609960
25E      00 7702        998          LI   Q,2              RESTORE Q...CONSTANT 2               51609970
25F      04 3820        999          L    MR0,YL           MR0 = ELEMENT TO ADD                 51609980
260      84 7A50       1000          L    MAR,MAR,MW       TAKE HALFWORD ELEMENT FROM R1        51609990
261      04 7640       1001          L    MEM,MR0          AND STORE IN DESIGNATED SLOT         51610000
262      04 7500       1002          LI   FLR,0            CLEAR FLAGS                          51610010
263      E4 6C60       1003          A    LOC,LOC,Q,IRJ    EXIT                                 51610020
                       1004  *                                                                   51610030
                       1005  *                                                                   51610040
 0264                  1006  ABL     EQU  *                ADD TO BOTTOM OF LIST       * 65 *  51610050
                       1007  *                                                                   51610060
264      00 7670       1008  ABL1    L    Q,MDR                                                 51610070
265      02 67FF       1009          NI   Q,'FF',Q         Q=NEXT BOTTOM POINTER                51610080
266      04 7A54       1010          INC  MAR,MAR,NULL     MAKE MAR ODD                         51610090
267      05 6647       1011          DEC  NULL,MR0,Q       COMPARE NEXT BOTTOM TO MAX           51610100
268      66 66E0       1012          BF   G+L,ABL3         LIST WRAP IF EQUAL                   51610110
269      04 2824       1013          INC  MR0,NULL,Q       NO WRAP...NEXT BOTTOM PLUS 1         51610120
26A      04 7EC0       1014  ABL2    L    MDR,MR0,CS       INSERT UPDATED POINTER               51610130
26B      85 7A54       1015          DEC  MAR,MAR,NULL,MW  STORE...PUT MAR BACK EVEN           51610140
26C      04 7670       1016          L    MEM,MDR                                               51610150
26D      7B A5B0       1017          B    ADDIT                                                 51610160
26F      04 7900       1018  ABL3    LI   MR0,0            IF WRAP, NEXT BOTTOM = 0             51610170
26F      7B A6A0       1019          B    ABL2                                                  51610180
```

LIST PROCESSING INSTRUCTIONS

```
 0270                   1021   RTL     EQU   *                 REMOVE FROM TOP OF LIST      * 66 *  51610200
                        1022   *                                                                      51610210
270     00 76F4        1023   RTL1    INC   Q,MDR,NULL,CS      Q = CURRENT TOP +1                    51610220
271     02 67FF        1024           NI    Q,'FF',Q                                                 51610230
272     04 E64A        1025           S     NULL,Q,MR0,CO       COMPARE CURRENT TOP TO MAX           51610240
273     63 A7B0        1026           BT    C,RTL3              NO WRAP IF LESS THAN LIMIT           51610250
274     00 7640        1027           L     Q,MR0               LIST WRAP, Q GETS MAX SLOT           51610260
275     04 7900        1028           LI    MR0,0               MR0 = NEW CURRENT TOP = 0            51610270
276     04 7EC0        1029   RTL2    L     MDR,MR0,CS          INSERT NEW CURRENT TOP POINTER       51610280
277     84 7A50        1030           L     MAR,MAR,MW          START MEMORY WRITE                   51610290
278     04 7670        1031           L     MEM,MDR             STORE CURRENT TOP/NEXT BOTTOM        51610300
279     00 A624        1032           DEC   Q,Q,NULL            Q=TARGET SLOT NUMBER                 51610310
27A     7B A876        1033           B     REMOVE,REFRESH      COMMON CODE                  R01     51610320
27B     04 2820        1034   RTL3    L     MR0,Q               NO WRAP, INCREMENT CURRENT TOP       51610330
27C     7B A760        1035           B     RTL2                                                     51610340
                        1036   *                                                                      51610350
                        1037   *                                                                      51610360
 027D                   1038   RBL     EQU   *                 REMOVE FROM BOTTOM OF LIST   * 67 *  51610370
                        1039   *                                                                      51610380
27D     00 7670        1040   RBL1    L     Q,MDR                                                    51610390
27F     02 67FF        1041           NI    Q,'FF',Q            Q=NEXT BOTTOM POINTER                51610400
27F     00 A624        1042           DEC   Q,Q,NULL            DECREMENT & TEST                     51610410
280     63 E820        1043           BF    C,RBL2              NO WRAP IF NOT LESS THAN ZERO        51610420
                        1044   *                                LIST WRAP  SET NEXT BOTTOM           51610430
281     01 7844        1045           DEC   MR0&Q,MR0,NULL      POINTER = MAX SLOT - 1               51610440
282     04 2826        1046   RBL2    L     MR0,Q,REFRESH       MR0 & Q = NEW NEXT BOTTOM    R01     51610450
283     04 7A54        1047           INC   MAR,MAR,NULL        MAKE MAR ODD                         51610460
284     04 7EC0        1048           L     MDR,MR0,CS          INSERT NEW NEXT BOTTOM POINTER       51610470
285     85 7A54        1049           DEC   MAR,MAR,NULL,MW     START MEMORY WRITE                   51610480
286     04 7670        1050           L     MEM,MDR             STORE UPDATED POINTER                51610490
 0287                   1051   REMOVE  EQU   *                 Q CONTAINS TARGET SLOT NUMBER        51610500
287     04 6901        1052           AI    MR0,'1',Q                                                51610510
288     00 6844        1053           INC   MR0&Q,MR0,Q         FORM 2Q+2                            51610520
289     04 6A50        1054           A     MAR,MAR,Q           ADD TO MEMORY ADDRESS                51610530
28A     A4 7A50        1055           L     MAR,MAR,MR          FETCH ELEMENT FROM LIST              51610540
28B     04 7E30        1056           L     MDR,MEM             COPY TO MDR                          51610550
28C     0C 707A        1057           L     YD,MDR,CO           PASS ON TO R1, CLEAR CARRY           51610560
28D     00 7702        1058           LI    Q,2                 RESTORE Q...CONSTANT 2               51610570
28F     E4 6C60        1059           A     LOC,LOC,Q,IRJ       FETCH NEXT, INCREMENT LOC            51610580
                        1060   *                                                                      51610590
28F     00 0000        1061           DC    0                   FILLER                               51610600
290     6E A906        1062   DELAY1  BT    CATN,*,REFRESH      WAIT FOR NO CATN             R01     51610610
291     7B 94A0        1063           B     CONSER              (P,16)                               51610620
```

SUPERVISOR CALL

```
292   84 7B94   1065  SVC1   LT   MAR,'94',MW                                          51610640
293   04 7640   1066         L    MEM,MR0          STORE A+(X2) AT '0094'            51610650
294   84 7B96   1067         LT   MAR,'96',MW                                        51610660
295   04 7610   1068         L    MEM,PSW          STORE OLD PSW AT '0096'           51610670
296   84 7B98   1069         LT   MAR,'98',MW                                        51610680
297   04 7660   1070         L    MEM,LOC          STORE OLD LOC AT '0098'           51610690
298   04 7920   1071         LT   MR0,'20'         PRESET MR0 = 32                   51610700
299   05 6842   1072  SVC1A  S    MR0,MR0,Q,YDP1   INCREMENT YD FIELD UNTIL IT      51610710
                1073  *                           WRAPS FROM F TO 0.,DECREMENT      51610720
29A   77 6996   1074         BF   YDCARY,SVC1A,REFRESH MR0 BY TWO EACH TIME         51610730
29B   A4 7B9A   1075  SVC2   LT   MAR,'9A',MR                                       51610740
29C   04 7E30   1076         L    MDR,MEM                                           51610750
29D   04 7270   1077         L    PSW,MDR          LOAD NEW PSW                     51610760
29E   00 7640   1078         L    Q,MR0            FETCH ONE OF 16 NEW LOC'S,       51610770
29F   04 699C   1079         AT   MR0,'9C',Q       SELECTED FROM LOCATION '9C'      51610780
2A0   A4 7A40   1080         L    MAR,MR0,MR       PLUS TWICE THE R1 FIELD          51610790
2A1   04 7C30   1081         L    LOC,MEM          LOAD NEW LOC                     51610800
2A2   00 7702   1082         LT   Q,2                                               51610810
2A3   7B 81D6   1083         B    EXIT1,REFRESH    (P,2)                     R01    51610820
2A4   00 0000   1084         DC   0                FILLER                           51610830
2A5   00 0000   1085         DC   0                FILLER                           51610840
```

BLOCK INPUT/OUTPUT

```
2A6     A4 6C60     1087    AL1     A       LOC,LOC,Q,MR        DROM 1 ENTRY POINT, FINISH          51610A60
2A7     04 7830     1088            L       MR0,MEM             INSTRUCTION FETCH                   51610A70
2A8     04 5845     1089            A       MR0,MR0,X2          FORM FINAL ADDRESS                  51610A80
2A9     A4 7B78     1090            LI      MAR,'78',MR         FETCH BINARY INPUT DEVICE SPECS.    51610A90
2AA     04 7E30     1091            L       MDR,MEM                                                 51610900
2AB     00 7780     1092            LI      Q,'80'              Q=START ADDRESS                     51610910
2AC     01 664A     1093            S       Q,MR0,Q,CO          END ADRS MINUS START ADRS           51610920
2AD     63 AD80     1094            BT      C,FINISH            LEAVE IF START GREATER (P.27)       51610930
2AE     04 78F0     1095            L       MR0,MDR,CS          DEVICE NUMBER DOWN                  51610940
2AF     04 7B80     1096            LI      MAR,'80'            START ADDRESS TO MAR                51610950
2B0     04 7041     1097            AIR     MR0                 ADDRESS THE DEVICE                  51610960
2B1     04 7072     1098            OC      MDR                 ISSUE OUTPUT COMMAND                51610970
2B2     04 7F00     1099            LI      MDR,0               CLEAR MDR                           51610975
2B3     04 7402     1100    LEADER  SS      FLR                 SENSE STATUS                        51610980
2B4     64 2D90     1101            BT      V+G+L,TERMIN        LEAVE ON BAD STATUS (P.27)          51610990
2B5     63 AB36     1102            BT      C,LEADER,REFRESH    LOOP IF JUST BUSY                   51611000
2B6     04 7E84     1103            RD      MDR,CS              INPUT BYTE TO MDR <0:7>             51611010
2B7     04 787C     1104            L       MR0,MDR,F           TEST MDR                            51611020
2B8     66 6B30     1105            BF      G+L,LEADER          LOOP IF ZERO                        51611030
                    1106    *                                                                       51611040
2B9     7B AD40     1107            B       STARTAL             (P.27)                              51611050
```

BLOCK INPUT/OUTPUT

```
28A     04 3021     1109  RWBRR   ADR   YD              ADDRESS THE DEVICE                51611070
28B     04 7E40     1110          L     MDR,MR0         MDR = START ADDRESS               51611080
28C     04 7821     1111          L     MR0,YSI,CLRYD                                     51611090
28D     04 7842     1112  BLKRR   L     MR0,MR0,YDP1    MAKE R1 & R2 FIELDS ALIKE         51611100
28F     05 7844     1113          DFC   MR0,MR0,NULL                                      51611110
28F     63 EBD6     1114          BF    C,BLKRR,REFRESH                                   51611120
2C0     04 3820     1115          L     MR0,YD          END ADDRESS TO MR0                51611130
2C1     7B ACA0     1116          B     BLOCK1                                            51611140
                    1117  *                                                               51611150
                    1118  *                                                               51611160
                    1119  *                                                               51611170
2C2     04 3021     1120  RWBRX   ADR   YD              ADDRESS THE DEVICE                51611180
2C3     A4 6C60     1121          A     LOC,LOC,Q,MR    FINISH INSTRUCTION FETCH          51611190
2C4     04 7830     1122          L     MR0,MEM                                           51611200
2C5     04 5845     1123          A     MR0,MR0,X2      PERFORM INDEXING IF SPECIFIED     51611210
2C6     A4 6A40     1124          A     MAR,MR0,Q,MR    FETCH START ADDRESS               51611220
2C7     04 7E30     1125          L     MDR,MEM         MDR = START ADDRESS               51611230
2C8     A4 7A50     1126          L     MAR,MAR,MR      FETCH END ADDRESS                 51611240
2C9     04 7830     1127          L     MR0,MEM         MR0 = END ADDRESS                 51611250
                    1128  *                                                               51611260
2CA     00 7A70     1129  BLOCK1  L     MAR,Q,MDR       START ADDRESS TO MAR & Q          51611270
2CB     01 664A     1130          S     Q,MR0,Q,CO      END MINUS START                   51611280
2CC     63 AD80     1131          BT    C,FINISH        LEAVE IF START GREATER            51611290
                    1132  *                                                               51611300
2CD     A4 7A50     1133  BLOCK2  L     MAR,MAR,MR      FETCH EVEN/ODD BYTE PAIR          51611310
2CE     04 7E30     1134          L     MDR,MEM                                           51611320
2CF     04 7402     1135  BLOCK3  SS    FLR             SENSE STATUS                      51611330
2D0     64 2D90     1136          BT    V+G+L,TERMIN    LEAVE IF BAD STATUS               51611340
2D1     63 ACF6     1137          BT    C,BLOCK3,REFRESH LOOP IF JUST BUSY                51611350
2D2     40 2620     1138          L     Q,G,D2                                            51611360
                    1139  *                                                               51611370
2D3     04 7E84     1140  RB.D2   RD    MDR,CS          INPUT DATA BYTE                   51611380
2D4     84 7A54     1141  STARTAL INC   MAR,MAR,NULL,MW                                   51611390
2D5     04 7670     1142          L     MEM,MDR         STORE                             51611400
2D6     00 A624     1143          DFC   Q,Q,NULL        DECREMENT BYTE COUNT              51611410
2D7     63 ECD0     1144          BF    C,BLOCK2                                          51611420
2D8     04 7500     1145  FINISH  LI    FLR,0           NORMAL EXIT,CLEAR FLAGS           51611430
2D9     00 7702     1146  TERMIN  LI    Q,2                                               51611440
2DA     E4 6C60     1147          A     LOC,LOC,Q,IRJ                                     51611450
                    1148  *                                                               51611460
2DB     04 70F4     1149  WB.D2   WD    MDR,CS          OUTPUT DATA BYTE                  51611470
2DC     04 7A54     1150          INC   MAR,MAR,NULL    INCREMENT MEMORY ADDRESS          51611480
2DD     00 A624     1151          DFC   Q,Q,NULL        DECREMENT COUNT                   51611490
2DE     63 ECD0     1152          BF    C,BLOCK2                                          51611500
2DF     7B AD80     1153          B     FINISH                                            51611510
```

HALFWORD IO

```
2E0   04 7804   1155  RHB    RD   MR0              INPUT FIRST BYTE                          51611530
2E1   04 7E04   1156         RD   MDR              INPUT SECOND BYTE                         51611540
2E2   04 7EC0   1157         L    MDR,MR0,CS       COMBINE                                   51611550
2E3   84 7A50   1158         I    MAR,MAR,MW                                                 51611560
2E4   04 7670   1159         I    MEM,MDR          STORE                                     51611570
2E5   E4 6C60   1160         A    LOC,LOC,Q,IRJ    FECTH NEXT INSTRUCTION                    51611580
2E6   7D AFE0   1161  RHR1   BT   HWIO,RHRH                                                  51611590
2E7   04 7B00   1162  RHRB   LI   MAR,0             FORCE MAR EVEN                            51611600
2E8   04 7E84   1163         RD   MDR,CS           INPUT FIRST BYTE                          51611610
2E9   04 7B01   1164         LI   MAR,1            ODD BYTE                                  51611620
2EA   04 7E84   1165         RD   MDR,CS           INPUT SECOND BYTE                         51611630
2EB   0C 7270   1166         L    YS,MDR           HALFWORD TO R2                            51611640
2EC   E4 6C60   1167         A    LOC,LOC,Q,IRJ                                              51611650
2ED   04 7AC0   1168  WHB    L    MAR,MR0,CS                                                 51611660
2EF   04 7054   1169         WD   MAR              OUTPUT FIRST BYTE                         51611670
2EF   04 7044   1170         WD   MR0              OUTPUT SECOND BYTE                        51611680
2F0   E4 6C60   1171         A    LOC,LOC,Q,IRJ                                              51611690
              1172  *                                                                        51611700


2F1   06 2A21   1174  BEGIN  N    MAR,NULL,Q,CLRYD  MAR AND YD FIELD GET ZERO               51611720
2F2   00 7702   1175         LI   Q,2                                                        51611730
2F3   A4 6A50   1176  GETREG A    MAR,MAR,Q,MR      FETCH REGISTER                          51611740
2F4   04 7E30   1177         L    MDR,MEM           COPY TO MDR                             51611750
2F5   0C 7072   1178         L    YD,MDR,YDP1       COPY FROM MDR TO GENERAL REGISTER       51611760
2F6   77 6F30   1179         BF   YDCARY,GETREG     LOOP                                    51611770
2F7   A4 7B24   1180         LI   MAR,'24',MR                                               51611780
2F8   04 7830   1181         L    MR0,MEM                                                    51611790
2F9   04 7240   1182         L    PSW,MR0           LOAD PSW                                51611800
2FA   A4 7B26   1183         LI   MAR,'26',MR                                               51611810
2FB   04 7C30   1184         L    LOC,MEM           LOAD LOC                                51611820
2FC   6E AFC6   1185         BT   CATN,*,REFRESH    WAIT FOR NO CATN          R01           51611830
2FD   7B 9360   1186         B    TEST2             GO TO WAIT OR RUN (P.14)                51611834
2FE   0C 7204   1187  RHRH   RD   YS                HALFWORD TO R2                          51611835
2FF   E4 6C60   1188         A    LOC,LOC,Q,IRJ                                              51611836
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300                     1190            ORG   '300'                                                    51611850
                        1191    *                                                                      51611860
                        1192    *  SIGNED MULTIPLY                                                     51611870
                        1193    *                                                                      51611880
300     04 7B00         1194    MH1     LT    MAR,0          CLEAR FLAG                                51611890
301     0C 3022         1195            I     YD,YD,YDP1     INCREMENT R1 FIELD                        51611900
302     00 362C         1196            L     Q,YD,F         Q GETS MULTIPLICAND, SET FLAGS            51611910
303     67 7060         1197            BF    L,MH.0010      SKIP IF NOT NEGATIVE                      51611920
304     04 7A54         1198            INC   MAR,MAR,NULL   INCREMENT FLAG                           51611930
305     01 2620         1199            S     Q,NULL,Q       TWO'S COMPLIMENT MULTIPLICAND             51611940
306     04 784C         1200    MH.0010 L     MR0,MR0,F      TEST MULTIPLIER                           51611950
307     67 70A0         1201            BF    L,MH.0011      SKIP IF NOT NEGATIVE                      51611960
308     04 F840         1202            S     MR0,NULL,MR0   TWO'S COMPLIMENT MULTIPLIER               51611970
309     04 7A54         1203            INC   MAR,MAR,NULL   INCREMENT FLAG                           51611980
30A     04 7843         1204    MH.0011 L     MR0,MR0,YDM1   POINT BACK TO R1                        51611990
30B     0C 7100         1205            LT    YD,0           CLEAR MS PRODUCT                          51612000
30C     04 7F10         1206            LT    MDR,16         MDR IS COUNTER                            51612010
                        1207    *                                                                      51612020
30D     11 B02A         1208    MH.0020 ISR   YD&Q,YD,C0     YD,Q RIGHT ONE BIT POSITION               51612030
                        1209    *                           CARRY EQUALS MULTIPLICAND BIT             51612040
30E     63 F100         1210            BF    C,MH.0021      NO MULTIPLY IF ZERO                       51612050
30F     0C 504A         1211            A     YD,MR0,YD,C0   IF SET, ADD MULTIPLIER                   51612060
310     05 7E77         1212    MH.0021 DFCE  MDR,MDR,NULL   DECREMENT COUNT                          51612070
311     67 70D6         1213            BF    L,MH.0020,REFRESH  LOOP UNTIL COUNT GOES NEGATIVE         51612080
312     04 7450         1214            I     FLR,MAR        TEST RESULT SIGN                          51612090
313     67 7182         1215            BF    L,MH.0030,YDP1 SKIP IF POSITIVE                          51612100
                        1216    *                           POINTING TO R1+1                          51612110
314     0D 202A         1217            S     YD,NULL,Q,C0   TWO'S COMP LS 16 BITS                     51612120
315     04 7843         1218            L     MR0,MR0,YDM1   POINTING TO R1                            51612130
316     0D 3029         1219            S     YD,NULL,YD,CI  TWO'S COMP MS 16 BITS                     51612140
317     7B B196         1220            B     EXIT.MD,REFRESH  EXIT                          R01       51612150
318     0C 2026         1221    MH.0030 L     YD,Q,REFRESH   LOAD LS 16 BITS                  R01       51612160
319     00 7702         1222    EXIT.MD LT    Q,2            RESTORE Q TO CONSTANT 2                   51612170
31A     04 7410         1223            L     FLR,PSW        NO CC CHANGE                              51612180
31B     E4 6C60         1224            A     LOC,LOC,Q,IRJ  FETCH NEXT                                51612190
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                        1226    *  UNSIGNED MULTIPLY                                                    51612210
                        1227    *                                                                       51612220
310     0C 3022         1228    MHU1        L       YD,YD,YDP1          POINT TO R1+1                   51612230
311     00 3623         1229                L       Q,YD,YDM1           Q GETS MULTIPLICAND             51612240
312     0C 7100         1230                LI      YD,0                CLEAR MS PRODUCT                51612250
313     04 7F10         1231                LI      MDR,16              MDR IS COUNTER                  51612260
314     11 B024         1232    MHU.0010    LSR     YD&Q,YD,JAM         33 BIT ROTATE ONE POSITION      51612270
315     63 F230         1233                BF      C,MHU.0011          NO MULTIPLY IF Q BIT 15 RESET   51612280
316     0C 504A         1234                A       YD,MR0,YD,CO        IF SET, ADD MULTIPLIER          51612290
317     05 7E77         1235    MHU.0011    DFCF    MDR,MDR,NULL        DECREMENT COUNT                 51612300
318     67 7206         1236                BF      L,MHU.0010,REFRESH  LOOP UNTIL COUNT GOES NEGATIVE  51612310
319     7B B182         1237                B       MH.0030,YDP1        LOAD RESULT THEN EXIT (P.29)    51612320

                        1239    *  DIVIDE                                                               51612340
                        1240    *                                                                       51612350
31A     04 3E22         1241    DH1         L       MDR,YD,YDP1                                         51612360
31B     84 7B24         1242                LI      MAR,'24',MW                                         51612370
31C     04 7670         1243                L       MEM,MDR             SAVE R1 AT '0024'               51612380
31D     04 3E20         1244                L       MDR,YD                                              51612390
31E     84 7B26         1245                LI      MAR,'26',MW                                         51612400
31F     04 7670         1246                L       MEM,MDR             SAVE R1+1 AT '0026'             51612410
320     04 7B01         1247                LI      MAR,1               PRESET FLAG                     51612420
321     04 784C         1248                I       MR0,MR0,F           TEST DIVISOR                    51612430
322     67 3326         1249                BT      L,DH.0010,REFRESH   BRANCH IF NEGATIVE        R01     51612440
323     66 F590         1250                BF      G,DEFAULT1          ERROR IF ZERO (P.31)            51612450
324     04 F840         1251                S       MR0,NULL,MR0        TWO'S COMPLIMENT IF POSITIVE    51612460
325     04 7B00         1252                LI      MAR,0               CLEAR FLAG                      51612470
326     00 3623         1253    DH.0010     I       Q,YD,YDM1           Q GETS LS DIVIDEND              51612480
327     04 7500         1254                LI      FLR,0                                               51612490
328     00 262C         1255                L       Q,0,F               TEST LS 16 BITS IF DIVIDEND     51612500
329     0C 302C         1256                L       YD,YD,F             TEST MS DIVIDEND                51612510
32A     66 7190         1257                BF      G+L,EXIT,MD         RESULT = DIVIDEND = ZERO (P.29) 51612520
32B     67 73C0         1258                BF      L,DH.0020           SKIP IF NOT NEGATIVE            51612530
32C     04 7A54         1259                INC     MAR,MAR,NULL        MAR15=DIVISOR SIGN              51612540
32D     04 7A54         1260                INC     MAR,MAR,NULL        MAR14=DIVIDEND SIGN             51612550
32E     01 262A         1261                S       Q,NULL,Q,CO         TWO'S COMP DIVIDEND             51612560
32F     0D 3029         1262                S       YD,NULL,YD,CI                                       51612570
330     04 564A         1263    DH.0020     A       NULL,MR0,YD,CO      TRIAL SUBTRACT                  51612580
331     63 B530         1264                BT      C,DEFAULT           ERROR...QUOTIENT OVERFLOW (P.31) 51612590
332     04 7F10         1265                LI      MDR,16              MDR = COUNTER                   51612600
333     0C 504A         1266    DH.0030     A       YD,MR0,YD,CO        SUBTRACT DIVISOR & MS DIVIDEND  51612610
334     63 B420         1267                BT      C,DH.0031           OK IF SUCCESSFUL SUBTRACT       51612620
335     0C D040         1268                S       YD,YD,MR0           NO GO, RESTORE MS DIVIDEND      51612630
336     19 B029         1269    DH.0031     LSL     YD&Q,YD,CI          SHIFT DIVIDEND LEFT...CARRY FROM 51612640
                        1270    *                                       SUBTRACT BECOMES QUOTIENT BIT IN 51612650
337     05 7E77         1271                DFCF    MDR,MDR,NULL        DECREMENT COUNT                 51612660
338     67 73F6         1272                BF      L,DH.0030,REFRESH   LOOP UNTIL COUNT GOES NEGATIVE  51612670
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                        1274    *  FINISHED DIVIDE                                                                  51612690
                        1275    *                                                                                   51612700
345     15 B020         1276              LSR   YD,YD          ADJUST REMAINDER                                     51612710
346     04 7450         1277              L     FLR,MAR        TEST FLAGS,  REMAINDER GETS SAME                     51612720
347     66 F490         1278              BF    G,DH.0040      SIGN AS DIVIDEND. SKIP IF IT WAS                     51612730
348     0D 3020         1279              S     YD,NULL,YD     POSITIVE, ELSE 2'S COMP REMAINDER                    51612740
349     66 B4F2         1280    DH.0040   BT    G,DH.0042,YDP1 BRANCH IF DIVIDEND MINUS                             51612750
34A     67 7500         1281              BF    L,DH.0043      BRANCH, DIVIDEND +, DIVISOR +                        51612760
34B     04 7500         1282    DH.0041   LI    FLR,0          CLEAR FLAGS FOR TEST                                 51612770
34C     0D 202C         1283              S     YD,NULL,0,F    QUOTIENT SHOULD BE NEGATIVE                          51612780
34D     66 F196         1284              BF    G,EXIT.MD,REFRESH TWO'S COMP THEN TEST (P.29)   R01                51612790
                        1285    *                              OK IF IT'S NEGATIVE OR ZERO                          51612800
34F     7B B520         1286              B     DFAULT0        ERROR IF IT GOES POSITIVE                            51612810
34F     67 74B0         1287    DH.0042   BF    L,DH.0041      BRANCH, DIVIDEND - DIVISOR +                         51612820
                        1288    *                              ELSE BOTH MINUS                                      51612830
                        1289    *                              OR BOTH PLUS                                         51612840
350     0C 202C         1290    DH.0043   L     YD,0,F         QUOTIENT SHOULD BE POSITIVE                          51612850
351     67 7196         1291              BF    L,EXIT.MD,REFRESH OK IF IT IS POSITIVE (P.29)   R01                51612860
                        1292    *                              ERROR IF IT ISN'T                                    51612870
352     04 7843         1293    DFAULT0   I     MR0,MR0,YDM1   POINT BACK TO C1                                     51612880
353     A4 7B24         1294    DFAULT    LI    MAR,'24',MR                                                         51612890
354     04 7E30         1295              I     MDR,MEM                                                             51612900
355     0C 7072         1296              L     YD,MDR,YDP1    RESTORE R1                                           51612910
356     A4 7B26         1297              LI    MAR,'26',MR                                                         51612920
357     04 7E30         1298              I     MDR,MEM                                                             51612930
358     0C 7070         1299              L     YD,MDR         RESTORE R1+1                                         51612940
359     04 7B48         1300    DFAULT1   LI    MAR,'48'       PRESET MAR                                           51612950
35A     04 3E20         1301              L     MDR,YD         SAVE YD                                              51612960
35B     15 F010         1302              LSR   YD,PSW        PSW RIGHT ONE TO YD                                  51612970
35C     04 3820         1303              I     MR0,YD         DROP RESULT INTO MR0                                 51612980
35D     0C 7070         1304              I     YD,MDR         RESTORE YD                                           51612990
35E     00 7702         1305              LI    Q,2            RESTORE Q                                            51613000
35F     04 74C6         1306              L     FLR,MR0,CS+REFRESH SWAP DOWN INTO FLR           R01                51613010
360     63 9200         1307              BT    C,GENSWP       C FLAG=PSW03. IF SET, TAKE                           51613020
                        1308    *                              ARITHMETIC FAULT INTERRUPT (P.14)                    51613030
361     7B 81D0         1309              B     EXIT1          ELSE, CONTINUE IN SEQUENCE (P.2)                     51613040
```

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                        1311    * A U T O M A T I C   L O A D E R   O P T I O N                    51613060
                        1312    *                                                                  51613070
362     00 7701         1313    AUTOLOAD LI     Q,1                                                51613080
363     06 2A21         1314             N      MAR,NULL,Q,CLRYD    MAR & YD FIELD = 0             51613082
364     04 7804         1315    ALOLOOP1 RD     MR0                 INPUT EVEN BYTE                51613084
365     04 7E04         1316             RD     MDR                 INPUT ODD BYTE                 51613086
366     04 7EC0         1317             L      MDR,MR0,CS          COMBINE                        51613088
367     0C 7072         1318             L      YD,MDR,YDP1         SAVE HALFWORDS IN GEN REGS     51613090
368     04 6A54         1319             INC    MAR,MAR,Q           INCREMENT MAR & YD FIELD       51613092
369     04 7450         1320             L      FLR,MAR             TEST IF 4 HALFWORDS YET        51613094
36A     63 F640         1321             BF     C,ALOLOOP1          LOOP                           51613096
36B     06 2A21         1322             N      MAR,NULL,Q,CLRYD    POINT BACK TO R0               51613098
36C     04 3222         1323             L      PSW,YD,YDP1         LOAD NEW PSW FROM R0           51613100
36D     04 3C22         1324             L      LOC,YD,YDP1         LOAD NEW LOC FROM R1           51613110
36E     04 3A22         1325             L      MAR,YD,YDP1         LOAD START ADRS FROM R2        51613120
36F     04 D85A         1326             S      MPC,YD,MAR,CO       FINAL ADDRESS MINUS START      51613130
370     63 9E50         1327             BT     C,RESET             ERROR IF START GREATER (P.19)  51613140
                        1328    *                                  MR0 CONTAINS BYTE COUNT        51613150
                        1329    *                                                                  51613160
371     A4 7A50         1330    ALOLOOP  L      MAR,MAR,MR          FETCH HALFWORD                 51613170
372     04 7E30         1331             L      MDR,MEM                                            51613174
373     04 7E84         1332             RD     MDR,CS              INSERT NEW BYTE                51613176
374     84 6A50         1333             A      MAR,MAR,Q,MW        START WRITE, INCREMENT MAR     51613180
375     04 7670         1334             L      MEM,MDR             STORE HALFWORD                 51613190
376     05 684A         1335             S      MR0,MR0,Q,CO        DECREMENT COUNT                51613200
377     63 F710         1336             BF     C,ALOLOOP           LOOP                           51613210
378     04 79C0         1337    RESTART  LI     MR0,DEVICE                                         51613220
379     00 7702         1338             LI     Q,2                                                51613225
37A     04 7041         1339             ADR    MR0                 ADDRESS THE ASCII CONSOLE      51613230
37B     04 7903         1340             LI     MR0,3                                              51613240
37C     04 7042         1341             OC     MR0                 ISSUE RESET COMMAND            51613250
37D     78 9360         1342             B      TEST2               FINISHED (P.14)                51613260
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MICRO DIAGNOSTIC

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037F                          1344   SELFTEST EQU  *                    DIAGNOSTIC ROUTINE INTERED AFTER      51613280
                              1345   *                                  POWER-UP OR INITIALIZE.               51613290
                              1346   *                                                                        51613300
37F     04 7500               1347   TEST.000 LI   FLR,0                TEST IMMEDIATE DATA PATH AND FLR      51613310
37F     60 37E6               1348            BT    C+V+G+L,*-1,REFRESH HANG IF FLR NOT ZERO                  51613320
                              1349   *                                                                        51613330
                              1350   *                                                                        51613340
                              1351   *                                                                        51613350
380     04 7501               1352   TEST.001 LI   FLR,1                C,V,G=0, L=1                          51613360
381     67 7806               1353            BF    L,TEST.001,REFRESH  HANG ON ERROR                         51613370
382     60 B800               1354            BT    C+V+G,TEST.001                                            51613380
383     67 3850               1355            BT    L,TEST.002                                                51613390
384     78 B800               1356            B     TEST.001                                                  51613400
                              1357   *                                                                        51613410
385     04 7502               1358   TEST.002 LI   FLR,2                C,V,L=0, G=1                          51613420
386     66 F856               1359            BF    G,TEST.002,REFRESH                                        51613430
387     61 3850               1360            BT    C+V+L,TEST.002                                            51613440
                              1361   *                                                                        51613450
388     04 7504               1362   TEST.004 LI   FLR,4                C,G,L=0, V=1                          51613460
389     65 F886               1363            BF    V,TEST.004,REFRESH                                        51613470
38A     62 3880               1364            BT    C+G+L,TEST.004                                            51613480
                              1365   *                                                                        51613490
38B     04 7508               1366   TEST.008 LI   FLR,8                V,G,L=0, C=1                          51613500
38C     63 F8B6               1367            BF    C,TEST.008,REFRESH                                        51613510
38D     64 3880               1368            BT    V+C+L,TEST.008                                            51613520
                              1369   *                                                                        51613530
                              1370   *                                                                        51613540
38E     00 7702               1371   TEST.010 LI   Q,2                  EXERCISE Q REGISTER LOADING           51613550
38F     04 2420               1372            A     FLR,NULL,Q           AND UN-LOADING                        51613560
390     66 F8E6               1373            BF    G,TEST.010,REFRESH                                        51613570
391     61 38E0               1374            BT    C+V+L,TEST.010                                            51613580
                              1375   *                                                                        51613590
392     04 7905               1376   TEST.01A LI   MR0,5                TEST MR0 LOADING                      51613600
393     04 7440               1377            L     FLR,MR0              AND UN-LOADING                        51613610
394     61 B926               1378            BT    C+V,TEST.01A,REFRESH                                      51613620
395     65 F920               1379            BF    V,TEST.01A                                                51613630
                              1380   *                                                                        51613640
396     67 7920               1381            BF    L,TEST.01A                                                51613650
                              1382   *                                                                        51613660
397     04 790D               1383   TEST.011 LI   MR0,'0D'                                                  51613670
398     04 78C0               1384            L     MR0,MR0,CS           TEST CROSS-SHIFT,                     51613680
399     04 74C0               1385            L     FLR,MR0,CS           SWAP DOWN TO FLR                      51613690
39A     63 F976               1386            BF    C,TEST.011,REFRESH                                        51613700
39B     65 F970               1387            BF    V,TEST.011                                                51613710
39C     66 B970               1388            BT    G,TEST.011                                                51613720
39D     67 7970               1389            BF    L,TEST.011                                                51613730
                              1390   *                                                                        51613740
39E     00 77AA               1391   TEST.012 LI   Q,'AA'                                                    51613750
39F     04 2E20               1392            A     MDR,NULL,Q           PROPOGATE VALUE THROUGH STACK         51613760
3A0     04 7C70               1393            L     LOC,MDR                                                   51613770
3A1     04 7A60               1394            L     MAR,LOC                                                   51613780
3A2     04 7850               1395            L     MRC,MAR                                                   51613790
3A3     04 7450               1396            L     FLR,MAR                                                   51613800
3A4     63 F9E6               1397            BF    C,TEST.012,REFRESH                                        51613810
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MICRO DIAGNOSTIC

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3A5   65 39E0   1398            BT   V+L,TEST.012                                    51613920
3A6   66 F9E0   1399            BF   G,TEST.012                                    51613930
                1400   *                                                           51613940
3A7   00 770A   1401   TEST.013 LI   Q,'0A'                                        51613950
3A8   07 650A   1402            XT   FLR,'0A',Q          TEST XOR                 51613960
3A9   60 3A76   1403            BT   C+V+G+L,TEST.013,REFRESH                      51613970
                1404   *                                                           51613980
3AA   00 7705   1405   TEST.014 LT   Q,'05'              TEST EXCLISIVE NOR       51613990
3AB   07 F50A   1406            XNI  FLR,'0A',Q                                    51614000
3AC   60 3AA6   1407            BT   C+V+G+L,TEST.014,REFRESH                      51614010
                1408   *                                                           51614020
3AD   00 7702   1409   TEST.015 LI   Q,2                                          51614030
3AE   00 6702   1410            AT   Q,2,Q                TEST INCREMENT           51614040
3AF   04 2420   1411            L    FLR,G                                         51614050
3B0   62 3AD6   1412            BT   C+G+L,TEST.015,REFRESH                        51614060
3B1   65 FAD0   1413            BF   V,TEST.015                                    51614070

3B2   00 7702   1415            LI   Q,2                                          51614080
3B3   04 7B00   1416            LI   MAR,0                                        51614090
3B4   04 7E50   1417   TEST.020 L    MDR,MAR                                       51614100
3B5   84 6A50   1418            A    MAR,MAR,Q,MW                                  51614110
3B6   04 7670   1419            L    MEM,MDR             WRITE ADDRESS AS DATA    51614120
3B7   04 74D0   1420            L    FLR,MAR,CS          THROUGH FIRST 2048 BYTES 51614130
3B8   63 FB40   1421            BF   C,TEST.020                                    51614140
3B9   07 FE50   1422   TEST.030 XNI  MDR,MAR,NULL                                  51614150
3BA   84 6A50   1423            A    MAR,MAR,Q,MW        WRITE ADDRESS FALSE      51614160
3BB   04 7670   1424            L    MEM,MDR                                       51614170
3BC   04 74D0   1425            L    FLR,MAR,CS          THROUGH SECOND 2048 BYTES 51614180
3BD   63 BB96   1426            BT   C,TEST.030,REFRESH                           51614190
3BE   04 7E50   1427   TEST.040 L    MDR,MAR                                       51614200
3BF   84 6A50   1428            A    MAR,MAR,Q,MW        WRITE ADDRESS TRUE       51614210
3C0   04 7670   1429            L    MEM,MDR             THROUGH THIRD 2048 BYTES 51614220
3C1   04 74D0   1430            L    FLR,MAR,CS                                    51614230
3C2   63 FBE6   1431            BF   C,TEST.040,REFRESH                           51614240
3C3   07 FE50   1432   TEST.050 XI   MDR,MAR,NULL                                  51614250
3C4   84 6A50   1433            A    MAR,MAR,Q,MW        WRITE ADDRESS FALSE      51614260
3C5   04 7670   1434            L    MEM,MDR             THROUGH FOURTH 2048 BYTES 51614270
3C6   04 74D0   1435            L    FLR,MAR,CS                                    51614280
3C7   63 BC36   1436            BT   C,TEST.050,REFRESH                           51614290
                1437   *                                                           51614300
                1438   *                                                           51614310
3C8   04 7B00   1439            LI   MAR,0                                        51614320
3C9   7B HCB0   1440            B    TEST.060                                     51614330
3CA   05 6A50   1441   ERROR.60 S    MAR,MAR,Q           DECREMENT ADDRESS        51614340
3CB   A4 6A50   1442   TEST.060 A    MAR,MAR,Q,MR        READ MEMORY, INCREMENT MAR 51614350
3CC   04 7E30   1443            L    MDR,MEM             MEMORY OUTPUT TO MDR     51614360
3CD   01 6650   1444            S    Q,MAR,Q             ADDRESS TRUE             51614370
3CE   04 7500   1445            LT   FLR,0               CLEAR FLR                51614380
3CF   07 667C   1446            X    NULL,MDR,Q,F        COMPARE DATA TO ADDRESS TRUE 51614390
3D0   00 7702   1447            LI   Q,2                 RESTORE Q                51614400
3D1   66 3CA6   1448            BT   G+L,ERROR.60,REFRESH HANG ON ERROR            51614410
3D2   04 74D0   1449            L    FLR,MAR,CS                                    51614420
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MICRO DIAGNOSTIC

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3D3     63 FCB0     1450              RF    C,TEST,060          LOOP THROUGH 1ST 2048 BYTES     51614340
3D4     7B BD60     1451              R     TEST,070                                            51614350
3D5     05 6A50     1452  ERROR,70    S     MAR,MAR,Q           DECREMENT ADDRESS               51614360
3D6     A4 6A50     1453  TEST,070    A     MAR,MAR,Q,MR        READ MEMORY, INCREMENT MAR      51614370
3D7     04 7E30     1454              I     MDR,MEM                                             51614380
3D8     01 6650     1455              S     Q,MAR,Q             ADDRESS TRUE                    51614390
3D9     04 7500     1456              LI    FLR,0               CLEAR FLAGS                     51614400
3DA     07 E67C     1457              XR    NULL,MDR,Q,F        COMPARE FALSE DATA TO ADDRESS   51614410
3DB     00 7702     1458              LI    Q,2                                                 51614420
3DC     66 3D56     1459              BT    G+L,ERROR,70,REFRESH ERROR                          51614430
3DD     04 74D0     1460              L     FLR,MAR,CS                                          51614440
3DE     63 BD60     1461              RF    C,TEST,070          LOOP THROUGH 2ND 2048 BYTES     51614450
3DF     7B BE10     1462              R     TEST,080                                            51614460
3E0     05 6A50     1463  ERROR,80    S     MAR,MAR,Q           DECREMENT ADDRESS               51614470
3E1     A4 6A50     1464  TEST,080    A     MAR,MAR,Q,MR        READ MEMORY, INCREMENT MAR      51614480
3E2     04 7E30     1465              I     MDR,MEM                                             51614490
3E3     01 6650     1466              S     Q,MAR,Q                                             51614500
3E4     04 7500     1467              LI    FLR,0                                               51614510
3E5     07 667C     1468              X     NULL,MDR,Q,F        COMPARE DATA TO ADDRESS TRUE    51614520
3E6     00 7702     1469              LI    Q,2                                                 51614530
3E7     66 3E06     1470              BT    G+L,ERROR,80,REFRESH                                51614540
3E8     04 74D0     1471              L     FLR,MAR,CS                                          51614550
3E9     63 FE10     1472              RF    C,TEST,080          LOOP THROUGH 3RD 2048 BYTES     51614560
3EA     7B BEC0     1473              R     TEST,090                                            51614570
3EB     05 6A50     1474  ERROR,90    S     MAR,MAR,Q           DECREMENT ADDRESS               51614580
3EC     A4 6A50     1475  TEST,090    A     MAR,MAR,Q,MR        READ MEMORY, INCREMENT MAR      51614590
3ED     04 7E30     1476              I     MDR,MEM                                             51614600
3EE     01 6650     1477              S     Q,MAR,Q                                             51614610
3EF     04 7500     1478              LI    FLR,0                                               51614620
3F0     07 E67C     1479              XR    NULL,MDR,Q,F        COMPARE FALSE DATA TO ADDRESS   51614630
3F1     00 7702     1480              LI    Q,2                                                 51614640
3F2     66 3EB6     1481              BT    G+L,ERROR,90,REFRESH                                51614650
3F3     04 74D0     1482              L     FLR,MAR,CS                                          51614660
3F4     63 FEC0     1483              RF    C,TEST,090          LOOP THROUGH 4TH 2048 BYTES     51614670
                    1484  *                                                                     51614680
                    1485  *                                                                     51614690
3F5     04 7300     1486  OPTIONS     LI    PSW,0               PSW = '0000'                    51614700
                    1487  *                                                 CLEAR ALARM LAMP    51614710
3F6     04 AD04     1488              ST    LOC,NULL,4          LOC = 'FFFC'                    51614720
3F7     76 6780     1489              BT    ARST,RESTART        USER ADDRESSABLE ROM (P.32)     51614730
                    1490  *                                                                     51614740
                    1491  *                                                                     51614750
                    1492  *                                                                     51614760
3F8     75 6620     1493  NOARST      BT    ALO,AUTOLOAD        BRANCH IF ALO ENABLED (P.32)    51614770
3F9     7B 9E50     1494              R     RESET               GO TO CONSOLE ROUTINE (P.19)    51614780
3FA                 1495              END                                                       51614790
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MICRO DIAGNOSTIC

NO ERRORS

ABL	0264			
ABL1	0264			
ABL2	026A	1019		
ABL3	026E	1012		
ACH	008E			
ACHR	008E			
ACK	00CC			
ACKR	00CA			
ADDIT	025B	1017		
ADJUST	0169	685		
AH	008F			
AHI	008F			
AHM	0091			
AHR	008F			
AIS	008F			
AL	00F0			
AL1	02A6	534		
ALOLOOP	0371	1336		
ALOLOOP1	0364	1321		
ATBL	0059			
ATBL1	022E	224		
ATL	0251			
ATL1	0251			
ATL2	0256	988		
AUTOID	010F	571		
AUTOID1	0110	438	574	
AUTOLOAD	0362	1493		
BAL	007B			
BALR	007B			
BBS	0073			
BEGIN	02F1	713	726	A11
BFBS	006F			
BFC	0068			
BFCR	006C			
BFFS	006F			
BFS	0077			
BLKRR	028D	1114		
BLOCK1	02CA	1116		
BLOCK2	02CD	1144	1152	
BLOCK3	02CF	1137		
BRRX	005C	256		
BTBS	0064			
BTC	005B			
BTCR	0061			
BTFS	0064			
BX	007C	309	315	
BXH	0088			
BXHLI	007E			
BXLE	008B			
CH	0098			
CHI	0098			
CHR	0098			
CLB	0036			

CLH	0034													
CLHT	0034													
CLHR	0034													
COMAND1	0022	814												
COMAND2	0082	768												
CONSER	014A	1063												
CR1	0033	355												
CRLF	01CF	669	698											
DELAY1	0290	841												
DEVICE	00C0	812	837	1337										
DFAULT	0353	1264												
DFAULT0	0352	1256												
DFAULT1	0359	1250												
DH	00A0													
DH.0010	0332	1249												
DH.0020	033C	1258												
DH.0030	033F	1272												
DH.0031	0342	1267												
DH.0040	0349	1278												
DH.0041	034B	1287												
DH.0042	034F	1280												
DH.0043	0350	1281												
DH1	0326	374												
DHR	00A0													
DISPLAY	015B	834												
DMA.RD	0145	632	645											
DMA.WRT	0140	638												
DMAATN	013A	555												
EPSR	00C2													
ERROR.60	03CA	1448												
ERROR.70	03D5	1459												
ERROR.80	03E0	1470												
ERROR.90	03EB	1481												
EXAMINE	01BE													
EXAMINE1	01BF	748												
EXBR	001F													
EXIT.MD	0319	1220	1257	1284	1291									
EXIT1	001D	67	111	118	127	135	241	248	263	270	308	314	590	623
		1083	1309											
EXIT1A	003A	213	216	880	893									
EXIT2	0051	198	205											
EXIT2A	0055	210												
EXIT3	0200	855	862											
EXIT3.1	01FF	868	874											
EXIT3A	0207	883												
EXIT4	00B1	391												
EXIT4.5	00B2	414												
EXIT4A	00B7	406												
EXIT5	00BA	398												
EXIT6	021E	911												
EXIT6.7	021F	940												
EXIT6A	0226	925												
EXIT7	022C	917												
EXIT7B	0221													

MICRO DIAGNOSTIC

FINISH	02D8	1094	1141	1153	
GENSWP	0120	569	618	1307	
GETREG	02F3	1179			
IDLE	01CE	821			
IF.EQUAL	018E	730			
IF.PLUS	0194	737			
IF.XFER	019D	743			
ILEGAL1	011E	548			
ILLEGAL	00FF				
INITIAL	0106	552			
INPUT1	017C	718	733	756	779
INPUT1A	018C	739			
INPUT2	01A4	723			
INTERUPT	0100	23			
INTRPT1	0102	543			
IOATN	0109	556			
LP	001A				
LBR	001B				
LCS	000D				
LEADER	02B3	1102	1105		
LH	000A				
LHI	000A				
LHR	000A				
LIS	000A				
LM	000E				
LPSW	00BD				
LSTOVF	024E	950	968		
MH	009E				
MH.0010	0306	1197			
MH.0011	030A	1201			
MH.0020	030D	1213			
MH.0021	0310	1210			
MH.0030	0318	1215	1237		
MHI	0300	364			
MHR	009E				
MHU	009F				
MHU.0010	0320	1236			
MHU.0011	0323	1233			
MHUI	031C	369			
MHUR	009F				
MODIFY	01C4	787			
NEXTCHAR	015C	693			
NH	003C				
NHI	003C				
NHR	003C				
NOARST	03F8				
NORRX	0069	232			
NOT.HEX	01B8	761	767	772	
NUMERIC	01B2	764			
OC	00D6				
OCR	00D7				
OH	003E				
OHI	003E				
OHR	003E				

MICRO DIAGNOSTIC

OKASCII	016A	684	686			
OPTIONS	03F5					
OUTPUT1	01D5	822	826	828	830	832
OUTPUT2	0173	704				
PROMPT	0170	753	784	806		
PROMPT1	0172	665				
QUEVAL	012B					
RB	00EE					
RB.D2	02D3					
RBL	027D					
RBL1	027D					
RBL2	0282	1043				
RBR	00EF					
RD	00DB					
RDR	00E5					
REMOVE	0287	1033				
RESET	01E5	554	618	1327	1494	
RESTART	0378	1469				
RH	00DF					
RHB	02E0	488				
RHR	00E4					
RHR1	02E6	496				
RHR2	02E7					
RHRH	02FE	1161				
RI	0007					
RLL	01F7					
RRINPUT	00F1	466	501			
RRID	00CB					
RRL	01FA					
RTBL	005A					
RTBL0	023D	227				
RTL	0270					
RTL1	0270					
RTL2	0276	1035				
RTL3	027B	1026				
RWBRR	02BA	530				
RWBRY	02C2	525				
RX	0002					
RXBYTE	0015					
RXID	0014					
SCH	0095					
SCHR	0095					
SELFTEST	037E	563				
SH	0096					
SHI	0096					
SHORT	000C					
SHOW	0159	795				
SHR	0096					
SINT	00C6					
SIS	0096					
SLA	0217					
SLHA	00AA					
SLHL	004B					
SLL	01F1					

MICRO DIAGNOSTIC

SLLS	004B						
SLRA	00BC						
SLRA1	020C	417					
SLRE	0058						
SLRE1	01EA	220					
SLRH	0044						
SLRHA	00A1						
SLRS	004A						
SRA	021A						
SRHA	00AD						
SRHL	004E						
SRL	01F4						
SRLS	004E						
SS	00CE						
SSR	00D3						
START	0000						
STARTAL	02D4	1187					
STB	0029						
STBR	002E						
STH	0020						
STM	0024						
STREG	0154	666					
SVC	00C9						
SVC1	0292	442					
SVC1A	0299	1074					
SVC2	029B						
TERMIN	02D9	1101	1136				
TEST.000	037E						
TEST.001	0380	1353	1354	1356			
TEST.002	0385	1355	1359	1360			
TEST.004	0388	1363	1364				
TEST.006	038B	1367	1368				
TEST.010	038E	1373	1374				
TEST.011	0397	1386	1387	1388	1389		
TEST.012	039E	1397	1398	1399			
TEST.013	03A7	1403					
TEST.014	03AA	1407					
TEST.015	03AD	1412	1413				
TEST.01A	0392	1378	1379	1381			
TEST.020	03B4	1421					
TEST.030	03B9	1426					
TEST.040	03BE	1431					
TEST.050	03C3	1436					
TEST.060	03CB	1440	1450				
TEST.070	03D6	1451	1461				
TEST.080	03E1	1462	1472				
TEST.090	03EC	1473	1483				
TEST1	0129	425	431	557			
TEST2	0136	607	616	639	646	1186	1342
THI	0042						
WAIT	00F4	544	622				
WB	00EE						
WB.D2	02DB						
WBR	00EF						

APPENDIX 3 (Continued)

MICRO DIAGNOSTIC

WD	00E7	
WDR	00EC	
WH	00EA	
WHB	02ED	515
WHR	00EB	
XH	0040	
XHI	0040	
XHR	0040	

APPENDIX 4
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

DEVICE OPERATION

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

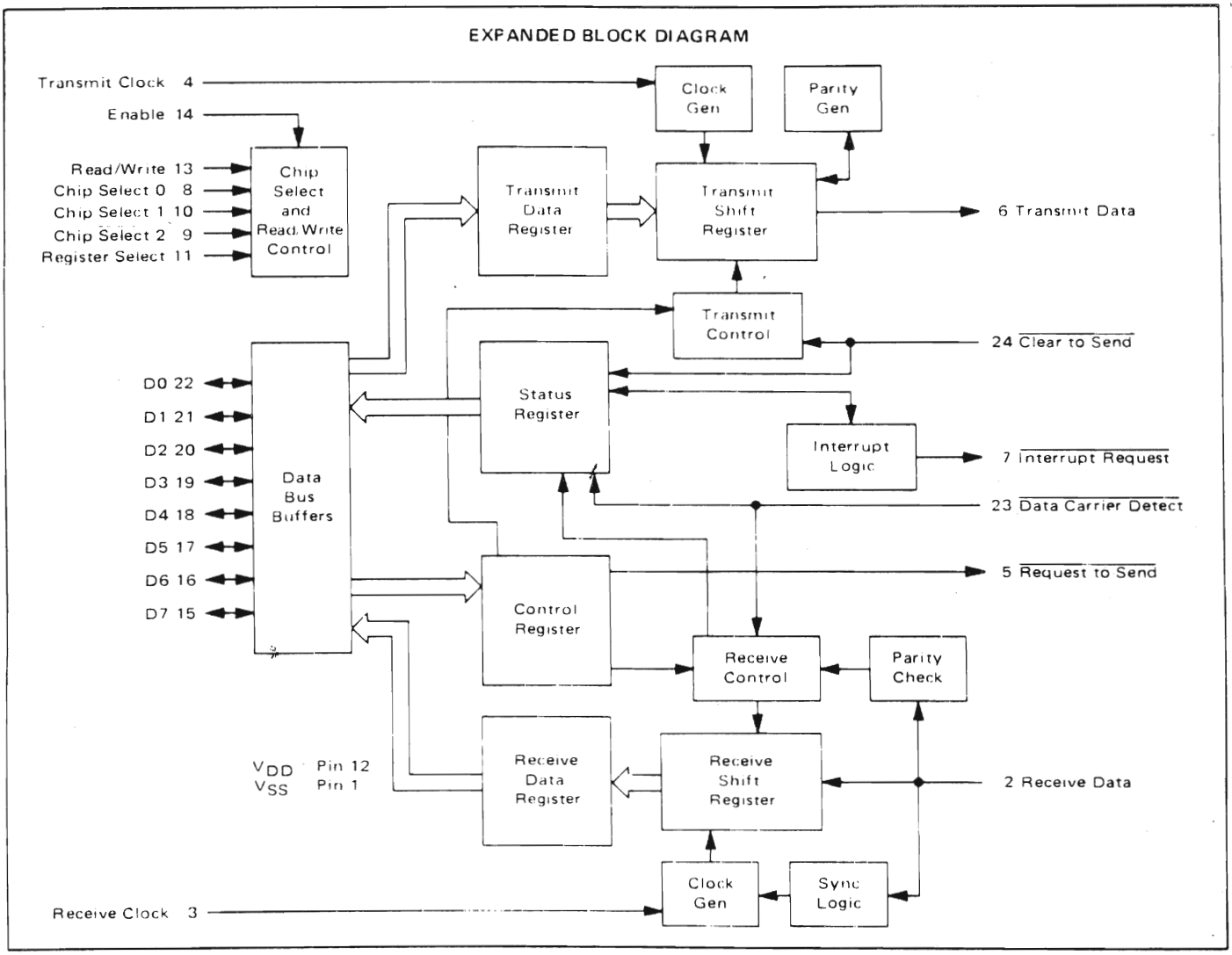

Figure A4-1. ACIA Expanded Block Diagram

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the ACIA functional configuration when the communications channel is required. Control bits CR5 and CR6 should also be programmed to define the state of RTS whenever master reset is utilized. The ACIA also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the ACIA. After master resetting the ACIA, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character

is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the Microprocessing Unit (MPU). When parity has been selected for an 8-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read again to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

ACIA INTERFACE SIGNALS FOR MPU

The ACIA interfaces to the MPU with an 8-bit bi-directional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals, in conjunction with the VMA output, permit the MPU to have complete control over the ACIA.

ACIA Bi-Directional Data (D0-D7) - The bi-directional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation.

ACIA Enable (E) - The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the 02 Clock.

Read/Write (R/W) - The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is low, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the ACIA.

Chip Select (CS0, CS1, $\overline{CS2}$) - These three high impedance TTL compatible input lines are used to address the ACIA. The ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the ACIA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS) - The Register Select line is a high impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data REgisters and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) - Interrupt Request is a TTL compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set. The IRQ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the ACIA. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5 • $\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data REgister except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the ACIA being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the ACIA. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the ACIA. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16 or 64 times the data rate may be selected.

Transmit Clock (Tx Clk) - The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (Rx Clk) - The Receive Clock input is used for synchronization of received data. (In the 1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data) - The Receive Data line is a high impedance TTL compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 kbps when external synchronization is utilized.

Transmit Data (Tx Data) - The Transmit Data output line transfers serial data to a modem or other peripheral. Data rates are in the range of 0 to 500 kbps when external synchronization is utilized.

PERIPHERAL/MODEM CONTROL

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) - This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) - The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready ($\overline{DTR}$).

Data Carrier Detect ($\overline{DCD}$) - This high impedance TTL compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set.

ACIA REGISTERS

The expanded block diagram for the ACIA indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in TABLE A4-1.

TABLE A4-1. DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • $\overline{R/W}$ Transmit Data Register (Write Only)	RS • R/W Receive Data Register (Read Only)	$\overline{RS}$ • $\overline{R/W}$ Control Register (Write Only)	$\overline{RS}$ • R/W Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	$\overline{\text{Data Carrier Detect}}$ ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	$\overline{\text{Clear to Send}}$ ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request (IRQ)

* Leading bit - LSB - Bit 0
** Data bit will be zero in 7 bit plus parity modes.
*** Data bit is "don't care" in 7 bit plus parity modes.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed and RS • $\overline{R/W}$ is selected. Writing data into the register causes the Transmit Data REgister Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to

whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

CONTROL REGISTER

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) - The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

TABLE A4-2. CLOCK DIVIDE RATIOS

CR1	CR0	FUNCTION
0	0	1
0	1	16
1	0	64
1	1	MASTER RESET

Word Select Bits (CR2, CR3, and CR4) - The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

TABLE A4-3. WORD SELECT ENCODING FORMAT

CR4	CR3	CR2	FUNCTION
0	0	0	7 BITS + EVEN PARITY + 2 STOP BITS
0	0	1	7 BITS + ODD PARITY + 2 STOP BITS
0	1	0	7 BITS + EVEN PARITY + 1 STOP BIT
0	1	1	7 BITS + ODD PARITY + 1 STOP BIT
1	0	0	8 BITS + 2 STOP BITS
1	0	1	8 BITS + 1 STOP BIT
1	1	0	8 BITS + EVEN PARITY + 1 STOP BIT
1	1	1	8 BITS + ODD PARITY + 1 STOP BIT

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) - Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

TABLE A4-4. TRANSMITTER CONTROL ENCODING FORMAT

CR6	CR5	FUNCTION
0	0	$\overline{RTS}$ = LOW, TRANSMITTING INTERRUPT DISABLED
0	1	$\overline{RTS}$ = LOW, TRANSMITTING INTERRUPT ENABLED
1	0	$\overline{RTS}$ = HIGH, TRANSMITTING INTERRUPT DISABLED
1	1	$\overline{RTS}$ = LOW, TRANSMITS A BREAK LEVEL ON THE TRANSMIT DATA OUTPUT. TRANSMITTING INTERRUPT DISABLED

Receive Interrupt Enable Bit (CR7) - The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full, Overrun, or a low to high transition on the Data Carrier Detect ($\overline{DCD}$) signal line.

STATUS REGISTER

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit 0 - Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. $\overline{\text{Data Carrier Detect}}$ being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 - The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

$\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), Bit 2 - The $\overline{\text{Data Carrier Detect}}$ bit will be high when the DCD input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the $\overline{\text{DCD}}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{\text{DCD}}$ input remains high after read status and read data or master reset has occurred, the interrupt is cleared, the $\overline{\text{DCD}}$ status bit remains high and will follow the $\overline{\text{DCD}}$ input.

$\overline{\text{Clear-to-Send}}$ ($\overline{\text{CTS}}$), Bit 3 - The $\overline{\text{Clear-to-Send}}$ bit indicates the state of the $\overline{\text{Clear-to-Send}}$ input from a modem. A low $\overline{\text{CTS}}$ indicates that there is a $\overline{\text{Clear-to-Send}}$ from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the $\overline{\text{Clear-to-Send}}$ status bit will be high. Master reset does not affect the $\overline{\text{Clear-to-Send}}$ Status bit.

Framing Error (FE), Bit 4 - Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 - Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The Overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status REgister until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 - The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request (IRQ), Bit 7 - The IRQ bit indicates the state of the $\overline{\text{IRQ}}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{\text{IRQ}}$ output is low the IRQ bit will be high to indicate the interrupt or service request status. IRQ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

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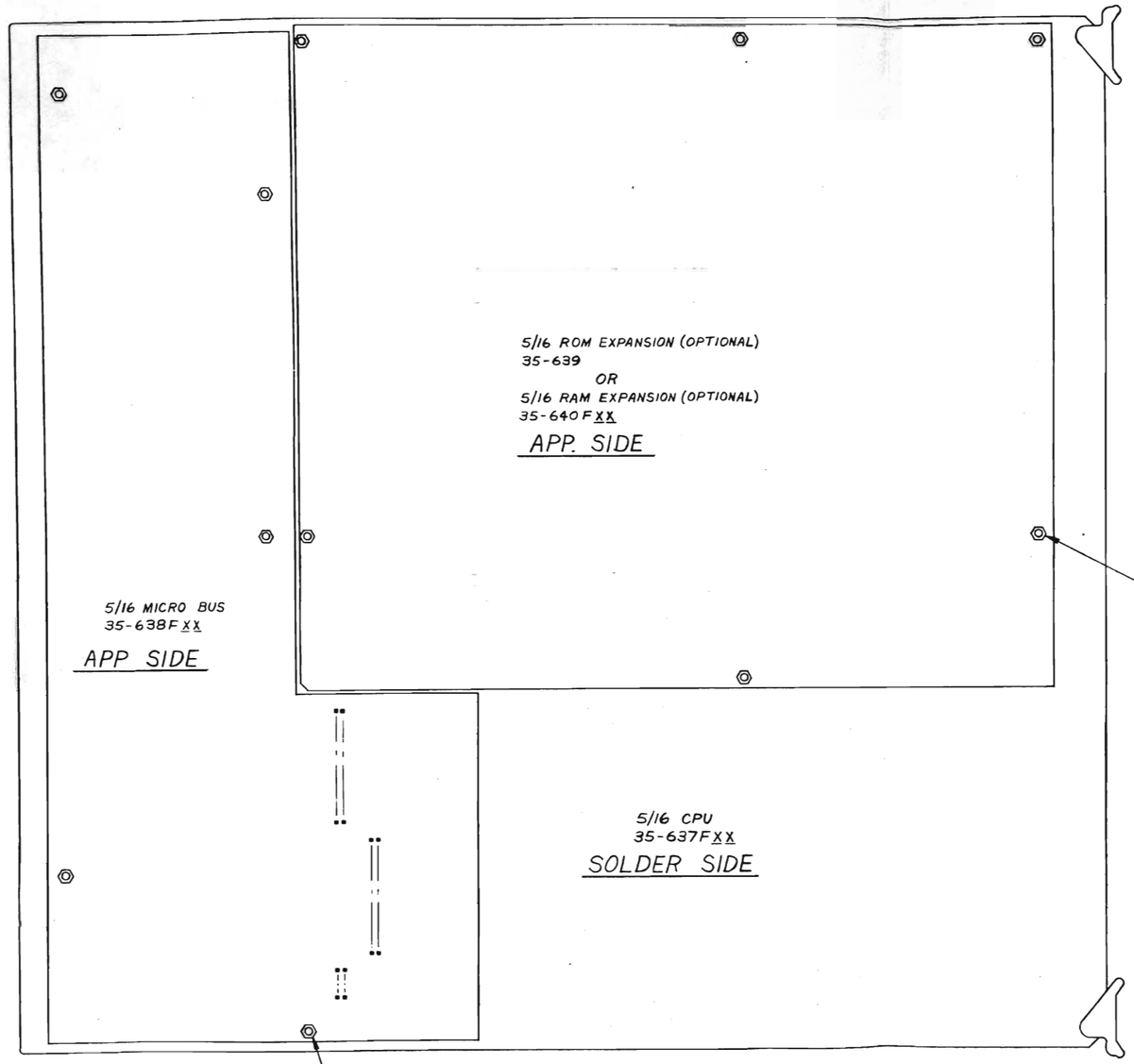

NOTES:
1. HARDWARE SHOWN IS FOR MAX. BOARD CONFIGURATION.

SCALE – 1:1	NAME	TITLE	DATE
TOLERANCE	K. LAFFERTY	DRAFT	2 MAY 77
.XXX ± .005	R. CERO	CHK	7-6-77
.XX ± .02	D. FRANKENBERGER	ENGR	7-6-77
.X ± .03	R. BARKER	Q.C.	7-6-77
ANGLES ± 1°	N. LENONDE	MGR	7-6-77
UNLESS OTHERWISE SPECIFIED			

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MODEL 5/16

TASK NO. 03867
DWG NO. 01-100 D12
SHEET 1 OF 1

BRUNING 44-231 24838

INTERDATA

REVISIONS
FOR PREVIOUS REVISION SEE REV R00 VOIDED COPY IN FILE
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NOTE: SWITCHES SHOWN ARE IN "OFF" POSITION.

PC2-A04 PC2-A05 PC2-A15 PC2-A12 PC2-A13 PC2-A11 PC2-A10 PC2-A14 PC2-A07 PC2-A08 PC2-A06 PC2-A09 GB

R13 PS PCI-12 4.7K
R15 PS PCI-14 4.7K
R14 PS PCI-13 4.7K
R17 PS PCI-16 4.7K
R18 PS PCI-17 4.7K
R16 PS PCI-15 4.7K
R20 PS PCI-19 4.7K
R19 PS PCI-18 4.7K
R22 PS PCI-21 4.7K MCH070
R21 PS PCI-20 4.7K MCH080
R23 PS PCI-22 4.7K MCH060
R24 PS PCI-23 4.7K MCH090

P/O 17-283 RAR150

MCH040 MCH050 MCH150 MCH120 MCH130 MCH110 MCH100 MCH140

AB 19-029 XOR 09 10 08
A9 19-029 XOR 09 10 08
AB 19-029 XOR 13 12 11
AB 19-029 XOR 04 05 06
AB 19-029 XOR 01 02 03
A3 19-029 XOR 04 05 06
A3 19-029 XOR 13 12 11
A9 19-029 XOR 01 02 03
A10 19-029 XOR 12 13 11
A10 19-029 XOR 09 10 08
A10 19-029 XOR 01 02 03
A10 19-029 XOR 04 05 06

A13 19-024 HA 11 09 10 08
A12 19-025 HA 13 10 09 12
A11 19-025 HA 01 05 04 02 06
A11 19-025 HA 13 12 09 10 08

SEE NOTE 3

P5 R27 1K 10 12 09 N.C. N.C. 11 08 N.C. 13 DS 1 A3 19-089 DC 0

W/W STAKES A B
OPTION SEE NOTE 2

A13 19-024 HA 03 04 05 06

R33 P5 2.2K C6 .1uf

P5 R32 2.2K R32 22 PCI-29 C5 .1uf R38 22 PCI-28

P/O 17-283 PC2 ADR MATCH0 SNGL0 NOTE: SWITCH #3 ARE IN OFF POSITION

P/O 17-283

A6 19-043 HG0 09 10 08
A5 19-002 G 11 09 10 08
A6 19-043 HG0 13 12 11
A7 19-029 XOR 05 04 06
A6 19-043 HG0 05 04 06

R29 1K P5 R36 22 PCI-30 PC2-ADR SYNC TP

P/O 17-283 PC2

DS 1 A3 19-089 DC 0 02 04 05 03 06 01
R28 1K P5
3CLR0C 102-3
FT1T0 103-3
BCLK0 104-3
TO CPU-HI BOARD 35-446

A12 19-025 HA 05 01 02 04 06

DS 1 A4 19-089 DC 0 02 04 05 03 06 FSADV1 N.C.
DS 1 A4 19-089 DC 0 12 10 09 11 08 13 N.C.
FADV0

P/O 17-283 PC2 ADV0 ADV1 GB PC2

PCI-26 R34 22 C3 .1uf R30 2.2K A5 19-002 G 01 13 02 12
PCI-27 R35 22 C4 .1uf R31 2.2K A5 19-002 G 03 04 05 06
ADVC0

P/O 17-283

C7 THRU C15 .1uf, 30V P5
DECOUPLING CAPACITORS

P/O 17-283 PC2 LED15 LED14 LED13 LED12 LED11 LED10 LED09 LED08 LED07 LED06 LED05 LED04

R1 PS 330 PCI-00
R12 PS 330 PCI-11
R2 PS 330 PCI-01
R3 PS 330 PCI-02
R4 PS 330 PCI-03
R7 PS 330 PCI-06
R10 PS 330 PCI-09
R11 PS 330 PCI-10
R8 PS 330 PCI-07
R9 PS 330 PCI-08
R5 PS 330 PCI-04
R6 PS 330 PCI-05

A1 19-044 HG0 13 12
A2 19-044 HG0 09 08
A1 19-044 HG0 11
A2 19-044 HG0 09 08
A1 19-044 HG0 01 02
A2 19-044 HG0 05 06
A2 19-044 HG0 13 12
A2 19-044 HG0 11 10
A2 19-044 HG0 03 04
A2 19-044 HG0 01 02
A1 19-044 HG0 03 04
A1 19-044 HG0 05 06

ALL DIODES 33-027

R26 PS 4.7K
R25 PS 4.7K

PC2- GA GB

P/O 17-283 PCI-24 PCI-25 C2 .2.2uf C1 .2.2uf
106-3 P5 101-3 105-3 100-3 112-3
TO CPU-HI BOARD 35-446

115-3 RAR150
114-3 RAR140
116-3 RAR130
117-3 RAR120
118-3 RAR110
113-3 RAR100
107-3 RAR090
110-3 RAR080
109-3 RAR070
108-3 RAR060
119-3 RAR050
120-3 RAR040
TO CPU-HI BOARD 35-446

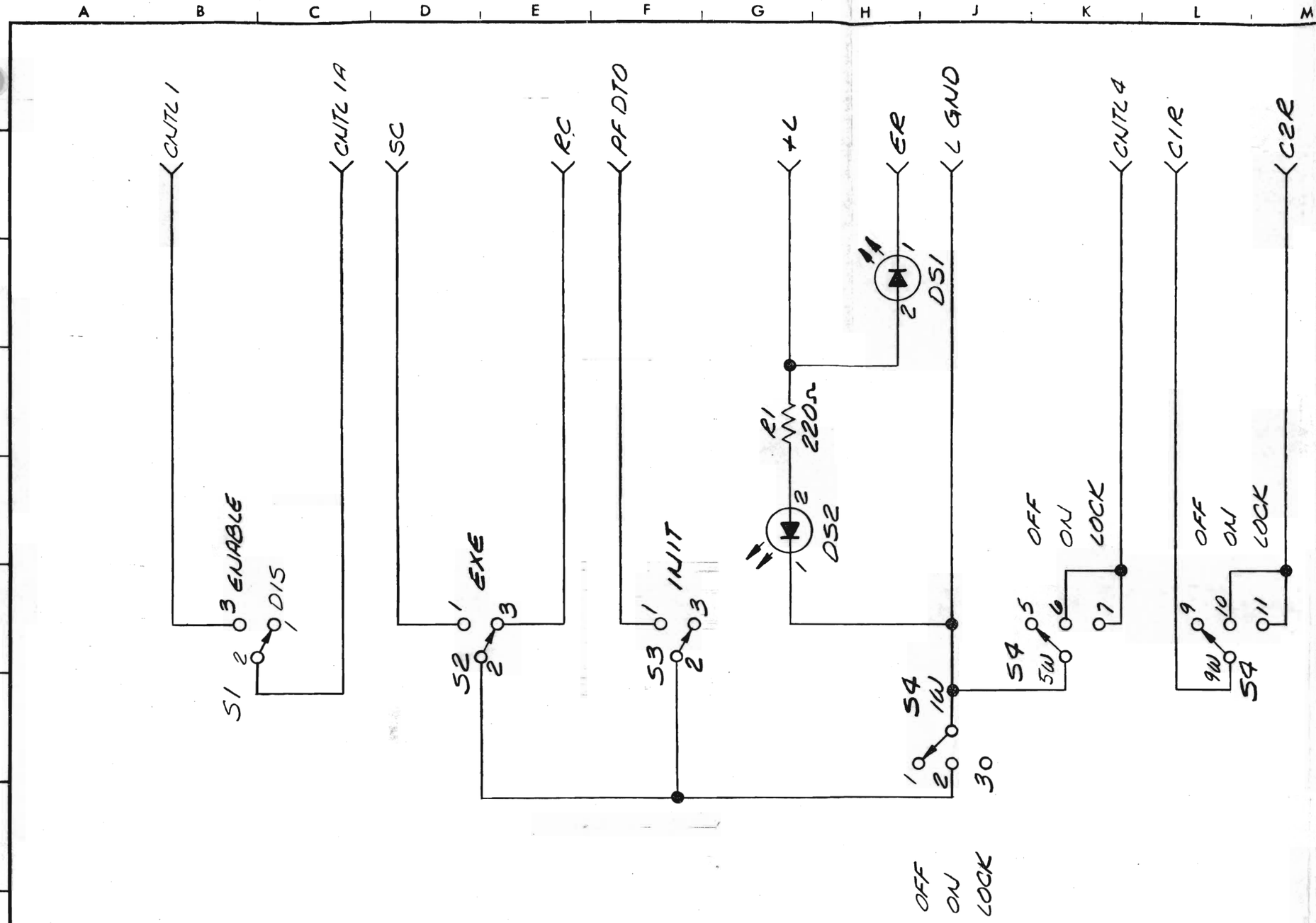
NOTES
1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS IS LOCATED ON TEST CONTROL BOARD 35-503.
2. REFER TO 02-276 TEST AID INFO SPEC.
3. THIS FLIP FLOP COULD BE USED AS A TEST AID.

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

NAME	TITLE	DATE
V. FERRI	DRAFT	7-17-73
E. CERO	CHK	7-18-73
G. JOYCE	ENGR	12-19-72
M. KOSS	Q.C.	12-19-72
D. FRANKENBERGER	DIR ENG	1-3-73

TITLE FUNCTIONAL SCHEMATIC
TEST AID
TASK NO 03047
DWG NO 02-276 R01 D08
SHEET OF 1 - 1

DRAWING 44-231 10042



INTERDATA
Subsidiary of PERKIN ELMER

REVISIONS

FOR PRODUCTION APPROVAL	INIT	DATE
	DEV GW	4/1/77
	PROD	

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

NOTES

SCALE—

TOLERANCE:
.XXX ± .005
.XX ± .02
.X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

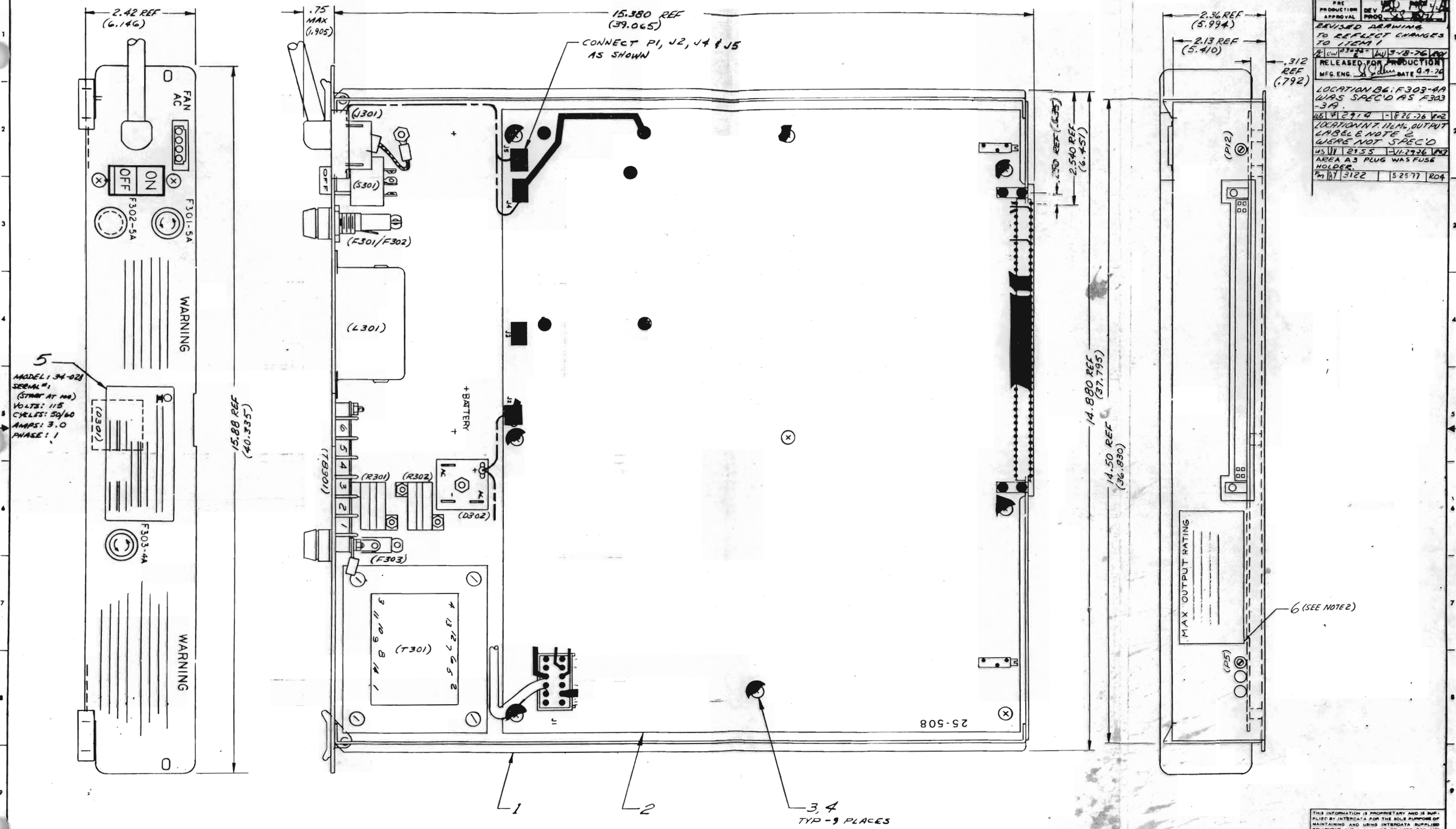
NAME	TITLE	DATE
A. SURAK	DRAFT	3-21-77
W. LIMPERT	CHK	4-1-77
G. WELLY	ENGR	
R. BARKER	Q.C.	
F. ABITANTE	MGR.	

TITLE
MOD 5/16
TURNKEY CONSOLE

TASK NO. 03867
DWG. NO. 17-436 B05
SHEET 1 — 1

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
PRE PRODUCTION APPROVAL	DEV PROG	WJD	4-9-76
REVISED DRAWING TO REFLECT CHANGES TO ITEM 1			
A WJD	03-03-76	WJD	5-18-76 ADV
RELEASED FOR PRODUCTION MFG. ENG.		DATE	6-9-76
LOCATION B6: F303-4A WAS SPEC'D AS F303-3A.			
WS WJD	2714	8-26-76	R02
LOCATION N7. 11.2MC, OUTPUT LABEL E NOTE 2 WERE NOT SPEC'D			
WS WJD	2955	11-29-76	R03
AREA A3 PLUG WAS FUSE HOLDER.			
WS WJD	3122	5-25-77	R04



NOTE: 1) DESIGNATIONS IN PARENTHESES ARE FOR REFERENCE ONLY; DIMENSIONS IN PARENTHESES INDICATE METRIC EQUIVALENT IN CM.

2) OUTPUT LABEL: MARK WITH THE FOLLOWING INFO:
+5 VOLTS @ 25 AMPS
±12 VOLTS @ 2 AMPS

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SCALE 1-1	NAME	TITLE	DATE
	J.F. FLEMING	DRAFT	1-26-76
	H. MATTER	CHK	4-9-76
	G. WELLY/LIOIO	ENGR	4-9-76
	R.A. BARKER	Q.C.	4-9-76
	P. ABITANTE	MGR	4-9-76

TITLE ASSEMBLY, SEMI-MEMORY POWER CONDITIONER

DWG NO. 34-028 R04 D03 — SHEET 1 OF 1

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

GRN. BLK WHT. F301 5A P/O S301 24-069 L301 (AC1) (AC2) D301 23-023 R301 1.0 25W R302 1.0 25W P1 J1 P/O 11-186 2B3 A 2A3 B 2A6 D

C136 475 200V C137 475 200V R156 100K R155 100K R154 100K R153 100K C110 15 200V C111 15 200V

30-048 T102 D101 23-042 CR13 R189 10,5W D102 23-042 100V .1 40mH L102 30-023 C108 16500 6V L101 30-050 3mH C107 330 6.3V R102 5.0 10W R103 5.0 10W P5 +L 100-2-113-2 200-2-212-2 P5 GND L GND 114-2-127-2 213-2-227-2

R104 21-075 .006 WHT WHT YEL YEL C B A

T101 30-049 C109 540 PF 1000V R196 .12,5W R197 .12,5W R109 450 N.I. 1 M H MAX 5W WW 20-030 Q103 20-030 Q105

P15 BIAS P15 AUX 2K7 R145 2K Q115 20-023 R144 100 1% Q113 20-023 R143 3.3K Q112 20-023 R134 33 Q117 20-023 Q118 20-027 Q114 20-023 Q116 20-027 R146 22 R137 33 R138 4.7K R139 4.7K R148 4.7K R147 4.7K D125 23-036 D126 23-036 D127 23-036 D128 23-036 D129 23-036 D130 23-036 D107 23-025 D105 23-025 R142 6.8K

R103 19-191 R102 19-192 CLK2 CLR2 CLK1 CLR1 R150 17.2K 1% C117 330PF 2% R195 10K

P15 BIAS R194 10K C135 .0039 C134 .0039 R193 5.1K Q132 20-013 D119 23-034 R135 10K R133 10K R136 1% 1K,1W Q119 20-038 RM1 13.3 1% R199 1 1W

P12 GND 2R4 R199 6.8K Q131 20-013 D131,23-034 C142 100 25V R200 100 ½W D133 23-022 D122 23-034 R165 1.5K Q129 20-013 Q128 20-013 R174 47K R171 100K C123 2.2 20V R191 6.8K C128 150 PF R190 5.1K C129 0.1 30V

R104 19-094 NC 07 Vcc V2 10 NC 01 VOUT NC 08 NC 14 COMP 13 11 12 02 03 04 CUR LIM SENSE INV IN 06 VREF NON INV IN 05 07

R198 68 C141 0.1 30V R105 10K R192 1K 1% C139 0.1,30V R152 20K 1% R151 4.99K 1% D123 G 23-028 R201 150 R202 22 D124 22-034 C144 15μf

P15 BIAS R159 10K R160 820K R161 47 D108 23-034 R162 10K R163 10K Q121 20-013 R158 3K R157 10K R106 2K

R105 19-085 08 Vcc 04 RESET OUTPUT 03 02 TRIGGER 07 DISCHARGE 06 THRESHOLD CONT.VOL GND 01 05 C121 0.1 30V C120 2.2 20V

20-013 Q120 PFOTO (POWER FAIL) 135-2 PWR FAIL GND 235-2

P/O 30-051 T301 P1 5 6 7 10 11 12 1 D113 23-034 D114 23-034 SEE NOTE 3 D115 23-034 D116 23-034 D117 23-034 C124 100 50V C126 4.7 50V C127 4.7 50V R185 681 1% C125 0.47 150V R181 150K 1% R186 1K 1% R182 357K 1% R178 15K R173 100K R179 10K R177 23.7K 1% R176 2K 1% R175 68K D112 23-043F02 6.2V, 1% R172 20K 1% Q125 20-013 Q126 20-038 Q123 20-023 Q122 20-013 R169 68K R170 68K R168 10K R166 10K R167 6.8K P15 AUX 2K7 R164 3K

P/O 11-186

08 09 13 12 R103 19-191 10 NC 11 NC

CHARGER ON/OFF 3E7

COMPONENT NUMBERING	
101-299	HI VOLTAGE BOARD
301-399	CHASSIS
401-499	BATTERY OPTION BD

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-614R01	BATTERY OPTION
35-615R08	HI VOLTAGE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

REVISIONS

PRE PRODUCTION APPROVAL	DEV	MKT	DATE	

REVISED SHEETS 1, 2, & 3 FOR PREVIOUS REVISION SEE R00 MICROFILM IN FILE, AREA K9, 35-614 WAS R00 & 35-615 WAS R02 — R01 | 030258 | 3-19-76 | R01

REVISED SHEETS 1 & 2 AREA K9, 35-615 WAS R04 AREAS F1, B7 DIODES SHOWN DOTTED WERE NOT SPEC'D. ADDED NOTE 3. AREA D5, C122 WAS 4.7/50V; AREA B5, C140 WAS 0.1/30V & WAS CONNECTED TO R140; AREA A6, ADDED R199; AREA F4, ADDED R200 & CR42; AREA J6, "CHARGER ON/OFF WAS WAS CONNECTED TO D109 CATH — R02 | 03025 M | 3-30-76 | R02

RELEASED FOR PRODUCTION ENG. DATE 4/3/76

REVISED SHTS 1 & 2; ADDED THE FOLLOWING COMPONENTS: D122-D131, D133, C143 & C144, R102, R189, R201 & R202. C142 WAS SPEC'D AS 15μf. AREA F1: DELETED DIODES, AREA B5: DELETED C116 0.1μf, R140 33Ω. REVISED CIRCUITRY AREA E2, G6, AREA L9: 35-615 R08 WAS R06. — WS 7 | 2910 | 8-26-76 | R03

AREA A1 & 1B & 2A ADDED COLORS TO WIRES CHANGED 2B3 WAS 2A3 & 2A3 WAS 2B6, CHANGED A WAS B & B WAS C. REVERSED POSITIONS OF F301 5A AND P/O S301. DELETED (FUSE) F302 5A. AREA D1, ADDED AC1 & AC2. ALSO CHANGED SHT 2. — PM | 3122 | 5 25 77 | R04

SHEET	REV LEVEL	4	4	1
INDEX	SHT. NO.	1	2	3

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
:ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
:ALL CAPACITORS ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE PART OF 35-615.
3. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

SCALE — NONE

	NAME	TITLE	DATE
DRAFT	J.R. BIELSKIE	DRAFT	11-10-75
CHK	H. MATTER	CHK	4-9-76
ENGR	P. LIOIO	ENGR	4-9-76
SYS TEST	J. JAMES	SYS TEST	4-9-76
MGR	S. MESSINA	MGR	4-9-76

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TITLE FUNCTIONAL SCHEMATIC POWER CONDITIONER

TASK NO 03025 | SHEET OF 1 — 3.

DWG NO 34-028 R04 D08

BRUNING 44-231 24530

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
FOR PREVIOUS REVISION SEE ROD MICROFILM IN FILE				
KB	03025-B		3-19-76	R01
AREA G2, R118 WAS NOT SPECIFIED AS 1%; AREAS E3, D5, D8 DIODES SHOWN DOTTED WERE NOT SPEC'D. ADDED NOTE 1.				
KB	03025-10		3-29-76	R02

AREA D2, F303 WAS 3A, AREA E3, DELETED UNEQUIPPED DIODE, ANODE TO J1-8, AND CATHODE TO J1-6; AREA G7, C145, C146, D132 & RELATED CIRCUITRY WAS NOT SPEC'D.

WS	7	2910	5-26-76	R03

AREA A4 TB301-2 WENT TO 1A2-C. AREA A4 ADDED TERM NO'S 3, 4, 5, & 6.

PM	GV	3122	5-25-77	R04

T301 P/O 30-051 · F303 4A · D302 23-023 · D118 23-025 · BATTERY STAND-BY 3L1 · D104 23-034 · R111 3.3K · R110 · Q104(HS) 20-006 · R108 0.1, 5W WW · (HS) 20-006 · R112 390 · R120 0.2 5W · R123 47K · R122 15K · R121 WW 1K 1% · R118 10K 1% · R119 10 · Q101 · Q106 20-023 · Q111 20-023 · Q110 20-023 · Q107 20-023 · P12/2A → 128-2-130-2, 228-2-230-2 · R107 6.99K 1% · C102 150 16V · C104 150 16V · C106 150 16V · C138 4800 50V · D121 23-034 · Q109 20-013 · R101 10K · Q108 20-038 · D103 23-041FD2 6.2V 5% · R116 20K 1% · C112 2.2 20V · R117 200K · R114 23.7K 1% · R113 4.99K 1% · C101 150 16V · C103 150 16V · C105 150 16V · P12 GND IC6 · P12 GND 1E4 · P12 GND · P5 GND J8 · R115 10K 1% · R188 68 2W · R187 68 2W · SEE NOTE 1 · C3 141-2 · C1 240-2 · 5 VAC/50 MA · 115V 230V · 7B301 · J301 · P301 · B301 · B302 · 1A2 · 1A1 · P1 J1 · J2

CHARGER INPUT 3A1 · Q102 20-006 · (HS) · R128 2 1W WW · P15 BIAS · R127 390 · D106 23-046 · C113 1000 75V · R129 10K 1% · R131 4.99K 1% · R130 10K 1% · R132 10K · A101 19-094 · NC 09 · VCC V4 10 · VOUT 01 · NC 08 · NC 14 · COMP 13 · CUR LIM. SENSE 12 · CUR 02 · INV IN 04 · VREF 06 · CHARGER REF 3A4 · NON INV IN 05 · V- 07 · C114 0.1 30V · SEE NOTE 1 · D132 23-025 · C115 100 50V · P15 AUX → 1F2, 1G6 · C145 100 25V · C146 100 25V · P5 GND · P5 · CHARGER INPUT GND 3A5

CHASSIS ASSY P/O 11-186

HI VOLTAGE BOARD P/O 35-615

NOTES:
1. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

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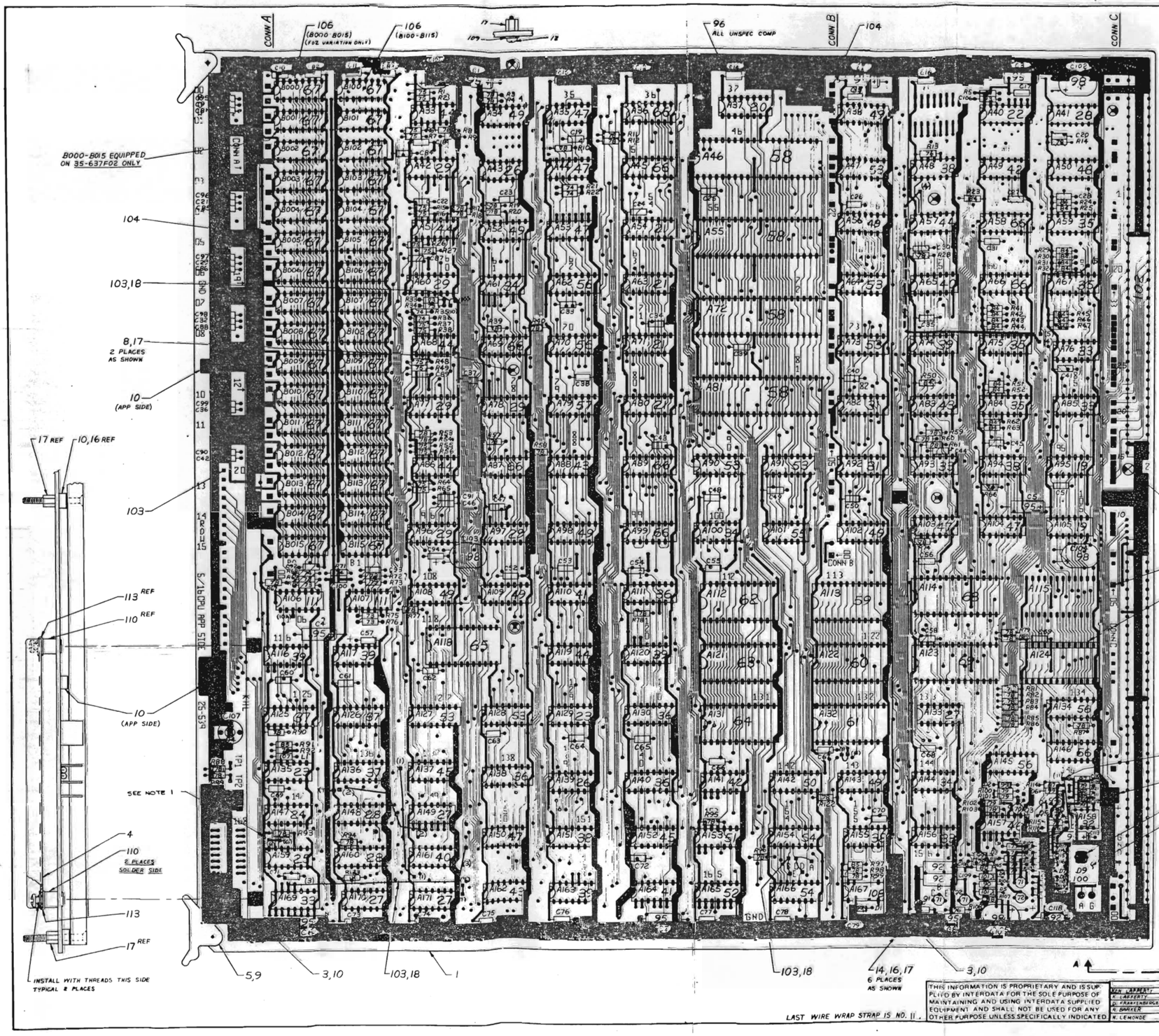
SCALE – ~

	NAME	TITLE	DATE
	J.R. BIELSKIE	DRAFT	11-10-75
		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

TASK NO. 03025 · DWG NO. 34-028 RD 008 · SHEET OF 2 – 3



VARIATION TABLE	
35-637F02	AS SHOWN (16KB)
35-637F01	WITHOUT B000 THRU B015 (8KB)

COMPONENT	REF. DESIGNATION
RESISTOR	R1 - R123
TRANSISTOR	Q1 - Q7
CHOKE	L1
DIODE	D1 - D9
CAPACITOR	C1 - C118
INTEGRATED CKT.	A1-A36, A40-A167, A169-A171

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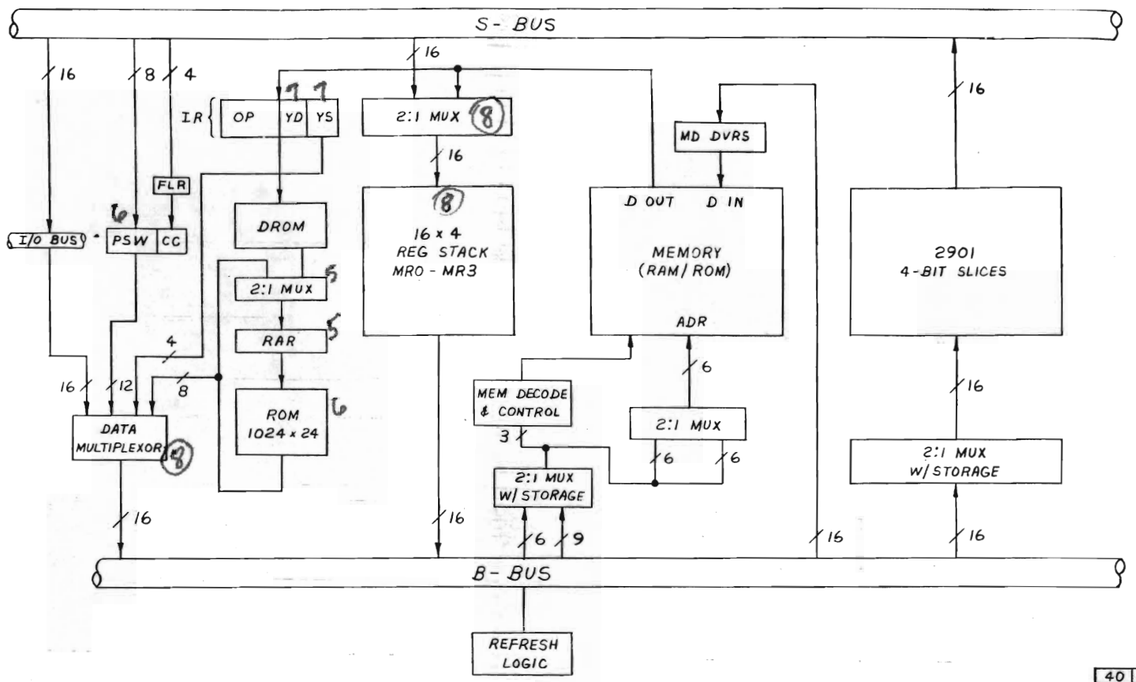
DES. APPROV.	DRAFT	12 JUN 77
R. LAFFERTY	CHK	12 JUN 77
D. FRANKENBERGER	ENG	13 JUN 77
G. BARKER	Q.C.	13 JUN 77
M. LEMONDE	MGR	13 JUN 77

ASSEMBLY 5/16 CPU
35-637 REV. E03
1 - 1.
C-01

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757



5/16 BLOCK DIAGRAM

PRINTED CIRCUIT BOARD ASSEMBLIES AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-637 F01 R03
35-637 F02 R04

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX	REV.	1											1	
	SHT. NO.	1	2	3	4	5	6	7	8	9	10	11	12	13

DECOUPLING CAPACITORS

P5 — C1 - C8, 15MF 25V TANTULUM
N5 — C95 - C100, .1MF 30V
P5 — C9 - C80, .1MF 30V
P12 — C101 - C105, 150MF 16V TANTULUM
P12 — C81 - C94, .1MF 30V

	CONN 2	CONN A	CONN B	CONN C	
40				GND	40
				SYNO	
				P5	
				ATNOA	
				SCLRO	
35				ADO	35
				ATNO	
			P12	GND	
		MS001	P12	DO70	
		N5	GND	DO60	
30		MS011	GND	DO50	30
		P12	P5	DO40	
		MS021	FRFRSHO	DO30	
		GND	P5	DO20	
		MS031	B031	DO10	
25		P5	B021	DO00	25
		MS041	B011	DRO	
		N5	B001	SRO	
		MS051	FRASI	DMATNO	
		P12	B041	DAO	
20	N.C.	MS061	WTI	CMDO	20
	N.C.	GND		ADRSO	
	RAR110	MS071	B051	TACKO	
	RAR120	P5	B071	ACKO	
	RAR130	MS081	B061	GND	
15	RAR150	N5	RFRSHI	DI20	15
	RAR140	MS091	GND	DI40	
	RAR100	P12	B081	DACKO	
	GND	MS101	B091	DI50	
	N.C.	GND	B101	DI30	
10	RARO80	MS111	B111	DI10	10
	RAR070	P5	RFCLKO	DO90	
	RAR060A	MS121	B131	DI00	
	RAR090	N5	B121	DO80	
	P5	MS131	P5	GND	
05	GND	P12	GDDCLKO	P5	05
	CLKO	MS141	B151	BCLKI	
	FTITO	GND	B141	FINRI	
	N.C.	MS151	FCADI	GND	
	P5	P5	P12 (N.C.)	P5	
00	GND	FCASI	GND	P12	00

CONN 1

	1	2
41	P5	GND
	GND	GND
	P12	P12
35		
30		
	SCLRO	HWO
25	GND	GND
	SYNO	ATNO
		ACKO
	CLO7O	DAO
20	DRO	CMDO
	SRO	ADRSO
	DI40	DI50
	DI20	DI30
	DI00	DI10
15	DO80	DO90
	DO60	DO70
	DO40	DO50
	DO20	DO30
	DOOO	DO10
10		
	FAULTO → EB	
	SCATNO → RC	RCATNO → SC
05	DNMI	
	CIS → C1A	
	C3 → GND	
	ARFCLKI	PFDTO
	GND	GND
00	P5	GND

CONN O

	1	2
41	P5	GND
	GND	GND
	P12	
35		
30		
25	GND	GND
20		
15		
10		
05		
	P12	
	GND	GND
00	P5	GND
	1	2

REVISIONS

PRE PRODUCTION APPROVAL	DEV PROD	INIT	DATE 7/DEC/77

REVISED SHT. 12. AREA AB: 35-637F01 WAS R01; F02 WAS R02.

P/N	ECR		
35-637	3274	K	16-9-77 R01

RELEASED FOR PRODUCTION
ENG. _____ DATE 7/DEC/77

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SCALE —	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	K. LAFFERTY	DRAFT	7 DEC 76
	K. LAFFERT.	CHK	13 JUN 77
	D. FRANKENBERGER	ENGR	13 JUN 77
	B. MULLER	SYS TEST	13 JUN 77
	R. BARKER	Q.C.	13 JUN 77

TITLE SCHEMATIC 5/16 CPU

PART NO.	SHEET OF
03867	1-13
DWG NO. 35-637R01 D08	

DRAWING 46-231 2/68

REFRESH COUNTERS

A62 19-180 4-BIT COUNTER

A70 19-180 4-BIT COUNTER OUTPUTS

A34 19-167 LDF

A52 19-167 LDF

A69 19-187 2:1 MUX W/STORAGE

A87 19-187

MEMORY ADDRESS REGISTERS

A78 19-065 2:1 MUX OUTPUTS 2Y STTL 4Y

A97 19-065 2:1 MUX STTL

ADDRESS MULTIPLEXERS

MEMORY ADDRESS DRIVERS

A53 19-165 LDF

A35 19-165 LDF

A44 19-165 LDF

FWT

FPWRUP

FRFRSH

FRFCY

A61 19-115 HA

A129 19-055 50

A137 19-161 LA

A83 19-159 LOR

A74 19-154 LG

A157 19-163 LH

A106 19-124 5.8

A107 19-124 5.8

NOT EQUIPPED

30μs OSC

A158 19-085 TIMING CKT

N5 SUPPLY

OVER VOLT PROT

1. STRAPS INSTALLED AT BOARD TEST.

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SCALE—	NAME	TITLE	DATE
TOLERANCE		DRAFT	12APR76
		CHK	
		ENGR	

TITLE SCHEMATIC 5/16 CPU

TASK NO. 03867

DWG NO. 35-637 D08

SHEET OF 2-13

DRUMING 44-231 2A538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

MD DRIVERS

LMEM1 1005 885 → 23-B, 8001 → R4 1K P5 → A33 19-160 LA (10 09 / 08) → R1 100 → MD001 → B100 (02)
885 → 24-B, 8011 → R3 1K P5 → A33 19-160 LA (13 12 / 11) → R2 100 → MD011 → B101 (02)
885 → 25-B, 8021 → R9 1K P5 → A33 19-160 LA (02 01 / 03) → R6 100 → MD021 → B102 (02)
885 → 26-B, 8031 → R8 1K P5 → A33 19-160 LA (05 04 / 06) → R7 100 → MD031 → B103 (02)
805 → 21-B, 8041 → R18 1K P5 → A51 19-160 LA (10 09 / 08) → R15 100 → MD041 → B104 (02)
805 → 18-B, 8051 → R20 1K P5 → A51 19-160 LA (13 12 / 11) → R16 100 → MD051 → B105 (02)
805 → 16-B, 8061 → R19 1K P5 → A51 19-160 LA (02 01 / 03) → R26 100 → MD061 → B106 (02)
805 → 17-B, 8071 → R17 1K P5 → A51 19-160 LA (04 05 / 06) → R27 100 → MD071 → B107 (02)
887 → 13-B, 8081 → R40 1K P5 → A68 19-160 LA (10 09 / 08) → R37 100 → MD081 → B108 (02)
886 → 12-B, 8091 → R11 1K P5 → A68 19-160 LA (13 12 / 11) → R38 100 → MD091 → B109 (02)
886 → 11-B, 8101 → R39 1K P5 → A68 19-160 LA (02 01 / 03) → R48 100 → MD101 → B110 (02)
886 → 10-B, 8111 → R12 1K P5 → A68 19-160 LA (05 04 / 06) → R49 100 → MD111 → B111 (02)
805 → 07-B, 8121 → R58 1K P5 → A86 19-160 LA (10 09 / 08) → R55 100 → MD121 → B112 (02)
805 → 08-B, 8131 → R53 1K P5 → A86 19-160 LA (13 12 / 11) → R56 100 → MD131 → B113 (02)
805 → 03-B, 8141 → R57 1K P5 → A86 19-160 LA (02 01 / 03) → R64 100 → MD141 → B114 (02)
805 → 04-B, 8151 → R54 1K P5 → A86 19-160 LA (05 04 / 06) → R65 100 → MD151 → B115 (02)

2K7 CS00
2D4 WT00
2H6 RAS00
2J7 CAS00
2L6 AD50
2M6 AD40
2M6 AD30
2N6 AD20
2N6 AD10
2N6 AD00

B100–B115: DIN, CS, WRITE, RAS, CAS, A5, A4, A3, A2, A1, A0 → DOUT; 19-197

2K7 CS10
2D4 WT10
2H6 RAS10
2J7 CAS10

B000–B015: 19-197

B000 → 32-A → MS001 → 5A1, 8B1
B001 → 30-A → MS011 → 5A1, 8B1
B002 → 28-A → MS021 → 5B1, 8C1
B003 → 26-A → MS031 → 5B1, 8C1
B004 → 24-A → MS041 → 5C1, 8D1
B005 → 22-A → MS051 → 5C1, 8D1
B006 → 20-A → MS061 → 5D1, 8E1
B007 → 18-A → MS071 → 5D1, 8E1
B008 → 16-A → MS081 → 7N1, 8F1
B009 → 14-A → MS091 → 7N1, 8F1
B010 → 12-A → MS101 → 7N1, 8G1
B011 → 10-A → MS111 → 7N1, 8G1
B012 → 08-A → MS121 → 7K1, 8H1
B013 → 06-A → MS131 → 7K1, 8H1
B014 → 04-A → MS141 → 7K1, 8H1
B015 → 02-A → MS151 → 7J1, 8J1

19-197
PIN 1 - N5
PIN 8 - P12
PIN 9 - P5
PIN 16 - GND

RAM

35-637F01 : LESS B000 THRU B015 (8KB)
35-637F02 : AS SHOWN (16KB)

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SCALE –
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

	NAME	DATE
DRAFT		12 APR 76
CHK		
ENGR		

TITLE SCHEMATIC 5/16 CPU
TASK NO. 03867
DWG. NO. 35-637 D08
SHEET 3 OF 13

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

10G4 DAMODO
RD091
A156 19-101 B
6M5
6M3 RD031
A120 19-154 LG
RD030
6M4 RD041
6M4 RD051
6N7 RD141
A110 19-156 LG
B0
A0
7J9 YS31
7K9 YS21
7K9 YS11
7K9 YS01
A90 19-179 QUAD 2:1 MUX (A0) TRISTATE
7N9 YD31
7N9 YD21
7N9 YD11
7N9 YD01
A91 19-174 QUAD 2 TO1 MUX (A0) TRISTATE
P5
R60 1K
7E1 ZERO1
7F1 OVL1
7G1 CARRY1
6M5 RD111
6M5 RD101
6M5 RD091
6M5 RD081
6M4 RD071
6M4 RD061
6M4 RD051
6M4 RD041
6M3 RD031
7A1,7C5 SLOSRI1
7A1,7B5 QLOQRI1
7B1,7B5 SLISRO1
7B1,7B5 QLIQRO1
12R7 DESCLK0
S001 6A7, 7E1, 8B1, 9B6
S011 6A7, 8C1, 9B6
S021 6A7, 8C1, 9C6
S031 6A7, 8C1, 9D6
S041 6A6, 8D1, 9E6
S051 6A5, 8E1, 9F6
S061 6A5, 8E1, 9F6
S071 6A5, 8E1, 9G6
S081 8F1, 9B6, 9H5
S091 8F1, 9C6, 9J5
S101 8G1, 9C6, 9K5
S111 8G1, 9D6, 9K5
S121 7F1, 8H1, 9E6, 9M5
S131 7F1, 8H1, 9F6, 9M5
S141 7E1, 8J1, 9G6, 9N5
S151 7E1, 8J1, 9G6, 9N5, 10N1
A46 19-184 4-BIT SLICE
A55 19-184 4-BIT SLICE
A72 19-184 4-BIT SLICE
A81 19-184 4-BIT SLICE
A37 19-040 LOOK AHEAD CARRY GEN.
7C5 CN1
DI001 8B9
DI011 8C9
DI021 8C9
DI031 8C9
DI041 8D9
DI051 8E9
DI061 8E9
DI071 8E9
DI081 8F9
DI091 8F9
DI101 8G9
DI111 8G9
DI121 8H9
DI131 8H9
DI141 8J9
DI151 8J9

I 0-2 ALU SOURCE
I 3-5 ALU FUNCTION
I 6-8 DESTINATION CONTROL

CPU

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SCALE—

NAME	TITLE	DATE
	DRAFT	13 APR 76
	CHK	
	ENGR	

TITLE SCHEMATIC 5/16 CPU

DWG NO 03867 D08 SHEET 4 OF 13

DWG NO 35-637

ROM CONTROL

OP REG

A108 19-167 QUAD D FF (NO PRESET)

A109 19-167 QUAD D FF (NO PRESET)

A118 19-186F20

A128 19-174 QUAD 2 TO 1 MUX (A0) TRISTATE

A127 19-174 QUAD 2 TO 1 MUX (A0) TRISTATE

A125 19-135 4 BIT CNTR STTL

A126 19-135 4 BIT CNTR STTL

A136 19-135 4 BIT CNTR STTL

A137 19-161 LA

A119 19-160 LA

A88 19-158 LOR

A116 19-154 LG

A117 19-154 LG

P5 1K XRP

R77 1K 7L4

XRP1

FINRQ 1049

MS001 3D9 MS011 3E9 MS021 3E9 MS031 3F9

MS041 3G9 MS051 3G9 MS061 3H9 MS071 3J9 D12 F9

RD161 6M6 RD171 6M6 RD181 6M7 RD191 6M7

CLKD1 12N6

RAR121 6EI RAR131 6FI RAR141 6FI RAR151 6FI

DR151 DR141 DR131 DR121 DR111 DR101 DR091 DR081

RAR150 115-2
RAR140 114-2
RAR130 116-2
RAR120 117-2
RAR081 6EI
RAR091 6EI
RAR101 6EI
RAR111 6EI
RAR110 118-2
RAR100 113-2
RAR090 107-2
RAR080 110-2
RAR071 6EI
RAR070 105-2
RAR060A 108-2
RAR061 6EI
RAR060 6HI

101-2 P5
106-2 P5
100-2 GND
105-2 GND
112-2 GND

1059 BRSELO
6M5 RD151
6M5 RD141
6M5 RD131
6M5 RD121
6M5 RD111
D1, 1084 D10
1084 D20
6M5 RD101

1158 SCLEOA
1084 DIEO
12N5 CLKO

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SCALE—

NAME	TITLE	DATE
	DRAFT	15 APR 76
	CHK	
	ENGR	

TITLE SCHEMATIC
5/16 CPU

TASK NO 03867
DWG NO 35-637 DO 5 REV

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

7N9 YD31
7N9 YD21
7N9 YD11
7N9 YD01
A101 19-179 LTTL
06 MSKO 10E9

NOTE 1

RAR061 5N8
CKRDO 12N6
RAR071 5N6
RAR081 5N4
RAR091 5N4
RAR101 5N4
RAR111 5N4
RAR121 5K1
RAR131 5K1
RAR141 5K1
RAR151 5K1
RAR060 5N8

7G6 FLR151 13
7F6 FLR141 12
7E6 FLR131 05
7E6 FLR121 04
A102 19-167 LDF
PSW151 8N1
PSW141 8N2
PSW131 8N3
PSW121 8N4
10C9 LDCCO

4H2 S071 13
4H2 S061 12
4H2 S051 05
4G2 S041 04
A56 19-167 LDF
PSW071 8N6
PSW061 8N6
PSW051 8N6
PSW040 10SG
PSW041 8N7

4F2 S031 13
4F2 S021 12
4F2 S011 05
4F2 S001 04
A38 19-167 LDF
PSW031 8N7
PSW021 8N7
PSW010 10N4
PSW011 8N7
PSW001 8N7
10D9 LPSW0
11S8 SCLR0A

PSW

A112 19-186F17
A113 19-186F14
A121 19-186F18
A122 19-186F15
A131 19-186F19
A132 19-186F16

PAGE 1
PAGE 0

RD001 10B1
RD011 10B1
RD021 10B1
RD031 4A1, 4A6, 7F1, 10C1, 10G6, 12H8
RD041 4A1, 4A6, 7C1, 10D1, 10G6
RD051 4A1, 4A6, 7C1, 10D1, 10F6
RD061 4A6, 10H6, 10L1
RD071 4A6, 10J6, 10L1
RD081 4A6, 10L6, 10M1
RD091 4B1, 4A6, 10K9
RD101 4A6, 5H9
RD111 4A6, 5F9
RD121 5F9, 8A6, 8F1, 10D1
RD131 5F9, 8A4, 10D1
RD141 4A1, 5F9, 8A4, 10E1
RD151 5F9, 7C1, 8N6, 8J9, 8K1, 10E1
RD161 5E1, 8N5, 10E7
RD171 5F1, 8A3, 8N5, 8K9, 10J1
RD181 5F1, 8A3, 8N5, 8K1, 10J1
RD191 5F1, 8A3, 8N4, 8K1, 8K9, 10J1
RD201 7B1, 8N3, 9E7, 10F1
RD211 7B1, 8N3, 9C6, 10G1
RD221 7B1, 8N2, 9B6, 10G1
RD231 7C1, 8N1, 9D6, 10G1

RDM

1. STRAP TO BE INSTALLED AT BOARD TEST.

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SCALE — | NAME | TITLE | DATE
TOLERANCE XXX ±.005, XX ±.02, X ±.06, ANGLES ±1° UNLESS OTHERWISE SPECIFIED
DRAFT 16APR76
CHK
ENGR

TITLE SCHEMATIC
5/16 CPU

TASK NO 03867
DWG NO 35-637 D08
SHEET 6 OF 13

SHIFT CONTROL

A123
19-213F01
PLA 5/16 SHIFT CONTROL

A114
19-199F03
PLA 5/16 FLAGS

FLR

FLAGS
MISC CONTROL YD & YS

A98
19-167
QUAD D FF
LDF

A79
19-181
ASYN 4 BIT
UP-DWN CNTR
LTTL

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SCALE—	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .09, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	19APR76
		CHK	
		ENGR	

TITLE SCHEMATIC
5/16 CPU

TASK NO. 03867
DWG NO. 35-637 DOB
SHEET NO. 7—13

DRAWING 64-251 B4539

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

DATA MULTIPLEXERS

MD MULTIPLEXER

REGISTER STACKS

CROSS SHIFT MULTIPLEXERS

A42 19-065 2:1 MUX STTL
A60 19-065
A77 19-065
A96 19-065
A54 19-041 4x4 REG. STACK
A63 19-041
A71 19-041
A80 19-041
A36 19-187 2:1 MUX W/S
A89 19-187
A45 19-187
A99 19-187
A92 19-073
A82 19-073 4:1 MUX (TRI-STATE)
A73 19-174
A64 19-174
A47 19-174 2:1 MUX LTTL
A83 19-159 LOR
A129 19-055 SG
A139 19-060 SG
A120 19-154 LG
A100 19-115 HA

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SCALE— | NAME | TITLE | DATE | DRAFT | CHK | ENGR

TITLE SCHEMATIC 5/16 CPU

TASK NO. 03867 | DWG NO. 35-637 | DO8 | SHEET OF 8—13

INTERDATA
2 Crescent Place Oceanport, New Jersey 07757

REVISIONS

I/O XCVRS

I/O CONTROL

IO BUFFER & CONTROL

A59 19-118 QUAD BUS TRANSCEIVER

A67 19-118 QUAD BUS TRANSCEIVER

A75 19-118 QUAD BUS TRANSCEIVER

A84 19-118 QUAD BUS TRANSCEIVER

A58 19-187

A66 19-187

J9 I00

A83 19-159 LDR

A40 19-042 ONE SHOT

FALSE SYNC

FCIN

FCOUT

FDAT

FSYN

SCALE—	NAME	TITLE	DATE
		DRAFT	21 APR 76
		CHK	
		ENGR	

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TITLE SCHEMATIC 5/16 CPU

DWG NO 03867

REV 35-637 D08

SHEET NO 9-13

DRAWING 44 231 24538

REVISIONS

A111 19-129 3:8 LINE DECODER STTL

A138 19-129

A130 19-129

A140 19-129

A142 19-168

A154 19-177 DUAL FOUR INPUT MUX LTTL

A166 19-177

A143 19-167 QUAD D FF LDF

RD DECODING

BRANCH LOGIC

NORMALLY STRAPPED: A TO C TO D & B TO E SEE TABLES 1 & 2 BELOW

TABLE 1. POWER UP SEQUENCING STRAPPING	TABLE 2. BREAKPOINT STRAPPING
AUTO RESTART (ROM) – A TO C & B TO D	ENABLE – B TO E
ALO (AUTOMATIC LOADER – A TO D & B TO C	DISABLE – A TO E
ASCII PROGRAMMER'S CONSOLE – A TO C TO D	

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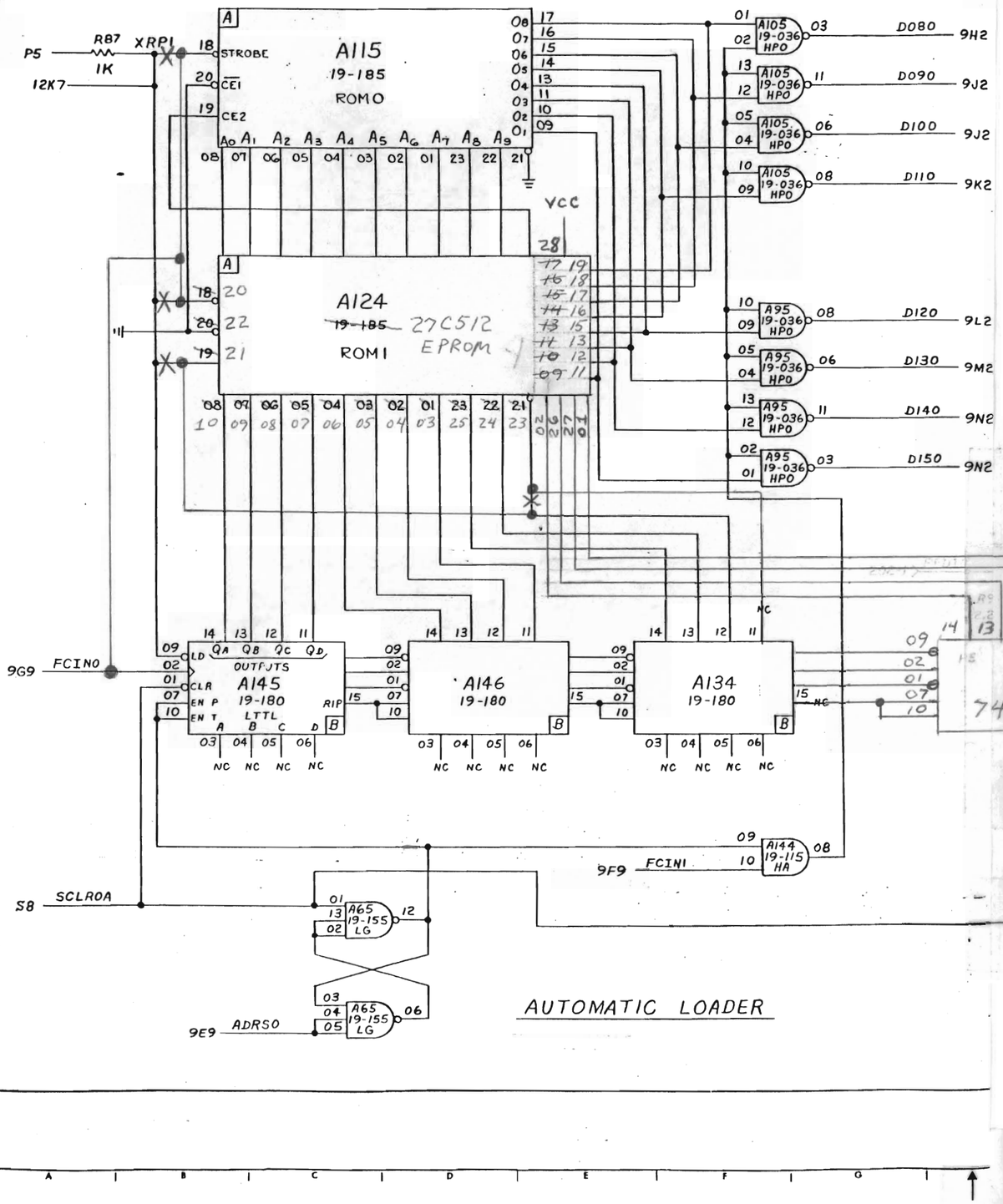
SCALE– | NAME | TITLE | DATE | DRAFT | CHK | ENGR

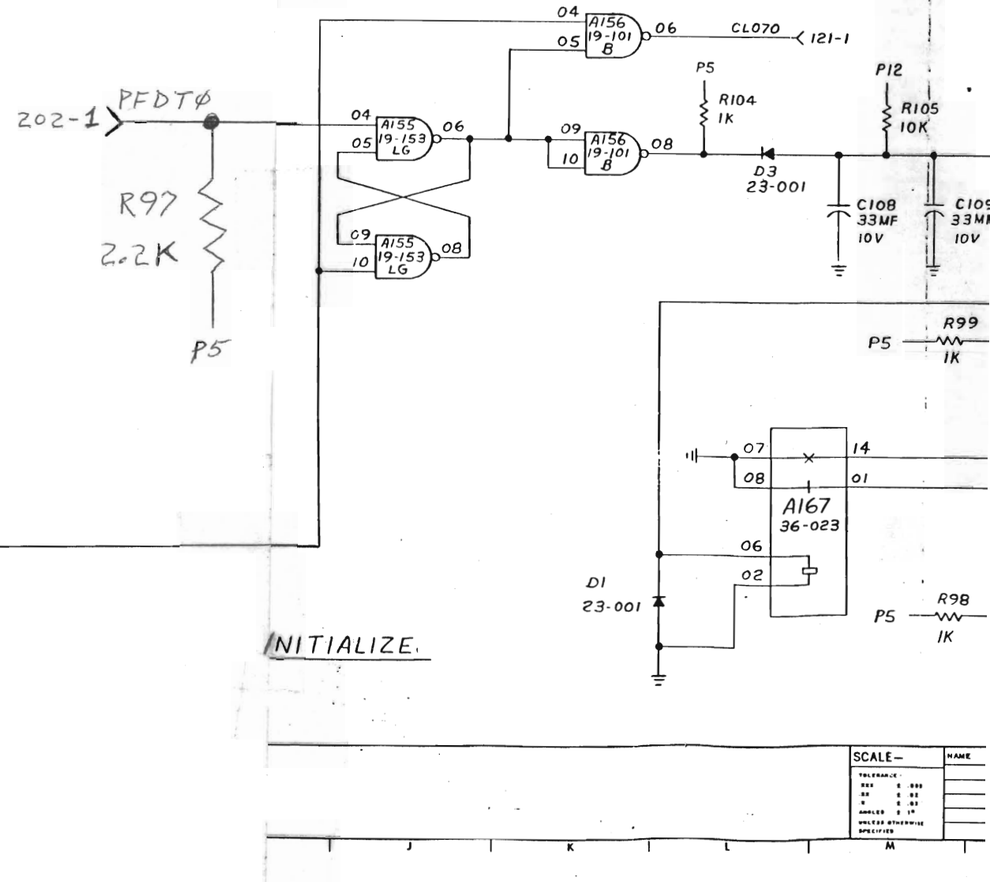
TITLE SCHEMATIC 5/16 CPU

TASK NO. 03867 | DWG NO. 35-637 D08 | SHEET OF 10 – 13

(With 27C512 EPROM)
11/13/95 AMD



AUTOMATIC LOADER



INITIALIZE.

REVISIONS

see previous page (new sheet 11)

A115
19-185
ROM0

A124
19-185
ROM1

A145
19-180
OUTFJTS
LTTL

A146
19-180

A134
19-180

P5 — R87 1K — XRP1 — 12K7

A105 19-036 HPO: D080 9H2; D090 9J2; D100 9J2; D110 9K2

A95 19-036 HPO: D120 9L2; D130 9M2; D140 9N2; D150 9N2

9G9 FCIN0

9F9 FCIN1 — A144 19-115 HA

S8 SCLR0A — A65 19-155 LG

9E9 ADRS0 — A65 19-155 LG

AUTOMATIC LOADER

202-1 PFDT0 — R97 2.2K — P5

A155 19-153 LG; A156 19-101 B

CL070 < 121-1

P5 — R104 1K — D3 23-001 — C108 33MF 10V — C109 33MF 10V

P12 — R105 10K — Q2 20-010 — Q1 20-010 — R108 220 — P12

P5 — R99 1K

A167 36-023

D1 23-001

P5 — R98 1K — SCLR0 < 126-1 < 36-C

A156 19-101 B — SCLR0A — A8, 2F4, 5G9, 6A8, 9K9, 10M1, 10A9, 12A6, 12H8, 12C2

INITIALIZE

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SCALE—

	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
5/16 CPU

TASK NO. 03867
DWG NO. 35-637 D08

SHEET OF 11 — 13

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
AREA J5: A148-15 WAS TO A148-04. AREA J3: R123 WAS SPEC'D R94. AREA M5: ADDED TP4 & NEW R94. ADDED STRAP OPTIONS ON CKRDO & CKRDI (AREA N6)
PC	M	SCR 3274	APP 6-9-77	BO1

MEMORY TIMING

CLOCKS

FMEM FRAS FXRAS FCAD FCAS

N4 DDCLKO N3 DCLKO N5 CLKO 10AG MEM1

2F1 FMEMO 2G4 FRASI 2F7 ERFRSHO 2K4 FCADI H7,2J4 FCASI

11S8 SCLROA R5 CLK1 2H8 RFRSH1

P5 R59 1K 106-1 SCATNO R61 1K 206-1 RCATNO

11S8 SCLROA 10D9 LPSWO R66 220 FAULTO 107-1

P5 R89 1K TP2 EXOSCO TP GND P5 R88 1K TP1 DISOSCO

R92 1K R91 2.2K C107 9-35PF L1 4.7μh

P5 R123 1K XRP3 10N1, 10C7 DCLKI

P5 R93 1K 2E7 103-2 9L9 FTITO IOSTOPO 10A6 MEM1 K1 FCAS1

XRP1 11A2 FSPATNI NC FSPATNO 10R6 DSTOPO 10F6 BRANCHO 10B4

103-1 C3 R100 4.7K 104-1 C1S D2 23-001 R101 4.7K P5 R102 4.7K Q3 20-001 105-1 DNMI TP3 P5 R103 1K

NMI N6 CKRDI 10C1 RD451 6M4 RD031 10L4 SAT0 11S8 SCLROA

DCLKO A1 DDCLKO A1, 9N6, 10B9 DDCLKI 2F1, 8A8, 9J4 TP4 R94 1K P5

CLK1 C2, 7R1, 8E1, 8B5, 9L4 CLKO A1, 2B4, 5G9 104-2 BCLKI 04-C

CKRDO 6E1, 7L1, 10R7, 10M1, 10B6 (SEE NOTE 1) CKRDI G8, 5J1, 10C6

DESCLKO 4A8 DESCLKI 7D1 DESTPO 8E1, 8B5

TO BE INSTALLED AT BOARD TEST.

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SCALE— | DRAFT 9 JUNE 76 | CHK | ENGR

TITLE SCHEMATIC 5/16 CPU

TAB NO 03867 SHEET OF 12—13

DWG NO 35-637R01 D08

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

0	1	2	
0	0	0	–
0	0	1	DI
0	1	0	D
0	1	1	BRANCH
1	0	0	MW
1	0	1	MR
1	1	0	–
1	1	1	IRJ

DESTINATION

12	13	14	
0	0	0	I/O
0	0	1	PSW
0	1	0	FLR
0	1	1	NULL, MEM
1	0	0	MRO
1	0	1	MAR
1	1	0	LOC
1	1	1	MDR

	3	4	5
S ← ALU, Q ← ALU	0	0	0
S ← ALU	0	0	1
S ← YS, YD ← ALU	0	1	0
YD ← ALU	0	1	1
YS ← ALU	1	0	0
YD & Q ← R ALU	1	0	1
YD ← R ALU	1	1	0
YD & Q ← L ALU	1	1	1
YD ← L ALU			

	12	13	14
	0	0	0
	0	0	1

	6	7	8
R + S	0	0	0
S · R	0	0	1
R · S	0	1	0
R ⊻ S	0	1	1
R + S	1	0	0
R̄ · S	1	0	1
R ⊕ S	1	1	0
R ⊙ S	1	1	1

	15	16	23
NOT BRANCH	1	IMMEDIATE DATA	

	15	16
CROSS SHIFT	0	1

	R	S
	(A) YS	YD (B)
	NULL	Q
	NULL	YD (B)
ILLEGAL COMBINATION →	NULL	YS (A)
	D	YD (A)
	D	Q
	D	NULL

9	10	11
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

SOURCE

17	18	19	
0	0	0	I/O
0	0	1	PSW
0	1	0	YS I
0	1	1	MEM
1	0	0	MRO
1	0	1	MAR
1	1	0	LOC
1	1	1	MDR

	20	21	22	23
I/O ACR/ACK	0	0	0	1
I/O CMD/STAT	0	0	1	0
I/O DA/DR	0	1	0	0
I/O DACK	1	0	0	1

NOT IMMEDIATE, NOT BRANCH

–X2 IF AMOD

0	1	2		9	
0	1	1		0	BT
0	1	1		1	BF

BRANCH ADDRESS

	3	4	5	6	7	8
C	0	0	0	1	1	1
V	0	0	1	0	1	1
G	0	0	1	1	0	1
L	0	0	1	1	1	0
ATN	0	1	0	1	1	1
DMA	0	1	1	0	1	1
CATN	0	1	1	1	0	1
PWRUP ← RESETS AFTER 64 REFRESHES	0	1	1	1	1	0
MASK	1	0	0	1	1	1
ALO	1	0	1	0	1	1
ARST (STRAP)	1	0	1	1	0	1
YDCARY ← SETS FOR ONE CLOCK AS A RESULT OF YDPI	1	0	1	1	1	0
UNCONDITIONAL	1	1	0	1	1	1
HWIO	1	1	1	0	1	1
SPATN ← BRANCH ON SPATN ONLY RESETS SPATN	1	1	1	1	0	1
BKPT	1	1	1	1	1	0

NOT IMMEDIATE, NOT I/O

IF LSR YD & Q, YD, JAM
MEANS CI + CO NO
ROTATE

	20	21	22	23
CLRYD	0	0	0	0
YDPI	0	0	0	1
YDMI	0	0	1	0
(JAM) INC/DEC, CO	0	0	1	1
AMOD	0	1	0	0
REFRESH	0	1	0	1
INC/DEC, F	0	1	1	0
	0	1	1	1

	20	21	22	23
CI	1	X	X	1
CO	1	X	1	X
FLAGS	1	1	X	X
	1	0	0	0

MICRO-PROGRAM FORMAT

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SCALE –	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	4-25-77
		CHK	
		ENGR	

TITLE: SCHEMATIC 5/16 CPU

TASK NO. 03867 | DWG NO. 35-637 D08 | SHEET OF 13 — 13

BRUNING 44-231 2453

REVISIONS

ZONE	PRODUCTION APPROVAL	INIT	DATE
	DEV	DJC	4-11-77
	PROD	JMC	4-11-77

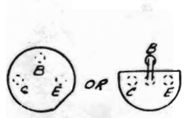
REVISED CIRCUITRY PER ROB COMPER. R18 WAS ITEM 17. RC3 (ITEM 26) WAS SPEC'D AS C28 ITEM 43. R20 WAS SPEC'D AS R18. ADDED R26 (ITEM 36), R27 (ITEM 30) & C32 (ITEM 44). IC A01 WAS SPEC'D AS ITEM 23.

PE	EC	3238	WF	5-31-77	R01

RELEASED FOR PRODUCTION
MFG ENG [signature] DATE 6/8/77

IC A01 VARIATION NOTE WAS NOT SPEC'D. REVISED VARIATION TABLE.

GS	[signature]	3301		8-1-77	R02



TYP. FOR Q1 & Q2
(ITEM 23)
(VIEWED FROM APP. SIDE)

SEE VARIATION TABLE

50 TYP
INSTALL ON SOLDER SIDE
(41 PLACES)

14.550 REF

REF
6.075

CONN A
CONN 2
CONN 3

49 TYP
INSTALL ON APP SIDE
(93 PLACES)

1

52,53
INSTALL ITEM 53 ON SOLDER SIDE

FO3	ALL COMPONENTS SHOWN LESS ITEM 20
FO2	ALL COMPONENTS SHOWN
FO1	ALL COMPONENTS LESS THOSE IN THE CROSS HASHED AREA
VAR	

COMPONENT	REF. DESIGNATIONS
ICS	A01, A02, A04-A06, A08-A39
RESISTORS	R1-R27
CAPACITORS	C1-C27, C29-C32
DIODES	D1-D10
TRANSISTORS	Q1, Q2

DIMENSIONS ARE IN INCHES.

THIS INFORMATION IS PROPRIETARY AND IS SUP... FOR ANY PURPOSE UNLESS SPECIFICALLY INDICATED

NAME	TITLE	DATE
S. ROBBINS	DRAFT	3-17-77
	CHK	6-13-77
D. FRANKENBERGER	ENGR	6-13-77
R. BARKER	Q.C.	6-13-77
M. DEMONDE	MGR	6-13-77

TITLE ASSEMPLY
5/16 MICRO BUS

TASK NO. 03867
DWG NO. 35-638P0003
SHT OF 1-1

CONN 2		
ROW 1	PIN	ROW 2
ENBL*1	00	GND
VPAIN	01	
RESETO	02	
RENDO	03	
WRITEO	04	
CIB	05	
MBACKO	06	
MBATNO	07	
RENDYO	08	
DATNC	09	
DMREQ	10	
WRDYO	11	
	12	
	13	
	14	
	15	
	16	GND

CONN 3		
ROW 1	PIN	ROW 2
AD15O	00	GND
AD14O	01	
AD13O	02	
AD12O	03	
AD11O	04	
AD10O	05	
AD09O	06	
AD08O	07	
D15O	08	
D14O	09	
D13O	10	
D12O	11	
D11O	12	
D10O	13	
D09O	14	
D08O	15	
	16	GND

CONN A		
ROW 1	PIN	ROW 2
	00	
AREFO	01	
GND (TDATA)	02	GND
DU	03	GND
RDATA	04	TDATA

CONN C	
PIN	MNEMONIC
0	PI2
1	P5
2	GND
3	FINRI
4	BCLKI
5	P5
6	GND
7	D08O
8	D10O
9	D09O
10	D11O
11	D13O
12	D15O
13	DACKO
14	D14O
15	D12O
16	GND
17	ACKO
18	TACKO
19	ADRSO
20	CMDO
21	DAO
22	DATAO
23	SRO
24	DRO
25	D00O
26	D01O
27	D02O
28	D03O
29	D04O
30	D05O
31	DXO
32	D07O
33	INT
34	ATNO
35	ADO
36	SCLRO
37	ATNOA
38	P5
39	SYNO
40	GND

BAUD RATE TABLE

STRAPPING	BAUD RATE	FREQ (Hz)	PERIOD (μSec)
A TO B	110	7044	141.9
A TO B	330	21132	47.3
A TO C	1200	76800	13.0
A TO C	1320	84480	11.8

BAUD RATE X 64 = FREQ. (Hz)

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV AJF	4-11-77
	PROJ	

ALLEGRA ADDED BAFO TO CONN A TABLE. AREA N3 FOI WAS R01, FOR WAS L'OR. REVISED SHEET 4.

P	MC	3238	AJF	5-31-77	R01

RELEASED FOR PRODUCTION
ENG [illegible] DATE 6/1/77

AREA M9 ADDED 35-638 FO3 TO TABLE. REVISED SHT 4.

GS	JT	3301		8-1-77	R02

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

BOARD	REV
35-638F01	R02
35-638F02	R03
35 638F03	R00

REV	2	-	-	3
SHEET	1	2		4

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SCALE –	NAME	TITLE	DATE
TOLERANCE XXX ± .005 XX ± .02 X ± .1 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	R.EDWARDS	DRAFT	12-8-76
	H.MATTEE	CHK	6-13-77
	D.FRANCHEVILLE	ENGR	6-13-77
	R.A.BARKER		6-13-77
	S.MESSINA	MGR	6-13-77

TITLE FUNCTIONAL SCHEMATIC 5/16 MICRO BUS

TABS NO. 02-0867 SHEET OF
DWG NO. 35-638 R02 D08 1 4

BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

12-C D150 → D150 → 108-3 (4A3)
14-C D140 → D140 → 109-3 (4A3)
11-C D130 → D130 → 110-3 (4A3)
15-C D120 → D120 → 111-3 (4A4)
10-C D110 → D110 → 112-3 (4A5)
8-C D100 → D100 → 113-3 (4A5)
9-C D090 → D090 → 114-3 (4A6)
7-C D080 → D080 → 115-3 (4A6)
32-C D070 → AD150 → 100-3 (4A2)
31-C D060 → AD140 → 101-3 (4A2)
30-C D050 → AD130 → 102-3 (4A2)
29-C D040 → AD120 → 103-3 (4A2)
28-C D030 → AD110 → 104-3 (4A2)
27-C D020 → AD100 → 105-3 (4A2)
26-C D010 → AD090 → 106-3 (4A1)
25-C D000 → AD080 → 107-3 (4A1)

A36 19-206 QUAD TRI-STATE BUS T/R
P5 R25 1K

04 → 02 AD080A (D) → 1
03 AD081 (F)
07 → 05 AD090A (H) → 3
06 AD091 (K)
12 → 14 AD100A (E) → 2
13 AD101 (G)
9 → 11 AD110A (J) → 4
10 AD111 (L)
01

A37 19-156 LG: 13, 10, 12, 09 → 08 → ADRSYNO 3L7
A24 19-160 LA: 13, 12 → 11
A25 19-154 LG: 19-C ADRS0 → 03 → 04 → ADRS1
A23 19-165 3 OF 8 DC: 04, 02, 05, 03, 01 → 06 → ADDA 3B1
3L5 DRDYO → 04; A27 19-153 LG: 05 → 06 → ADO → 35-C
A28 19-138 LN: 3-C FINR1 → 03, 02 → 01
JA SCLR1
A29 19-154 LG: 36-C SCLR0 → 01 → 02; 13 → 12 → SCLR0A 4H2

3H7 ENABLE0 → 10, 15 → 09 → ENABLE1 (100-2) 4A9
3M6 VPR0 → 12 → 11 → VPR1A (101-2) 4D1
3F2 C/D → 02, 01 → 03 → C/D (105-2) 4E1
3F1 WRITE1 → 04 → 05 → WRITE0 (104-2) 4E1
3F1 READ1 → 06 → 07 → READ0 (103-2)
F9 SCLR1 → 14 → 13 → RESET0 (102-2)

A34 19-134 HEX TRI-STATE INVERT A

3L5 MBTACK1 → 10, 15 → 09 → MBACK0 (106-2)
3L4 MUXTCK1 → 06 → 07 → TACK0 (18-C)
107-2 MBATN0 → 12 → 11 → MBATN1 3A5
P5 R24 1K → 01 → 13 → READY1 3A6
108-2 READY0 → 14 → 03 → NC
P5 R23 1K → NC 02 → 05 → NC
NC 04

A35 19-134 HEX TRI-STATE INVERTER B

200-2 … 208-2 → 200-3 … 216-3

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SCALE—	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	P.EDWARDS	DRAFT	10-25-76
		CHK	
		ENGR	

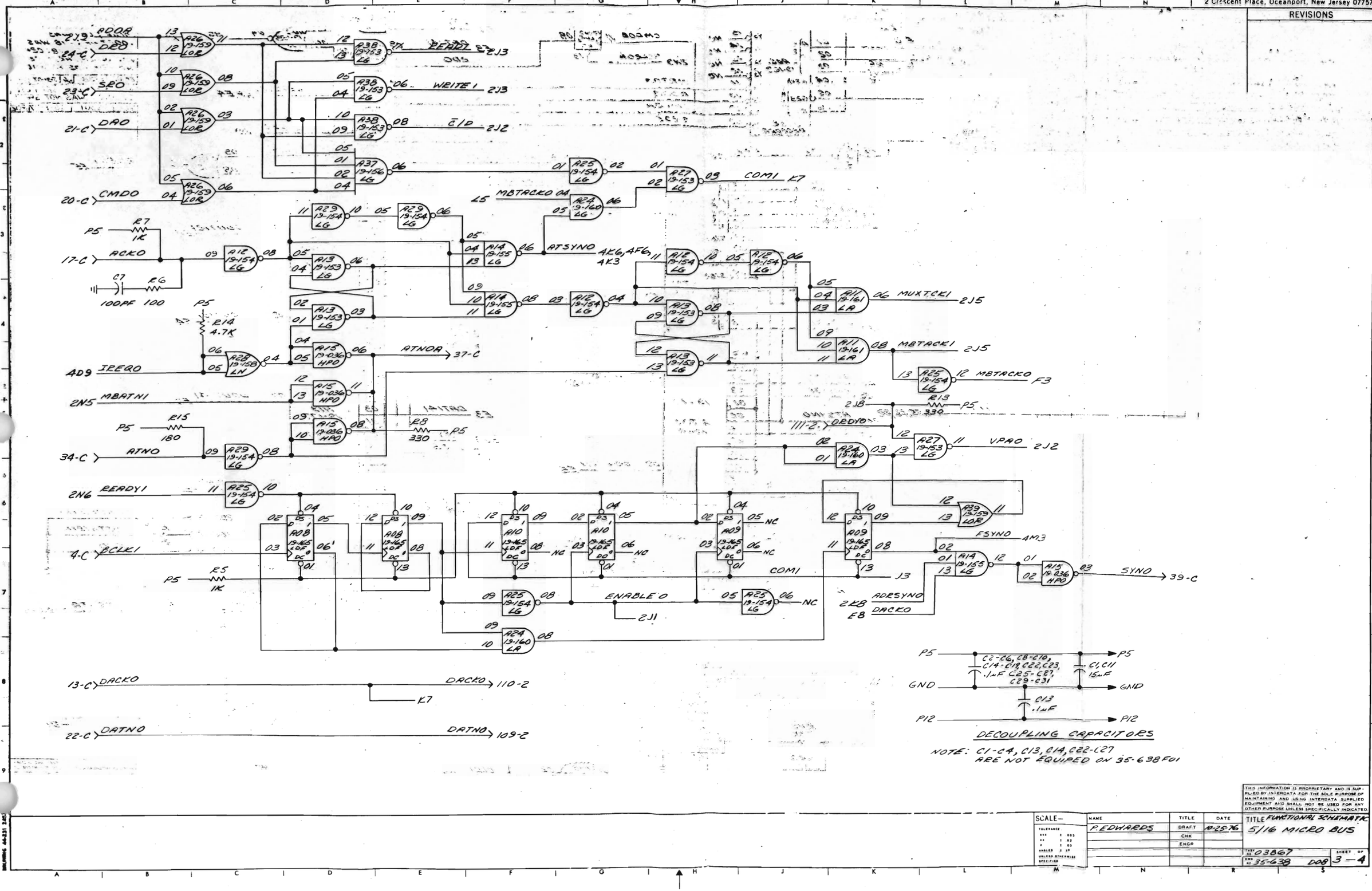
TITLE FUNCTIONAL SCHEMATIC 5/16 MICRO BUS

TASK NO 03867 CMS NO 35-638 DO8 SHEET OF 2-4

DRAWING 44-E31 E4539

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



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	NAME	TITLE	DATE
	P. EDWARDS	DRAFT	10-25-76
		CHK	
		ENGR	

SCALE—

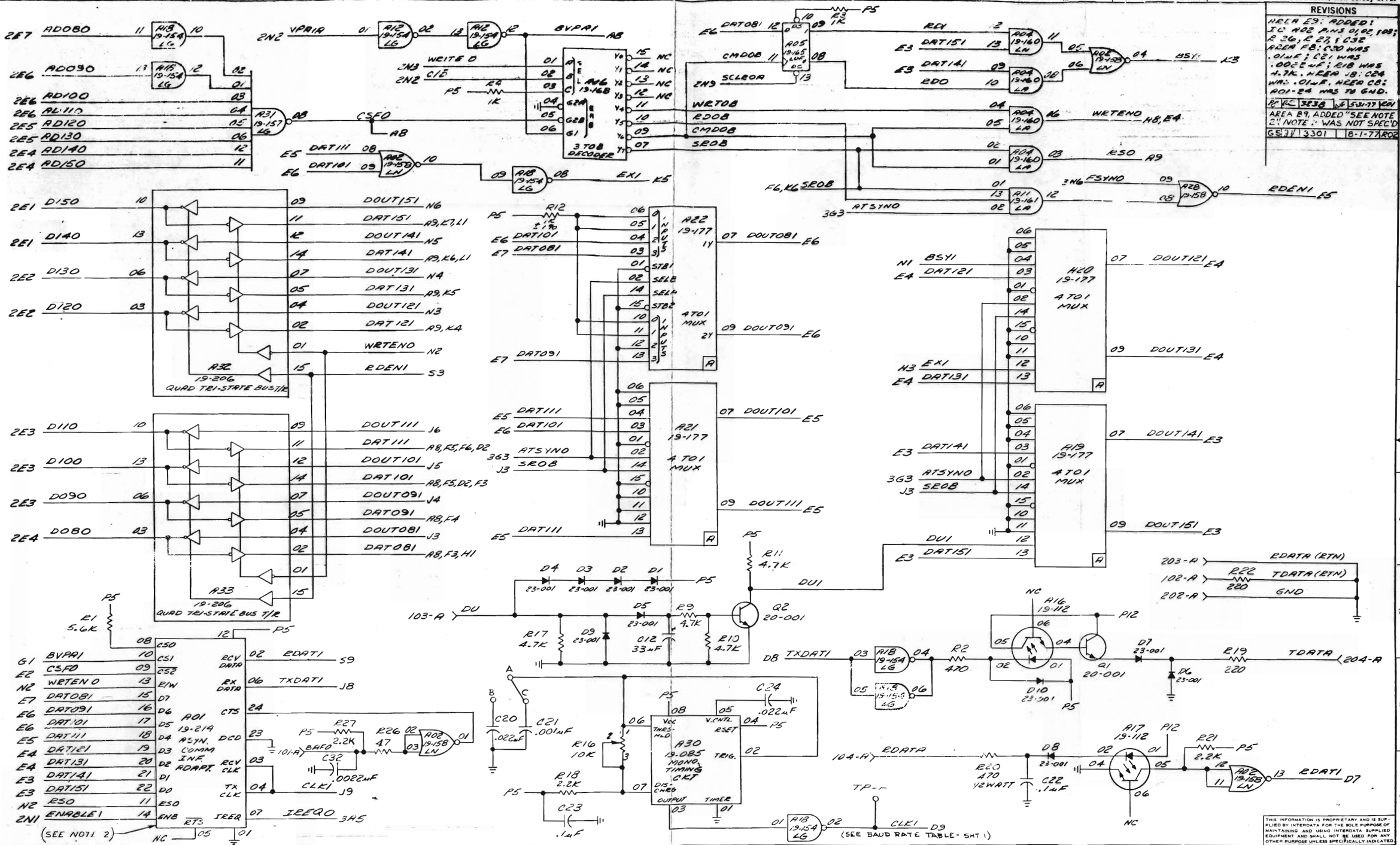
TITLE FUNCTIONAL SCHEMATIC
5/16 MICRO BUS

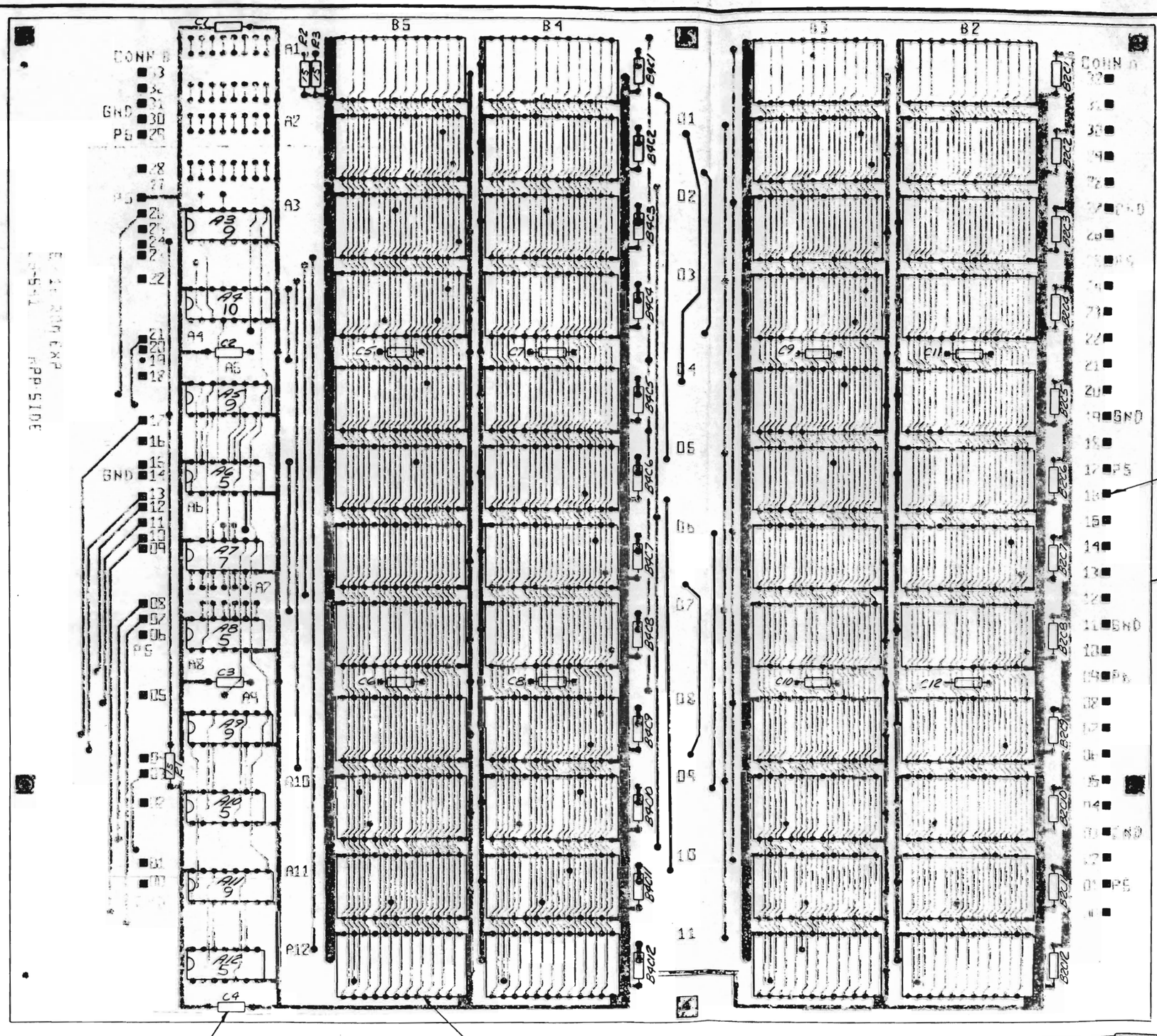
TABY NO 03867
SIZE NO 35-638 D08
SHEET OF 3—4

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

LTR	DESCRIPTION	ECN	DATE	APPR
	HELP E9: ADDED: IC A02 PINS 01,02,10&13; R 26, C 27, & C32 AREA F8: C30 WAS .01uF; C21 WAS .0022uF; R18 WAS 4.7K. AREA J8: C24 WAS .01uF. AREA C8: A01-24 WAS TO GND.			
B		3838	5-31-77	KRH
	AREA B9, ADDED "SEE NOTE 2" NOTE 1: WAS NOT SPEC'D			
C		3301	8-1-77	ROB





REVISIONS

RELEASED FOR PRODUCTION
MFG ENG. _____ DATE. _____

REMOVED WIRE WRAP STAKE REF B-19.			
G S	3263	7-14-77	A01

COMPONENT	REF. DESIGNATIONS
INTEGRATED CKT.	A3 - A12
CAPACITOR	C1-C12, B2C1-B2C12, B4C1-B4C12
RESISTOR	R1-R3

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NAME	TITLE	DATE
J. HELVATY	DRAFT	3-30-77
W. LIN BERT	CHK	3-30-77
D. FRANKENBERGER	ENGR	6-13-77
R. BARKER	Q.C.	6-13-77
J. LEMONDE	MGR	6-13-77

TITLE ASSEMBLY
5/16 ROM
EXPANSION

TASK NO. 03367 SHT OF 1-1

DWG NO. 5639A01 D03

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
RELEASED FOR PRODUCTION
ENG. ___ DATE 6/14/77

05-B) GDDCLK1 — A7 19-154 LG (09 → 08)
28-B) FRFRSH0 — A7 19-154 LG (13 → 12)
22-B) FRHS1

A4 19-168 LTTL
01 A, 02 B, 03 C, 04 G2A, 05 G2B, 06 G1
Y0 15 N.C.; Y1 14 N.C.; Y2 13 ROMENO20 2H6; Y3 12 ROMENO30 2H4; Y4 11 ROMENO90 2H2; Y5 10 ROMENO50 2A6; Y6 09 ROMENO60 2A4; Y7 07 ROMENO70 2A2

23-B) B001
24-B) B011
25-B) B021
A3 19-167 CLR LDF
04 D, 05 D, 12 D, N.C. 13 D, 09, 01 CLR
Q 02; Q̄ 03 N.C.; Q 07; Q̄ 06 N.C.; Q 10; Q̄ 11 N.C.; Q 15 N.C.; Q̄ 14 N.C.

26-B) B031
21-B) B041
18-B) B051
16-B) B061
A5 19-167 CLR LDF
13, 05, 12, 04, 09, 01 CLR
15, 14, 07, 06, N.C. 10, 11, N.C. 02, 03

17-B) B071
13-B) B081
12-B) B091
11-B) B101
A9 19-167 CLR LDF
04, 05, 12, 13, 09, 01 CLR
N.C. 02, 03; N.C. 07, 06; N.C. 10, 11; N.C. 15, 14

10-B) B111
07-B) B121
08-B) B131
09-B) B141
A11 19-167 CLR LDF
04, 05, 12, 13, 09, 01 CLR
N.C. 02, 03; N.C. 07, 06; N.C. 10, 11; N.C. 15, 14

P5 — R1 1K

A6 19-124 SB
01, 02 → 03 MA030 2A3
12, 13 → 11 MA031 2A2
04, 05 → 06 MA040 2A2
09, 10 → 08 MA041 2A2
04, 05 → 06 MA051 2A1
01, 02 → 03 MA061 2A1

A10 19-124 SB
12, 13 → 11 MA071 2A2
09, 10 → 08 MA081 2A2
04, 05 → 06 MA091 2A1
01, 02 → 03 MA101 2A1

A12 19-124 SB
12, 13 → 11 MA111 2A1
09, 10 → 08 MA121 2A1
04, 05 → 06 MA131 2A1
01, 02 → 03 MA141 2A1

P12	N.C.	33	———	N.C.
P12	N.C.	32	MS001	
GND		31	N5	N.C.
GND		30	MS011	
P5		29	P12	N.C.
FRFRSHO		28	MS021	
P5		27	GND	
B031		26	MS031	
B021		25	P5	
B011		24	MS041	
B001		23	N5	N.C.
FRAS1		22	MS051	
B041		21	P5	N.C.
WTI	N.C.	20	MS061	
———	N.C.	19	GND	
B051		18	MS071	
B071		17	P5	
B061		16	MS081	
RFRSH	N.C.	15	N5	N.C.
GND		14	MS091	
B081		13	P12	N.C.
B091		12	MS101	
B101		11	GND	
B111		10	MS111	
RFCLKO	N.C.	09	P5	
B131		08	MS121	
B121		07	N5	N.C.
P5		06	MS131	
GDDCLK1		05	P12	N.C.
B151		04	MS141	
B141		03	GND	
FCAD1	N.C.	02	MS151	
P12	N.C.	01	P5	
GND		00	FCAS1	N.C.
CONN. B		PIN	CONN. A	

TABLE A

SEE TABLE A — P5 — C1-C-2 BC1-1-23-C12 BQ-1-184-C12 .1UF — GND — P5

REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.
BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

35-639	R00

REV		
SHEET	1	2

BRUNING 44-231 BASM

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SCALE— TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
A. SWEAK	DRAFT	2-8-77
W. LIMPERT	CHK	6-13-77
D. FRANKELBERGER	ENGR	6-13-77
R. BARKER	Q.C.	6-13-77
N. LEMONDE	MGR.	6-13-77

TITLE SCHEMATIC 5/16 ROM EXP.
TASK NO 03867
DWG NO 35-639 DOB
SHEET OF 1-2

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

1J5 MA06I
1J5 MA05I
1J9 MA18I
1J9 MA13I
1J8 MA12I
1J8 MA11I
1J7 MA10I
1J7 MA09I
1J6 MA08I
1J6 MA07I

1J4 MA03I
1J4 MA04O
1J2 ROMEN07O

1J4 MA04I
1J4 MA03O

1J2 ROMEN06O

1J2 ROMEN05O

1J2 ROMEN04O

	B5 (SEE NOTE 1)	1024 x 8 BIT ROM B4 (SEE NOTE 1)	2048x8 BIT ROM B4 (SEE NOTE 1)
	00	x'F800'-x'FFFF' 00	N/A
	01	x'F000'-x'F7FF' 01	x'F000'-x'FFFF'
	02	x'E800'-x'EFFF' 02	N/A
	03	x'E000'-x'E7FF' 03	x'C000'-x'EFFF'
	04	x'D800'-x'DFFF' 04	N/A
	05	x'D000'-xD7FF' 05	x'D000'-x'DFFF'
	06	x'C800'-x'CFFF' 06	N/A
	07	x'C000'-xC7FF' 07	x'C000'-x'CFFF'
	08	x'B800'-x'BFFF' 08	N/A
	09	x'B000'-x'B7FF' 09	x'B000'-x'BFFF'
	10	x'A800'-x'AFFF' 10	N/A
	11	x'A000'-x'A7FF' 11	x'A000'-x'AFFF'

1J1 ROMEN03O
1J1 ROMEN02O

	IC24x8 BIT ROM B3 (SEE NOTE 1)	2048 x 8 BIT ROM B3 (SEE NOTE 1)	1024x8 BIT ROM B2 (SEE NOTE 1)	2048x8 BIT ROM B2 (SEE NOTE 1)
	x'9800'-x'9FFF' 00	N/A	00	
	x'9000'-x'97FF' 01	x'9000'-x'9FFF'	01	
	x'8800'-x'8FFF' 02	N/A	02	
	x'8000'-x'87FF' 03	x'8000'-x'8FFF'	03	
	x'7800'-x'7FFF' 04	N/A	04	
	x'7000'-x'77FF' 05	x'7000'-x'7FFF'	05	
	x'6800'-x'6FFF' 06	N/A	06	
	x'6000'-x'67FF' 07	x'6000'-x'6FFF'	07	
	x'5800'-x'5FFF' 08	N/A	08	
	x'5000'-x'57FF' 09	x'5000'-x'5FFF'	09	
	x'4800'-x'4FFF' 10	N/A	10	
	x'4000'-x'47FF' 11	x'4000'-x'4FFF'	11	

R2 1K P5
R3 1K P5

MS151 → 02-A
MS141 → 04-A
MS131 → 06-A
MS121 → 08-A
MS111 → 10-A
MS101 → 12-A
MS091 → 14-A
MS081 → 16-A
} LS BYTE

MS071 → 18-A
MS061 → 20-A
MS051 → 22-A
MS041 → 24-A
MS031 → 26-A
MS021 → 28-A
MS011 → 30-A
MS001 → 32-A
} MS BYTE

NOTES:
1. INTEGRATED CIRCUITS B800-B811, B300-B311, B400-B411, B500-B511 TO BE CUSTOMER INSTALLED.

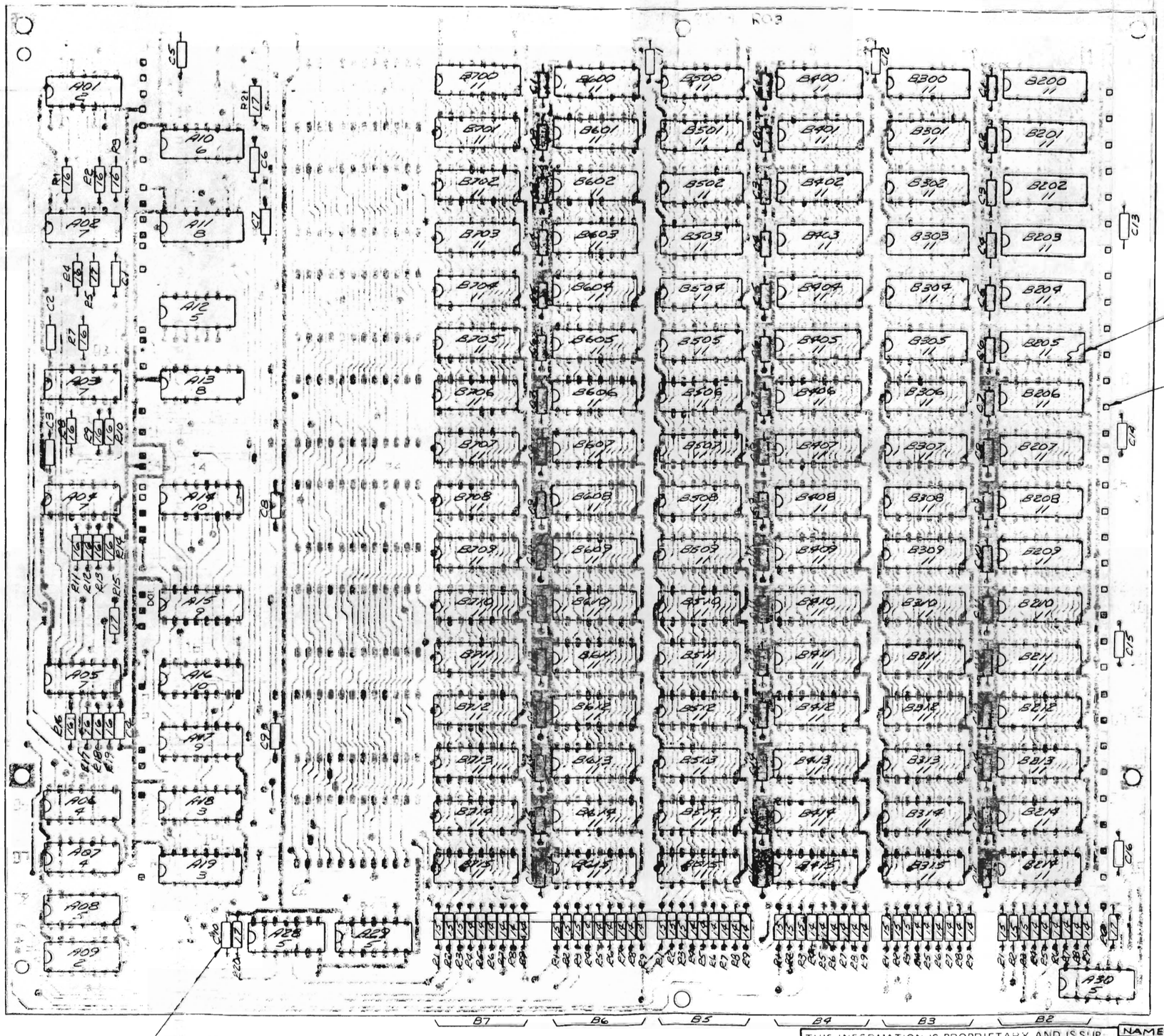
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE SCHEMATIC
5/16 ROM EXP.
TASK NO 03867
DWG NO 35-639 D08
SHEET OF 2—2

BRUNING 44-231 24830



REVISIONS

				REV LET OF PC BOARD A... WAS REQ. ADDED R21.
GH	11	7-7	3265	RC
				RELEASED FOR PRODUCTION
				SPRAGUE WIRE WRAP STA...
	JV	A3	7-14-77	KR

VARIATION	EQUIP. (ITEM 11) IN LOCATION	EQUIP. (ITEM 20) IN LOCATION
F01	B200 THRU B215	B2-E1 THRU B2-E9
F02	B210 THRU B215 B300 THRU B315	B2-C1 THRU B2-C16
F03	B200 THRU B215 B300 THRU B315 B400 THRU B415	B2-C1 THRU B2-C16 B3-E1 THRU B3-E9 B4-E1 THRU B4-E9
F04	B200 THRU B215 B300 THRU B315 B400 THRU B415 B500 THRU B515	B2-C1 THRU B2-C16 B3-E1 THRU B3-E9 B4-E1 THRU B4-E9 B5-E1 THRU B5-E9
F05	B200 THRU B215 B300 THRU B315 B400 THRU B415 B500 THRU B515 B600 THRU B615	B2-C1 THRU B2-C16 B3-E1 THRU B3-E9 B4-E1 THRU B4-E9 B5-E1 THRU B5-E9 B6-E1 THRU B6-E9
F06	ALL LOCATIONS	ALL LOCATIONS

COMPONENT	REF. DESIGNATIONS
INTEGRATED CIRCUIT	A01 THRU A19, A28, A29, A30 B200 THRU B215, B300 THRU B315, B400 THRU B415, B500 THRU B515, B600 THRU B615, B700 THRU B715
RESISTORS	R1 THRU R21, BR1-B2R9, B3R1-B3R9, B4R1-B4R9, B5R1-B5R9, B6R1-B6R9, B7R1-B7R9
CAPACITORS	C1 THRU C16, B2C1-B2C16, B4C1-B4C16, B6C1-B6C16

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NAME	TITLE	DATE
J. HELVATY	DRAFT	5-22-77
W. LIMBERT	CHK	6-13-77
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TITLE ASSEMBLY
5/16 RAM EXPANSION

TASK NO. 03567 SHT. OF 1-1

DWG NO. 35-670-2103

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REVISIONS			
PRE PRODUCTION APPROVAL	DEV PROD	INIT DJF	DATE 4-27-77

REVISED SHT 2. ORIGINAL ISSUE WAS R01

CM #	3265	6-5-77	R02

RELEASED FOR PRODUCTION
ENG. _____ DATE 6/14/77

CONN A		CONN B
FC951	0	GND
P5	1	———
MS151	2	CAD1
GND	3	B141
MS141	4	B151
P12	5	GDDCLK1
MS131	6	P5
N5	7	B121
MS121	8	B131
P5	9	RFCLK0
MS111	10	B111
GND	11	B101
MS101	12	B091
P12	13	B081
MS091	14	GND
N5	15	RFRSH
MS081	16	B061
P5	17	B071
MS071	18	B051
GND	19	———
MS061	20	WT1
P12	21	B041
MS051	22	FRAS1
N5	23	B001
MS041	24	B011
P5	25	B021
MS031	26	B031
GND	27	P5
MS021	28	FRFRSH0
P12	29	P5
MS011	30	GND
N5	31	GND
MS001	32	P12
———	33	P12

P5 → 01-A, 06-B, 09-A, 27-B, 17-A, 29-B, 25-A
P12 → 05-A, 13-A, 32-B, 21-A, 33-B, 29-A
N5 → 07-A, 15-A, 23-A, 31-A
GROUND → 03-A, 00-B, 11-A, 14-B, 19-A, 30-B, 27-A, 31-B
* .1mf

* FOR DECOUPLING CAP INFORMATION REFER TO 35-640D03

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F02	R02
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F04	R02
F05	R02
F06	R02

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TASK NO. 03867
DWG NO. 35-640 R02D08
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PMS 09-11/13-17 ON IC'S				
A20 THRU A27 WIRED SO MA IN REVERSE ORDER				
ZM	11	3265	6577	R01

A17 19-180 — A15 19-180 4 BIT COUNTER — A24 (SEE NOTE 1) — A25 (SEE NOTE 1) — A26 (SEE NOTE 1) — A27 (SEE NOTE 1) — A20 (SEE NOTE 1) — A21 (SEE NOTE 1) — A22 (SEE NOTE 1) — A23 (SEE NOTE 1) — A10 19-129 3 TO 8 DECODER STTL — A01 19-057 3G — A12 19-124 5B — A28 19-124 5B — A8 19-124 5F — A07 19-115 HA — A06 19-115 HA — A09 19-057 5G

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5/16 RAM EXPANSION

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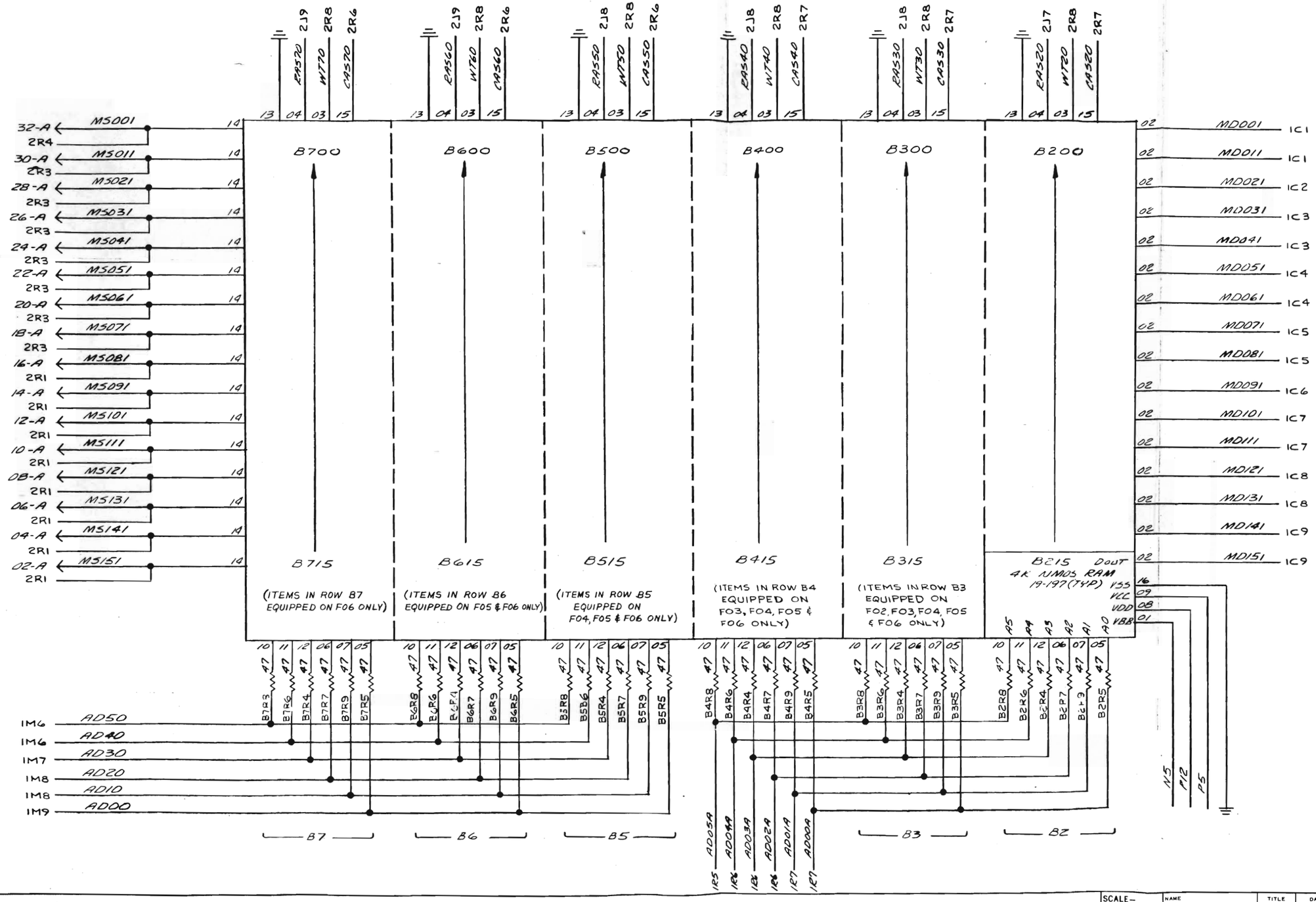

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THIS PACKAGE UPDATES THE FOLLOWING PUBLICATIONS

PUB. NO.	OLD REV.	NEW REV.	TITLE
29-494	R04	R07	Power Conditioner Maintenance Manual

This revision includes changes reflecting:

ECNs 3687, 3572, 3597

SCNs

Briefly, the changes are as follows:

This Package Consists Of:

This Instruction Sheet

New Title Sheet

Page Revision Status Sheet

Sheet iii/iv, 1-1, 1-2, 2-1, 2-2, 2-3, 2-4

Delete 34-028D08

Delete 34-028D03

35-615R07E03 Sheet 1 of 1

34-030R02D08 Sheets 1, 2, 3

34-030R02D03 Sheet 1, 2

Publication Number 29-494R07

POWER CONDITIONER

MAINTENANCE MANUAL

PERKIN-ELMER

Interdata Division
2 Crescent Place
Oceanport, N.J. 07757

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PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-494

TITLE Power Conditioner Maintenance Manual

REVISION R07 DATE June 1978

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
i/ii	R03	3/77						
iii/iv	R07	6/78						
1-1	R07	6/78						
1-2	R07	6/78						
1-3/ 1-4	R00	5/76						
2-1	R07	6/78						
2-2	R07	6/78						
2-3	R07	6/78						
2-4	R00	5/76						
I-1	R03	3/77						

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Battery Option PC Board Assembly, 35-614R02C03
VDE Schematic, 34-030R02D08
VDE Assembly, 34-030R02D03

CHAPTER 1
POWER CONDITIONER INSTALLATION

1.1 INTRODUCTION

INTERDATA computer systems feature a highly modular structure allowing exact configurations to suit user needs. The Semi-Memory Power Conditioner (34-030) supports the 6/16 Processor with MOS Memory rather than Core Memory. In expansion systems where both MOS and Core Memories are used, the Semi-Memory Power Conditioner can be used in conjunction with older version power conditioners (34-017, 34-020, 34-026) used for Core Memories, to satisfy user requirements. The Semi-Memory Power Conditioner also features an option consisting of an internal Battery and Charger Board that can sustain the system's power requirement for a 1.5 hour period if the Power Conditioner source voltage drops below a specified level. Provision has also been made for the user to connect his own back-up power source through the Power Conditioner rear panel. This chapter provides the user with installation information for the 34-030 Power Conditioner installed in a standard INTERDATA cabinet.

1.2 POWER CONDITIONER MOUNTING

The Power Conditioner unit is placed in the upper three card slots of a standard INTERDATA System Chassis (refer to Figure 1-1) and is attached to the chassis with four screws (two in the front and two in the rear). The unit is properly installed in the chassis if the ac connector is mated with the FAN AC receptacle located at the left side of the Power Conditioner's front panel. Refer to the Semi-Memory Power Conditioner Assembly Drawing (34-030D03) for views of the front panel.

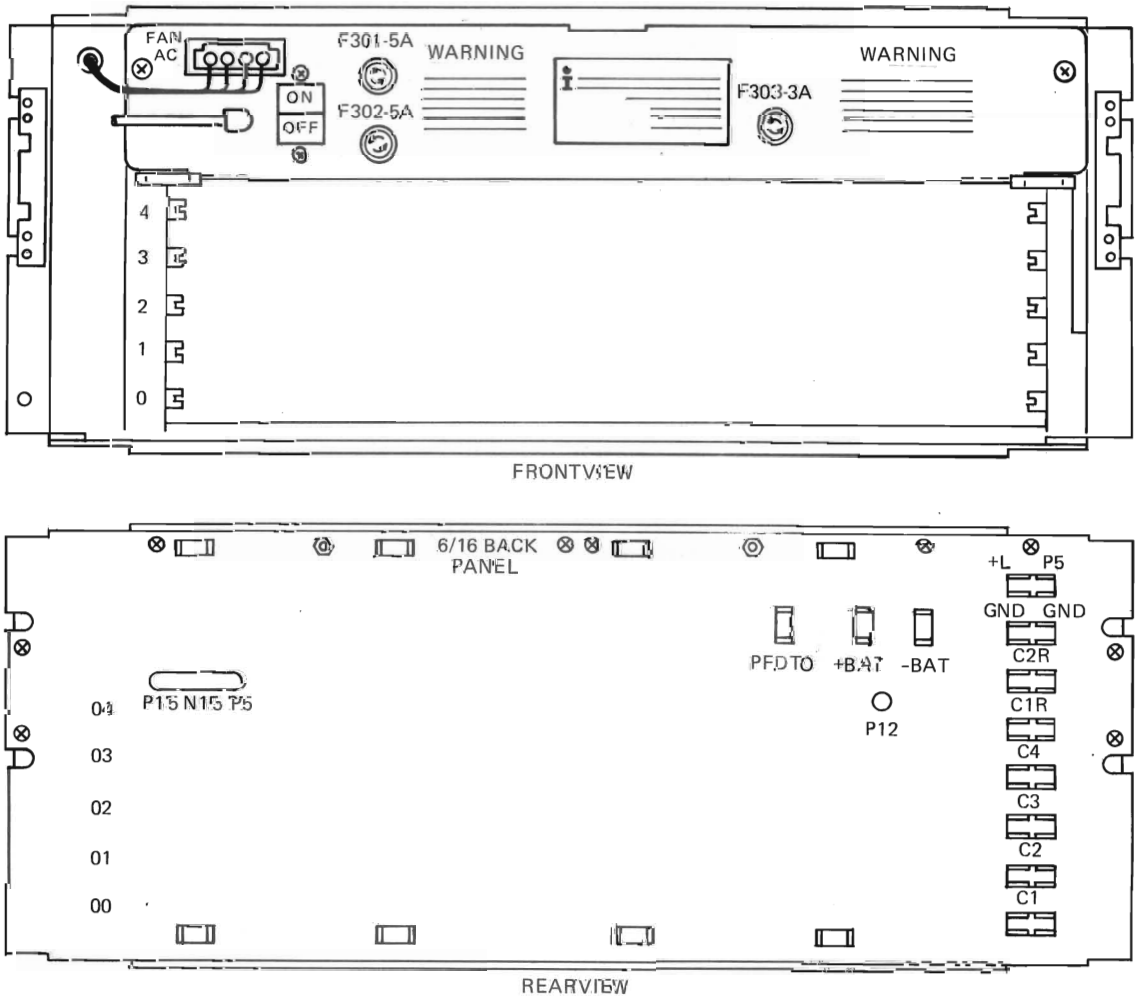

Figure 1-1. Views of Installed Power Conditioner Unit

1.3 BATTERY OPTION

This option consists of an 18 volt battery with a trickle charger mounted on a board for easy installation into the Power Conditioner unit. Five screws are provided for mounting the board and for establishing electrical contact. The charger is set for 21.0 volts (slightly above the battery voltage under load conditions) at the factory. A current limiting of 200 ma is characteristic of the battery charger. This board can be checked independently from the other portions of the Power Conditioner.

1.4 PRIMARY POWER

Primary power supplied to the Power Conditioner can be either 115 Vac or 230 Vac ±10%, 47 to 63 Hz, depending on the available power at the installation. The unit is strapped at the factory for either 115 or 230 volt operation. Only if 230 volt operation is specified by the user in his purchase order will the unit be strapped for 230 volt operation. The user can, however, convert the Power Conditioner from 115 to 230 volt operation by performing the following procedure:

1. Remove the unit from the chassis exposing terminal board TB301 (Refer to drawing 34-028D03 for the location of TB301.)

2. Verify that TB301 terminals are strapped for 115 Vac operation:

   1 to 2
   3 to 4
   5 to 6

3. Remove all straps from TB301.

4. For 230 volt operation, strap terminals 2 and 3 of TB301.

5. Place the unit back into the chassis.

6. Label the Power Conditioner "Connected for 230 Vac Operation."

7. Change the 5 Amp fuse to 3A.
   Change the 3 Amp fuse to 2A.

WARNING

PLACE THE ON/OFF SWITCH (S301) TO THE OFF POSITION PRIOR TO REMOVING THE UNIT FROM THE CHASSIS TO DISCONNECT THE INTERNAL BATTERY (OPTIONAL) AND TO REMOVE THE LINE VOLTAGE (EITHER 115 OR 230) AT TB301 AND AT THE PRIMARY SIDE OF TRANSFORMER T301 (PINS 1-4). FAILURE TO DISCONNECT THE INTERNAL BATTERY WITH THE ON/OFF SWITCH CAUSES THE BATTERY TO DRAIN. THIS IS ESPECIALLY IMPORTANT FOR TURNKEY CONSOLE OPERATION WHERE THE OPERATOR MAY TURN THE CONSOLE OFF, BUT LEAVE THE POWER CONDITIONER ON.

1.5 POWER CONDITIONER EXPANSION

If more than one 34-030 Power Conditioner units are used at an installation, the C4 contacts located at the rear panel, must be strapped together to insure proper power turn on. For expansion involving the use of 34-017, 34-020, or 34-026 units, strapping at the rear panel is accomplished differently. Refer to Figures 1-2 and 1-3 for strapping requirements.

CHAPTER 2
POWER CONDITIONER MAINTENANCE

2.1 INTRODUCTION

This chapter provides maintenance information for the INTERDATA Semi-Memory Power Conditioner (34-030). Included is a listing of general specifications, theory of operation, and procedures for performing voltage checks and adjustments. The following drawings are included in this manual for convenient reference:

Functional Schematic	Chassis Assembly	Component Locator
34-030D08	34-030D03	35-615E03 (High Voltage Board) 35-614C03 (Battery Option Board)

2.2 GENERAL SPECIFICATIONS

Input

115 or 230 Vac ± 10%, 50 or 60 Hz

Outputs

P5	+ 5.0 Vdc	25.0 Amperes
P12	+ 12.0 Vdc	2.0 Amperes

Regulation

Mnemonic	
P5	<160mv (No Load to Full Load)
P12	<160mv (No Load to Full Load)

Ripple and Noise (Maximum peak to peak)

Mnemonic	
P5	<70mv
P12	<30mv

Ambient Temperature Range

Operating	0°C TO 50°C
Storage	-40°C TO +70°C

Output Current Limiting

Mnemonic	Max Short Circuit Output Current
P5	<34 AMPS
P12	<1.0 AMPS

2.3 THEORY OF OPERATION

This section describes the operation of the 34-030 Power Conditioner. First, a general overview is presented in the section entitled Block Diagram Description. Second, the block diagram of Figure 2-1 is explained in greater detail in the section entitled Circuit Description.

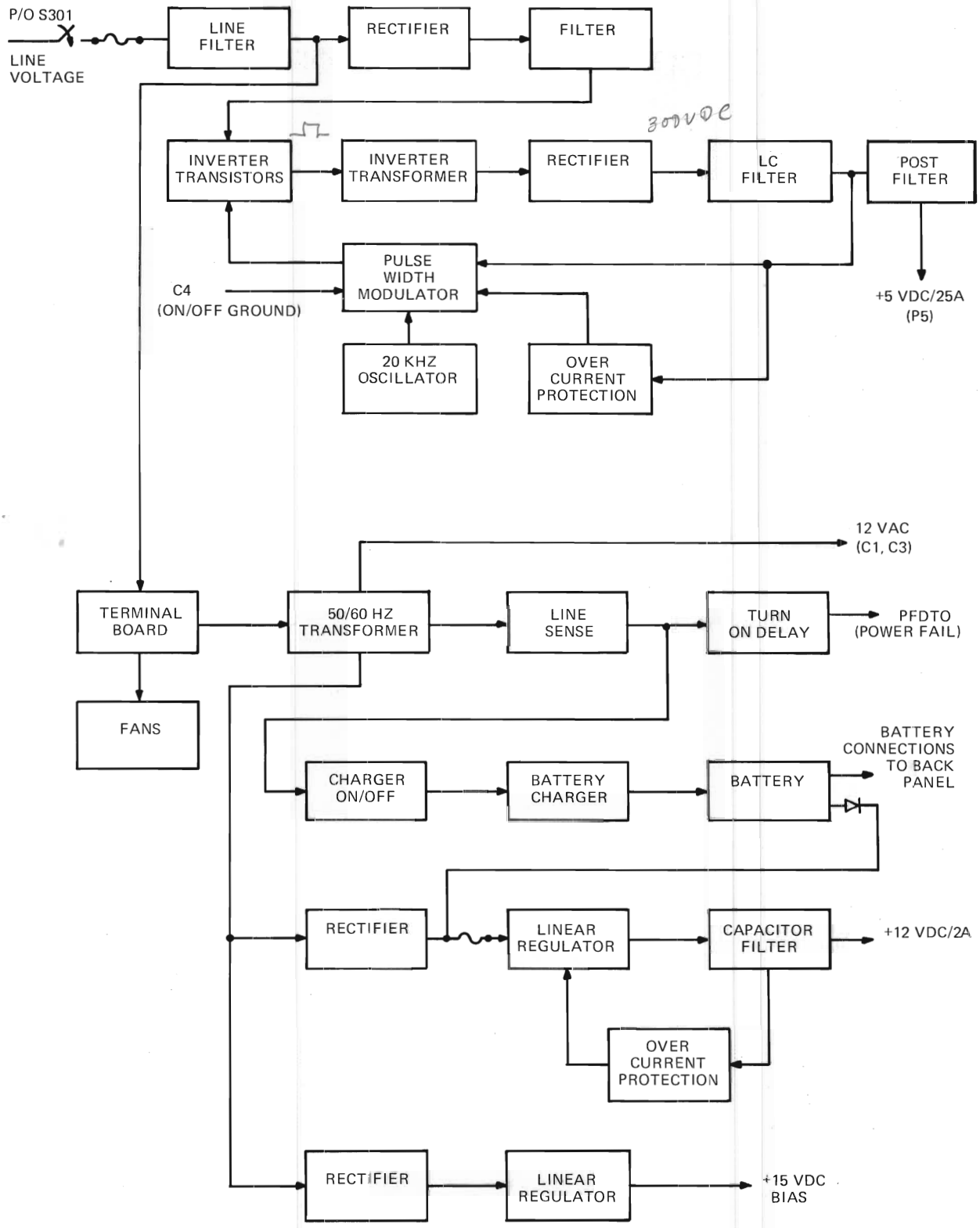

Figure 2-1. Power Conditioner Block Diagram

2.3.1 Block Diagram Description

With the line switch (S301) placed in the ON position, the Display Panel LOCK-ON-OFF switch controls the +5 volt output (P5) of the Power Conditioner. With the Display switch to the OFF position, P5 is not active, but the +12 volt output (P12) remains active to maintain information stored in the memory. The rectifier and filter (capacitor bank) produce 300 Vdc from the ac line. This dc voltage is first converted into a 20 kHz square wave by the pulse width modulator, 20 kHz oscillator, and inverter transistors, and then applied to the primary side of the inverter transformer. The voltage is stepped down to an appropriate level for the P5 output. Next, full wave rectification occurs and the signal is applied to the LC filter for smoothing. The pulse width modulator senses the +5 volt output to regulate P5 by controlling the 20 kHz square wave duty cycle. The +12 volt circuit receives its input voltage from the 50/60 Hz transformer. This ac voltage is rectified and applied to a linear (pass) regulator and capacitor filter to produce P12. Both P12 and 12 Vac output produced by the 50/60 Hz transformer are independent of the Display Panel switch. The 50/60 Hz transformer also energizes the +15 Vdc bias supply to energize the Power Conditioner's control circuits.

2.3.2 Circuit Description

The following sections describe in greater detail the major functional elements of the Power Conditioner. The reader, when referring to the functional schematic 34-030D08, should observe the following convention to locate a circuit area or component being described in the text. In the three digit coordinate given in parentheses, for example, (1H2), the first digit (1) refers to sheet 1 and the next two digits (H2) refer to the coordinates of the circuit component, transformer T101 in this case.

2.3.2.1 Rectifier And Filter (115 Vac Connection)

If the unit is connected for 115 Vac line operation, the rectifier is connected as a doubler, producing 300 Vdc. The filter capacitors charge through the series resistors R301 (1D1) and R302 (1D2) limiting the turn-on current and preventing turn-on surges from causing equipment malfunction.

2.3.2.2 Rectifier And Filter (230 Vac Connection)

If the unit is connected for 230 Vac operation, a bridge rectifier is used rather than the doubler for 115 Vac operation. However, in both cases, the rectifier output is approximately 300 Vdc. Removing the strap at TB301 pin 1 and pin 2 (2A4), converts the rectifier D301 (1D1) into a bridge rectifier.

2.3.2.3 Inverter Transistors And Inverter Transformer

Two high voltage transistors Q103 and Q105 (1H3) switch the rectified line (300Vdc) through the inverter transformer T102 (1J1) at a 20 kHz rate. Capacitors C110 and C111 (1G1) divide the 300 Vdc into two 150 volt sources. Transistor Q103 switches the upper 150 volt source and transistor Q105 switches the lower source. Base drive to Q103 and Q105 is supplied from T101 (1H2). Integrated circuit A104 (1G4) controls the base drive to the high voltage transistors.

Other secondaries on T101 (pins 4, 5 and 8, 9) supply additional drive power to the high voltage transistor bases. As current through these windings increases due to increasing load requirements, additional drive power becomes available. Turn off drive is provided by both Q117, D105 (1F3) and Q114, D107 (1F3) circuit components.

2.3.2.4 5 Volt Rectifier And Filter

Schottky rectifiers D101 and D102 (1K1) rectify up to 25 amperes of P5 output current. Pulsating dc is filtered through inductor L102 (1K2) and capacitor C108 (1L1). Output current flowing through resistor R104 (1K2) provides a current sensing signal for the P5 overcurrent circuit.

2.3.2.5 Pulse Width Modulator Circuit

The pulse width modulator circuit monitors the P5 output voltage and modulates the duty cycle of the high voltage transistors to maintain P5 at +5 volts in line with load variations. The P5 output current is also monitored and controlled to prevent overloading the unit. A +5 volt reference is established by integrated circuit A104 (1G4). The A104 unit compares this reference to the P5 output voltage and produces an error signal at its output, pin 10. The level of this signal is compared to the sawtooth riding on a dc level generated at the base of Q132 (1D4). The on time of Q131 (1E4) and Q115 (1E2) is varied to control the on time of the high voltage transistors.

2.3.2.6 +12 Volt Regulator

Zener diode D103 (2E4) provides a reference for dual transistor Q108 (1H3) which acts as a differential amplifier. The output voltage is fed back through R107 (2J2) and R115 (2J4). The amplified error signal appears at pin 7 of Q108 and controls the conduction of Q107 and Q106 that act as drivers for pass transistors Q104 and Q101 (2G2). Resistor R120 (2F2) monitors output current for overload protection.

2.3.2.7 +15 Volt Bias Supply

Integrated circuit A101 (2E7) forms a +5 volt reference. The A101 unit compares the output voltage to the reference and the amplified error signal appears at pin 10 to control pass transistor Q102 (2E6). The current is monitored through R128 (2F6) for overload protection.

2.3.2.8 Line Sense Circuit

The ac line is monitored by a winding from T301, pins 5, 6 and 7 (1A6). The output appears at D109 (1H7) and is high when the ac line is too low for operation. This signal holds the inverter transistors in the off mode resulting in no P5 output. This circuit does not control the P12 output or the unregulated ac output across C1 through C3.

2.3.2.9 KEY CONTROL (C4)

This signal from the Display Panel is received by the Power Conditioner (1B5) and only controls the P5 output. When a low (short to ground) is received, the P5 output is enabled.

2.3.2.10 POWER FAIL (PFDTO)

The power fail circuit receives its input signal at the anode of D110 (1J7). Its signal is from the line sense circuit or the key control function. Upon receiving a high, the PFDTO output is low indicating either a fault in the ac power or an OFF command from the Display Panel key. When a low is received, P5 is allowed to rise, and at least 1.5 seconds later, PFDTO will change state to a high. When an OFF command is received, PFDTO will drop to a low, and at a minimum of 3ms later, P5 will go out of regulation.

2.3.2.11 Battery Option

The battery option includes the following: a battery, battery charger, and a charger ON/OFF. The battery supports the P12 output in the event of ac power failure and is capable of maintaining the P12 output in regulation for a minimum of 1.5 hours.

2.4 VOLTAGE CHECKS AND ADJUSTMENTS

Although the Power Conditioner voltages are adjusted at the factory, the user should verify all voltages prior to connecting the unit to the system. Some voltage checks and adjustments require the Power Conditioner tray to be pulled out, while others can be performed with the tray in. Refer to the high voltage board assembly drawing (35-615E03) and the battery option board assembly drawing (35-614C03) for the location of components and adjustments. Steps 4 through 6 in the following procedure are optional with the battery charger board.

1. Pull out tray to expose the high voltage board components.
2. Measure the dc voltage across the capacitor C115.
3. If necessary, adjust potentiometer R132 for a 15±.05 Vdc reading.
4. Disconnect the battery cables from J3 and J5.
5. Measure the voltage across J3 and J5.
6. If necessary, adjust potentiometer R415 at the battery charger board for a reading of 21.0 Vdc and connect the battery cables to J3 and J5.
7. Push the tray in.
8. At the rear panel, measure the dc voltage across one of the gold pins 28, 29 or 30 of slot 5 and the GND faston.
9. Adjust P12 for a +12±.05 Vdc reading.
10. Measure the voltage across the P5 faston and the GND faston.
11. Adjust potentiometer P5 for a +5±.05 Vdc reading.

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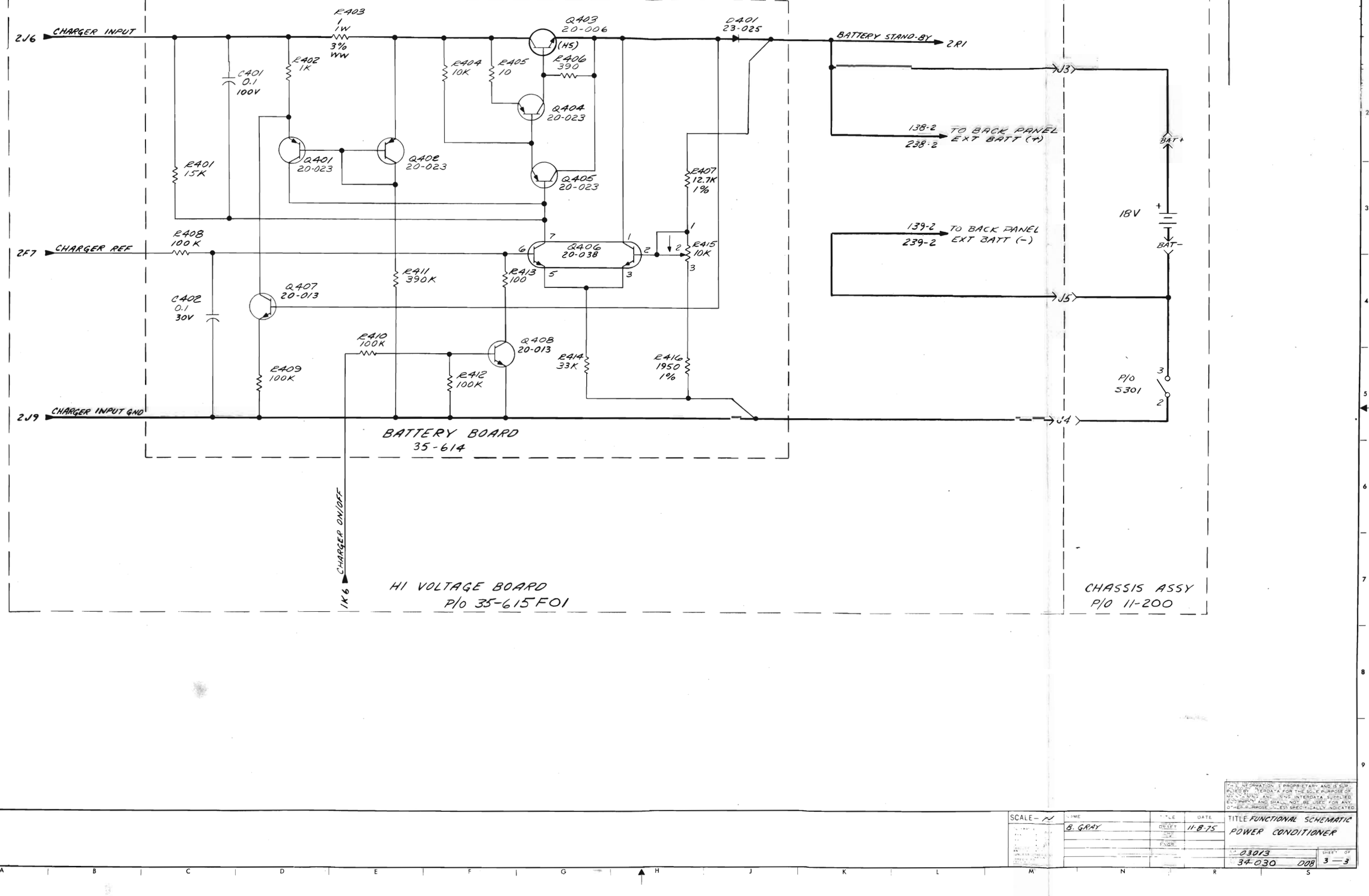

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03013
34-030 008
SHEET OF 3 — 3

DRAWING 44-231 24538

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PRE PRODUCTION APPROVAL	DEV CRL	INIT DATE 7-13-76

AREA F3 & F4 : Q118 & Q116 WERE SPEC'D AS 20-027. P.C. BRD 35-615F01 WAS R00.

WTA	JJ	3687	5-31-78	R01

AREA H1: C110 & C111 WERE SPEC'D AS 15 200V. AREA H2: T101 WAS SPEC'D AS 30-049F01. AREA F2: D134, 23-025 WAS NOT SPEC'D. AREA J1 & J3: D135 & D136 (23-017) WERE NOT SPEC'D. AREA H2 & H3 DELETED R196 FROM EMITTER Q103. ADDED R203 13.3 TO BASE Q103. DELETED R197 FROM EMITTER, Q105. ADDED R209, 13.3 TO BASE, Q105 AREA G3: CONNECTED ANODE OF D107 & D105 TO GND. AREA C5 D137, 23-034 & D138 23-036 WERE NOT SPEC'D. AREA D5: R184 WAS SPEC'D AS 68K. AREA E5 COLLECTOR OF Q129 WAS CONNECTED TO COLLECTOR of Q128 P.C. Brd. 35-615F01 WAS R06. REVISE SHT. 2.

WTA	JJ	3572	6-13-78	R02

most Recent

COMPONENT NUMBERING	
101-299	HI VOLTAGE BOARD
301-399	CHASSIS
401-499	BATTERY OPTION BD

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL :

35-614R01	BATTERY OPTION
35-615F01 R07	HI VOLTAGE

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   :ALL CAPACITORS ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE PART OF 35-615F01.
3. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

SCALE — NONE

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J. CONWAY	DRAFT	7-8-76
R.F. CERO	CHK	9-9-76
E. CENTOFANTI	ENGR	
B. MULLER	SYS TEST	
S. MESSINA	MGR	

TITLE FUNCTIONAL SCHEMATIC POWER CONDITIONER

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AREA M5 : 12VAC/50MA WAS SPEC'D AS 5VAC/50MA.			
WTA	3572	6-13-78	R01

T301 P/O 30-051

F303 4A

D302 23-023

D118 23-025 — BATTERY STAND-BY 3L1

D104 23-034

R111 3.3K

R110 0.1, 5W WW

Q104(NS) 20-006

(HS) 20-006

R108 0.1 5W WW

R120 0.2 5W WW

R123 47K

R122 15K

R121 1K 1%

R118 10K 1%

R119 10

Q101

R112 390

Q106 20-023

Q111 20-023

Q110 20-023

Q107 20-023

P12/2A — 128-2-130-2, 228-2-230-2

R107 6.99K 1%

C102 150 16V

C104 150 16V

C106 150 16V

C138 4800 50V

D121 23-034

Q109 20-013

R101 10K

Q108 20-034

D103 23-040 MOD2 6.2V 5%

R116 20K 1%

C112 2.2 20V

R117 200K

R115 10K 1%

R114 23.7K 1%

R113 4.99K 1%

C101 150 16V

C103 150 16V

C105 150 16V

P12 GND IC6

P12 GND IE4

P12 GND

P5 GND J8

115V 230V

TB301

B 112 A 111

J301 P301

B301 B302

D 122

P1 J2 P1 J1

R188 68 2W

SEE NOTE 1

R187 68 2W

C3 141-2

12 VAC / 50 MA

C1 240-2

P1 12 P1 J1 5 3

D106 23-046

CHARGER INPUT 3A1

Q102 20-006 (HS)

R128 2 1W WW

P15 BIAS

R127 390

R129 10K 1%

D132 23-025

C113 1000 75V

NC 09 V_{CC} V_E 11 12 02 03 V_4 COR. COR. LIM. SENSE

NC 01 10 V_{OUT} INV IN 04

NC 08 R101 19-094 V_{REF} 06 CHARGER REF 3A4

NC 14 NON INV IN 05 R132 10K

COMP V_- 13 07

C114 0.1 30V

R130 10K 1%

R131 4.99K 1%

C115 100 50V

P15 AUX — 1F2, 1G6

C145 100 25V

C146 100 25V

P5 GND P5

CHARGER INPUT GND 3A5

CHASSIS ASSY P/O 11-200

HI VOLTAGE BOARD P/O 35-615F01

NOTES:
1. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

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SCALE – ~

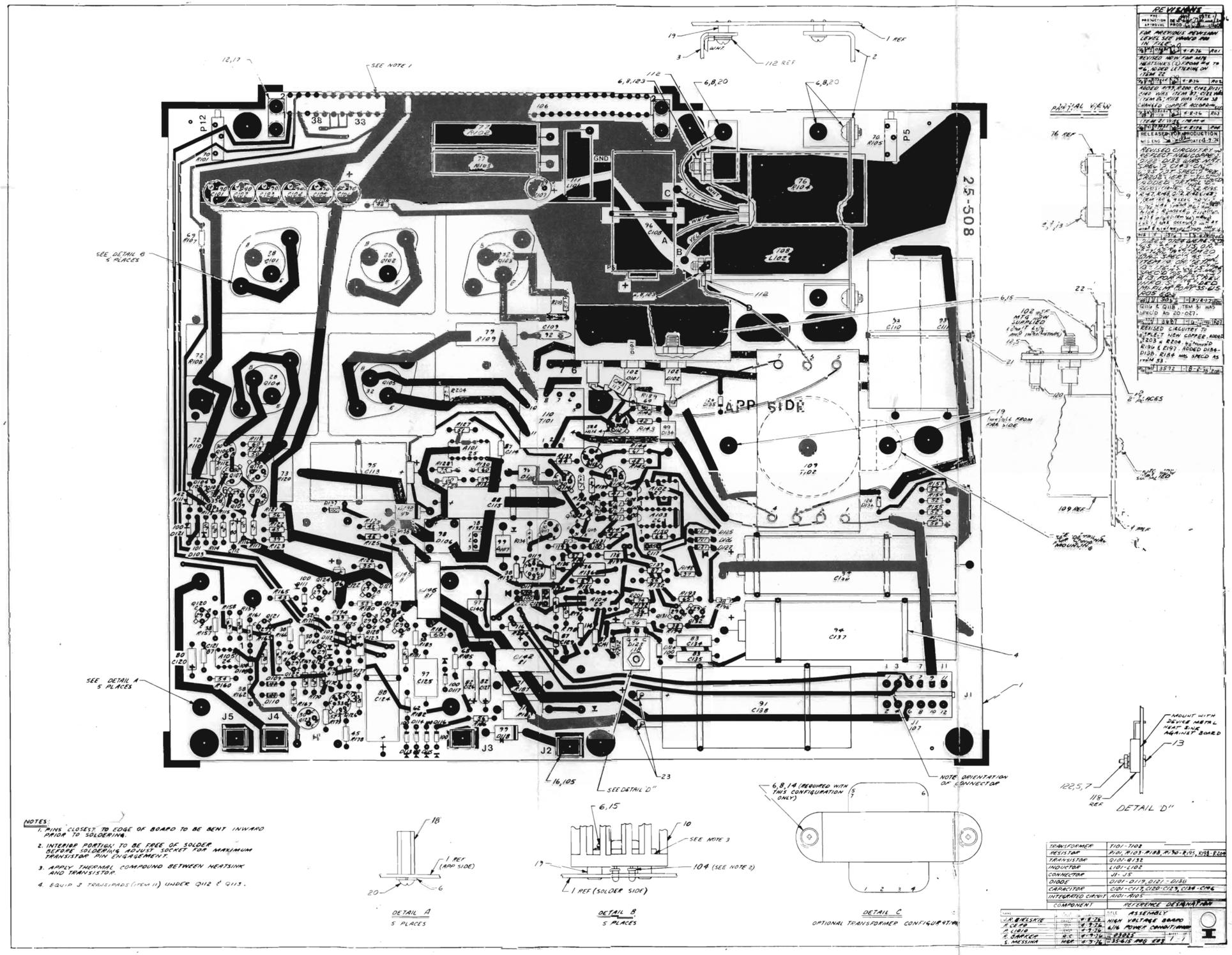
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J. CONWAY	DRAFT	7-8-76
	CHK	
	ENGR	

TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

TASK NO. 03013 — SHEET OF 2 — 3

DWG NO. 34-030 R01 D08



NOTES:

1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
2. INTERIOR PORTIONS TO BE FREE OF SOLDER BEFORE SOLDERING ADJUST SOCKET FOR MAXIMUM TRANSISTOR PIN ENGAGEMENT.
3. APPLY THERMAL COMPOUND BETWEEN HEATSINK AND TRANSISTOR.
4. EQUIP J3 TRANSPADS (ITEM 11) UNDER Q112 & Q113.

TRANSFORMER	T101-T102
RESISTOR	R101, R103-R188, R190-R195, R198-R204
TRANSISTOR	Q101-Q132
INDUCTOR	L101-L102
CONNECTOR	J1-J5
DIODE	D101-D119, D121-D130
CAPACITOR	C101-C117, C120-C123, C126-C146
INTEGRATED CIRCUIT	A101-A105
COMPONENT	REFERENCE DESIGNATION

J.R. BIELSKIE		8-9-76	TITLE ASSEMBLY
A. DE LEO		8-9-76	HIGH VOLTAGE BOARD
R. BARKER	R.C.	8-9-76	4/16 POWER CONDITIONER
S. MESSINA	MGR.	8-9-76	23223
			35-615 AND 693

Publication Number 29-494

POWER CONDITIONER MAINTENANCE MANUAL

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INTERDATA®

Subsidiary of PERKIN-ELMER
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Printed in U.S.A.
May 1976

PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-494

TITLE Power Conditioner Maintenance Manual

REVISION R00 DATE May, 1976

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
i/ii	R00	5/76						
1-1	R00	5/76						
1-2	R00	5/76						
1-3/								
1-4	R00	5/76						
2-1	R00	5/76						
2-2	R00	5/76						
2-3	R00	5/76						
2-4	R00	5/76						

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Schematic, 34-028D08R02
Chassis Assembly, 34-028D03R01
Chassis Assembly, Battery Option, 02-423C03
High Voltage PC Board Assembly, 35-615E03R04
Battery Option PC Board Assembly, 35-614C03R02

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CHAPTER 1
POWER CONDITIONER INSTALLATION

1.1 INTRODUCTION

INTERDATA computer systems feature a highly modular structure allowing exact configurations to suit user needs. The Semi-Memory Power Conditioner (34-028) supports the 6/16 Processor with MOS Memory rather than Core Memory. In expansion systems where both MOS and Core Memories are used, the Semi-Memory Power Conditioner can be used in conjunction with older version power conditioners (34-017, 34-020, 34-026) used for Core Memories, to satisfy user requirements. The Semi-Memory Power Conditioner also features an option consisting of an internal Battery and Charger Board that can sustain the system's power requirement for a 1.5 hour period if the Power Conditioner source voltage drops below a specified level. Provision has also been made for the user to connect his own back-up power source through the Power Conditioner rear panel. This chapter provides the user with installation information for the 34-028 Power Conditioner installed in a standard INTERDATA cabinet.

1.2 POWER CONDITIONER MOUNTING

The Power Conditioner unit is placed in the upper three card slots of a standard INTERDATA System Chassis (refer to Figure 1-1) and is attached to the chassis with four screws (two in the front and two in the rear). The unit is properly installed in the chassis if the ac connector is mated with the FAN AC receptacle located at the left side of the Power Conditioner's front panel. Refer to the Semi-Memory Power Conditioner Assembly Drawing (34-028D03) for views of the front panel.

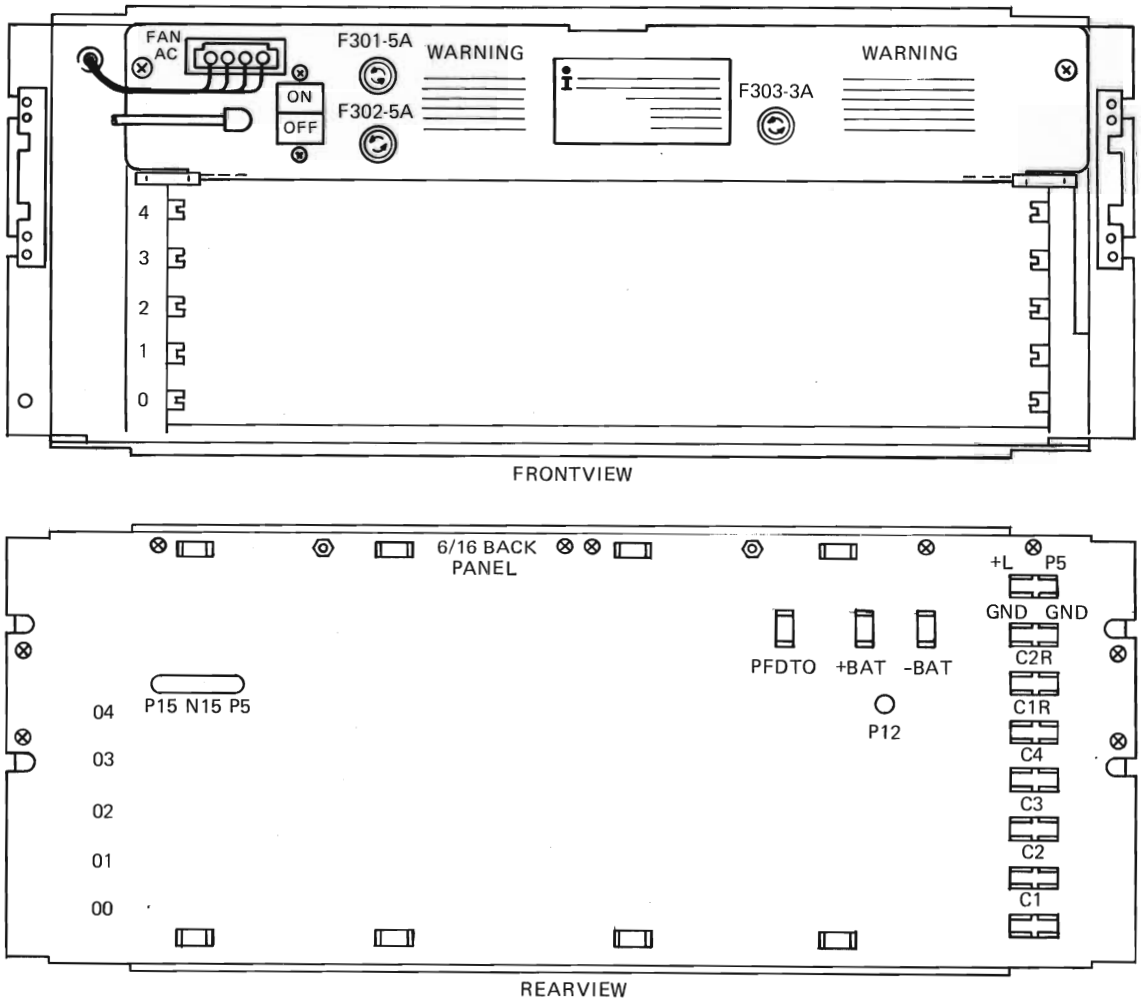

Figure 1-1. Views of Installed Power Conditioner Unit

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1.3 BATTERY OPTION

This option consists of an 18 volt battery with a trickle charger mounted on a board for easy installation into the Power Conditioner unit. Five screws are provided for mounting the board and for establishing electrical contact. The charger is set for 21.0 volts (slightly above the battery voltage under load conditions) at the factory. A current limiting of 200 ma is characteristic of the battery charger. This board can be checked independently from the other portions of the Power Conditioner.

1.4 PRIMARY POWER

Primary power supplied to the Power Conditioner can be either 115 Vac or 230 Vac ±10%, 47 to 63 Hz, depending on the available power at the installation. The unit is strapped at the factory for either 115 or 230 volt operation. Only if 230 volt operation is specified by the user in his purchase order will the unit be strapped for 230 volt operation. The user can, however, convert the Power Conditioner from 115 to 230 volt operation by performing the following procedure:

1. Remove the unit from the chassis exposing terminal board TB301 (Refer to drawing 34-028D03 for the location of TB301.)

2. Verify that TB301 terminals are strapped for 115 Vac operation:

   1 to 2
   3 to 4
   5 to 6

3. Remove all straps from TB301.

4. For 230 volt operation, strap terminals 2 and 3 of TB301.

5. Place the unit back into the chassis.

6. Label the Power Conditioner "Connected for 230 Vac Operation."

WARNING

PLACE THE ON/OFF SWITCH (S301) TO THE OFF POSITION PRIOR TO REMOVING THE UNIT FROM THE CHASSIS TO DISCONNECT THE INTERNAL BATTERY (OPTIONAL) AND TO REMOVE THE LINE VOLTAGE (EITHER 115 OR 230) AT TB301 AND AT THE PRIMARY SIDE OF TRANSFORMER T301 (PINS 1-4). FAILURE TO DISCONNECT THE INTERNAL BATTERY WITH THE ON/OFF SWITCH CAUSES THE BATTERY TO DRAIN. THIS IS ESPECIALLY IMPORTANT FOR TURNKEY CONSOLE OPERATION WHERE THE OPERATOR MAY TURN THE CONSOLE OFF, BUT LEAVE THE POWER CONDITIONER ON.

1.5 POWER CONDITIONER EXPANSION

If more than one 34-028 Power Conditioner units are used at an installation, the C4 contacts located at the rear panel, must be strapped together to insure proper power turn on. For expansion involving the use of 34-017, 34-020, or 34-026 units, strapping at the rear panel is accomplished differently. Refer to Figures 1-2 and 1-3 for strapping requirements.

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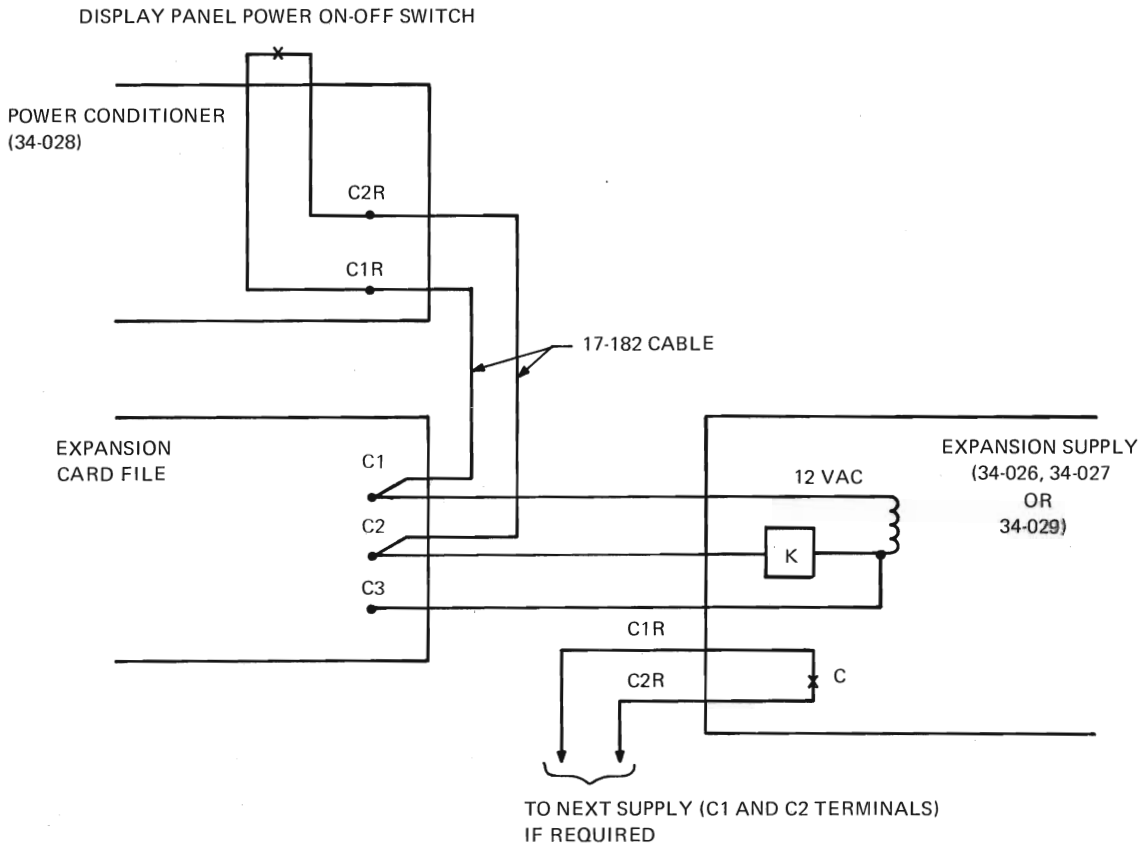

Figure 1-2. Expansion System Involving 34-026, 34-027, and 34-029 Units

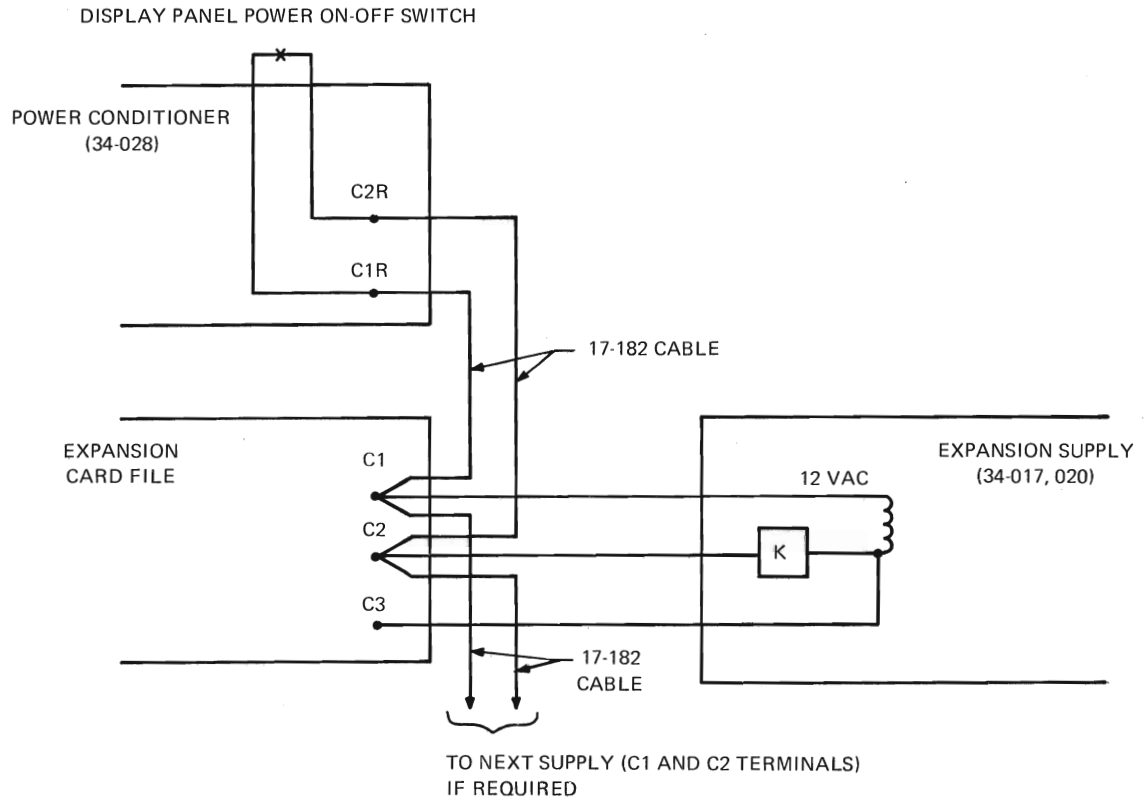

Figure 1-3. Expansion System Involving 34-017 and 34-020 Units

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CHAPTER 2
POWER CONDITIONER MAINTENANCE

2.1 INTRODUCTION

This chapter provides maintenance information for the INTERDATA Semi-Memory Power Conditioner (34-028). Included is a listing of general specifications, theory of operation, and procedures for performing voltage checks and adjustments. The following drawings are included in this manual for convenient reference:

Functional Schematic	Chassis Assembly	Component Locator
34-028D08	34-028D03	35-615E03 (High Voltage Board) 35-614C03 (Battery Option Board)

2.2 GENERAL SPECIFICATIONS

Input

115 or 230 Vac ± 10%, 50 or 60 Hz

Outputs

P5	+ 5.0 Vdc	25.0 Amperes
P12	+ 12.0 Vdc	2.0 Amperes

Regulation

Mnemonic	
P5	<160mv (No Load to Full Load)
P12	<160mv (No Load to Full Load)

Ripple and Noise (Maximum peak to peak)

Mnemonic	
P5	<70mv
P12	<30mv

Ambient Temperature Range

Operating	0°C TO 50°C
Storage	-40°C TO +70°C

Output Current Limiting

Mnemonic	Max Short Circuit Output Current
P5	<34 AMPS
P12	<1.0 AMPS

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2.3 THEORY OF OPERATION

This section describes the operation of the 34-028 Power Conditioner. First, a general overview is presented in the section entitled Block Diagram Description. Second, the block diagram of Figure 2-1 is explained in greater detail in the section entitled Circuit Description.

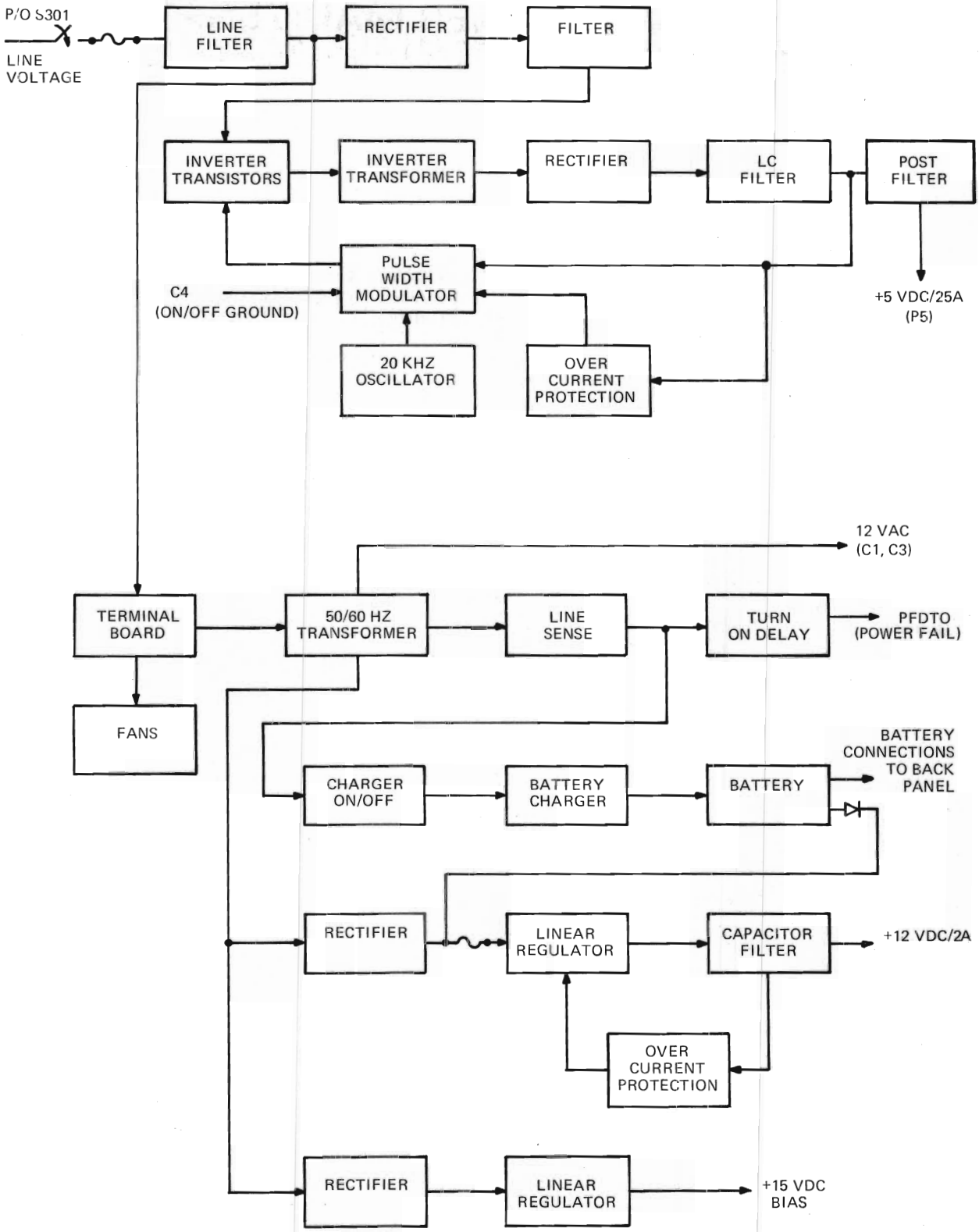

Figure 2-1. Power Conditioner Block Diagram

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2.3.1 Block Diagram Description

With the line switch (S301) placed in the ON position, the Display Panel LOCK-ON-OFF switch controls the +5 volt output (P5) of the Power Conditioner. With the Display switch to the OFF position, P5 is not active, but the +12 volt output (P12) remains active to maintain information stored in the memory. The rectifier and filter (capacitor bank) produce 300 Vdc from the ac line. This dc voltage is first converted into a 20 kHz square wave by the pulse width modulator, 20 kHz oscillator, and inverter transistors, and then applied to the primary side of the inverter transformer. The voltage is stepped down to an appropriate level for the P5 output. Next, full wave rectification occurs and the signal is applied to the LC filter for smoothing. The pulse width modulator senses the +5 volt output to regulate P5 by controlling the 20 kHz square wave duty cycle. The +12 volt circuit receives its input voltage from the 50/60 Hz transformer. This ac voltage is rectified and applied to a linear (pass) regulator and capacitor filter to produce P12. Both P12 and 5 Vac output produced by the 50/60 Hz transformer are independent of the Display Panel switch. The 50/60 Hz transformer also energizes the +15 Vdc bias supply to energize the Power Conditioner's control circuits.

2.3.2 Circuit Description

The following sections describe in greater detail the major functional elements of the Power Conditioner. The reader, when referring to the functional schematic 34-028D08, should observe the following convention to locate a circuit area or component being described in the text. In the three digit coordinate given in parentheses, for example, (1H2), the first digit (1) refers to sheet 1 and the next two digits (H2) refer to the coordinates of the circuit component, transformer T101 in this case.

2.3.2.1 Rectifier And Filter (115 Vac Connection)

If the unit is connected for 115 Vac line operation, the rectifier is connected as a doubler, producing 300 Vdc. The filter capacitors charge through the series resistors R301 (1D1) and R302 (1D2) limiting the turn-on current and preventing turn-on surges from causing equipment malfunction.

2.3.2.2 Rectifier And Filter (230 Vac Connection)

If the unit is connected for 230 Vac operation, a bridge rectifier is used rather than the doubler for 115 Vac operation. However, in both cases, the rectifier output is approximately 300 Vdc. Removing the strap at TB301 pin 1 and pin 2 (2A4), converts the rectifier D301 (1D1) into a bridge rectifier.

2.3.2.3 Inverter Transistors And Inverter Transformer

Two high voltage transistors Q103 and Q105 (1H3) switch the rectified line (300Vdc) through the inverter transformer T102 (1J1) at a 20 kHz rate. Capacitors C110 and C111 (1G1) divide the 300 Vdc into two 150 volt sources. Transistor Q103 switches the upper 150 volt source and transistor Q105 switches the lower source. Base drive to Q103 and Q105 is supplied from T101 (1H2). Integrated circuit A104 (1G4) controls the base drive to the high voltage transistors.

Other secondaries on T101 (pins 4, 5 and 8, 9) supply additional drive power to the high voltage transistor bases. As current through these windings increases due to increasing load requirements, additional drive power becomes available. Turn off drive is provided by both Q117, D105 (1F3) and Q114, D107 (1F3) circuit components.

2.3.2.4 5 Volt Rectifier And Filter

Schottky rectifiers D101 and D102 (1K1) rectify up to 25 amperes of P5 output current. Pulsating dc is filtered through inductor L102 (1K2) and capacitor C108 (1L1). Output current flowing through resistor R104 (1K2) provides a current sensing signal for the P5 overcurrent circuit.

2.3.2.5 Pulse Width Modulator Circuit

The pulse width modulator circuit monitors the P5 output voltage and modulates the duty cycle of the high voltage transistors to maintain P5 at +5 volts in line with load variations. The P5 output current is also monitored and controlled to prevent overloading the unit. A +5 volt reference is established by integrated circuit A104 (1G4). The A104 unit compares this reference to the P5 output voltage and produces an error signal at its output, pin 10. The level of this signal is compared to the sawtooth riding on a dc level generated at the base of Q132 (1D4). The on time of Q131 (1E4) and Q115 (1E2) is varied to control the on time of the high voltage transistors.

2.3.2.6 +12 Volt Regulator

Zener diode D103 (2E4) provides a reference for dual transistor Q108 (1H3) which acts as a differential amplifier. The output voltage is fed back through R107 (2J2) and R115 (2J4). The amplified error signal appears at pin 7 of Q108 and controls the conduction of Q107 and Q106 that act as drivers for pass transistors Q104 and Q101 (2G2). Resistor R120 (2F2) monitors output current for overload protection.

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2.3.2.7 +15 Volt Bias Supply

Integrated circuit A101 (2E7) forms a +5 volt reference. The A101 unit compares the output voltage to the reference and the amplified error signal appears at pin 10 to control pass transistor Q102 (2E6). The current is monitored through R128 (2F6) for overload protection.

2.3.2.8 Line Sense Circuit

The ac line is monitored by a winding from T301, pins 5, 6 and 7 (1A6). The output appears at D109 (1H7) and is high when the ac line is too low for operation. This signal holds the inverter transistors in the off mode resulting in no P5 output. This circuit does not control the P12 output or the unregulated ac output across C1 through C3.

2.3.2.9 KEY CONTROL (C4)

This signal from the Display Panel is received by the Power Conditioner (1B5) and only controls the P5 output. When a low (short to ground) is received, the P5 output is enabled.

2.3.2.10 POWER FAIL (PFDTO)

The power fail circuit receives its input signal at the anode of D110 (1J7). Its signal is from the line sense circuit or the key control function. Upon receiving a high, the PFDTO output is low indicating either a fault in the ac power or an OFF command from the Display Panel key. When a low is received, P5 is allowed to rise, and at least 1.5 seconds later, PFDTO will change state to a high. When an OFF command is received, PFDTO will drop to a low, and at a minimum of 3ms later, P5 will go out of regulation.

2.3.2.11 Battery Option

The battery option includes the following: a battery, battery charger, and a charger ON/OFF. The battery supports the P12 output in the event of ac power failure and is capable of maintaining the P12 output in regulation for a minimum of 1.5 hours.

2.4 VOLTAGE CHECKS AND ADJUSTMENTS

Although the Power Conditioner voltages are adjusted at the factory, the user should verify all voltages prior to connecting the unit to the system. Some voltage checks and adjustments require the Power Conditioner tray to be pulled out, while others can be performed with the tray in. Refer to the high voltage board assembly drawing (35-615E03) and the battery option board assembly drawing (35-614C03) for the location of components and adjustments. Steps 4 through 6 in the following procedure are optional with the battery charger board.

1. Pull out tray to expose the high voltage board components.
2. Measure the dc voltage across the capacitor C115.
3. If necessary, adjust potentiometer R132 for a 15±.05 Vdc reading.
4. Disconnect the battery cables from J3 and J5.
5. Measure the voltage across J3 and J5.
6. If necessary, adjust potentiometer R415 at the battery charger board for a reading of 21.0 Vdc and connect the battery cables to J3 and J5.
7. Push the tray in.
8. At the rear panel, measure the dc voltage across one of the gold pins 28, 29 or 30 of slot 5 and the GND faston.
9. Adjust P12 for a +12±.05 Vdc reading.
10. Measure the voltage across the P5 faston and the GND faston.
11. Adjust potentiometer P5 for a +5±.05 Vdc reading.

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INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
PRE PRODUCTION APPROVAL	DEV	DATE	
REVISED SHEETS 1, 2, & 3 FOR PREVIOUS REVISION SEE R00 MICROFILM IN FILE. AREA K9, 35-614 WAS R00 & 35-615 WAS R02			
JRB	030258	3-19-76	R01
REVISED SHEETS 1 & 2 AREA K9, 35-615 WAS R04 AREAS F1, B7 DIODES SHOWN DOTTED WERE NOT SPEC'D. ADDED NOTE 3. AREA D5: C122 WAS 4.7/50V; AREA B5, CR40 WAS 0.1/30V & WAS CONNECTED TO R140; AREA A6, ADDED R199; AREA F4, ADDED R200 & CR42; AREA J6, CHARGER ON/OFF WAS WAS CONNECTED TO Q109 CATH.			
JRB	030258	3-30-76	R02
RELEASED FOR PRODUCTION			
ENG		DATE	4/9/76

P/O 5301 F301 5A F302 5A 24-069 L301 D301 23-023 R301 1.0 25W R302 1.0 25W P/O 11-186 P15 BIAS

SEE NOTE 3 C136 475 200V C137 475 200V R156 100K R155 100K R154 100K R153 100K C110 15 200V C111 15 200V

30-048 T102 D101 23-042 D102 23-042 L102 40μH 30-023 R104 21-075 .006 WHT WHT L101 30-050 3μH C107 330 6.3V C108 16500 6V

P5 +L 100-2-113-2 200-2-212-2 R103 5.0 10W 2(5Ω) in Parallel P5 GND ⊥GND 114-2-127-2 213-2-227-2

T101 30-049 C109 540 PF 1000V R196 .12,5W R197 .12,5W R103 450 N.J. 1μH MAX 5W WW 20-030 Q108 20-030 Q105

Q113 Q115 20-023 Q112 20-023 R144 100 1% R143 3.3K R145 2K R138 4.7K R139 4.7K R148 4.7K R147 4.7K R134 33 Q117 20-027 Q118 20-027 Q114 20-027 Q116 R146 22 R137 33 D107 23-025 D105 23-025 R142 6.8K

D134 D136 No Diodes

A103 19-191 A102 19-132 CLK R195 10K R150 17.2K 1% C117 330PF 2% R135 10K R133 10K R136 1% 1K,1W R194 10K C135 .0039 C134 .0039 R193 5.1K Q132 20-013 Q131 20-013 P15 BIAS P12 GND 2R4 C142 15 25V R200 100 1/2W D119 23-034 C140 0.47 150V 140-2 C4 R124 160K R125 15K R165 1.5K Q124 20-013 D111 23-034 R126 100 C122 15 25V R184 68K R183 10K R180 68K Q130 20-013 Q127 20-013 Q129 20-013 R149 6.8K R174 47K R171 100K C123 2.2 20V R191 6.8K Q128 20-013 C128 150 PF C129 0.1 30V R190 5.1K A104 19-094 Vcc V+ V2 VOUT VREF COMP CUR LIM SENSE CUR INV IN NON INV IN C141 0.1 30V R198 68 C139 0.1,30V R152 20K 1% R151 4.99K 1% R105 10K R192 1K 1% Q119 20-038 R141 13.3 1% R199 1W C116 0.1 30V R140 33

CHARGER ON/OFF 3E7

P/O 30-051 T301 D115 23-034 D113 23-034 D116 23-034 D117 23-034 D114 23-034 SEE NOTE 3 C124 100 50V R186 1K 1% R182 357K 1% R178 15K R173 100K R179 10K Q126 20-038 R176 2K 1% R175 68K C126 4.7 50V C127 4.7 50V R185 681 1% C125 0.47 150V R181 150K 1% R177 23.7K 1% R172 20K 1% R170 68K Q125 20-013 D112 23-043 F02 6.2V, 1% R168 10K Q123 20-023 R167 6.8K R169 68K R166 10K Q122 20-013 R164 3K D109 23-034 D110 23-034 R162 10K R163 10K Q121 20-013 R161 47 D108 23-034 C120 2.2 20V A105 19-085 TRIGGER OUTPUT RESET DISCHARGE THRESHOLD CONT.VOL. GND Vcc C121 0.1 30V R159 10K P15 BIAS R160 820K R158 3K R157 10K 20-013 Q120 R106 2K PROTO (POWER FAIL) 135-2 PWR FAIL GND 235-2

P/O 11-186

A103 19-191 NC NC

COMPONENT NUMBERING	
101-299	HI VOLTAGE BOARD
301-399	CHASSIS
401-499	BATTERY OPTION 8D

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-614 R01	BATTERY OPTION
35-615 R06	HI VOLTAGE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX	REV LEVEL	2	2	1
	SHT. NO.	1	2	3

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   :ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
   :ALL CAPACITORS ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE PART OF 35-615.
3. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

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SCALE— NONE

	NAME	TITLE	DATE
DRAWN	J.R. BIELSKIE	DRAFT	11-10-75
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ENG'D	P. LLOYD	ENGR	4-9-76
TEST	J. JAMES	SYS TEST	4-9-76
MFG	S. MESSINA	MGR	4-9-76

TITLE FUNCTIONAL SCHEMATIC POWER CONDITIONER

TASK NO. 03025 SHEET OF 1 — 3

DWG NO. 34-028 R02008

BRUNING 44-231 2453B

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
FOR PREVIOUS REVISION SEE R00 MICROFILM IN FILE				
JRB		03025B	3-19-76	R01
AREA G2, R118 WAS NOT SPECIFIED AS 1%; AREAS E3, D5, D8 DIODES SHOWN DOTTED WERE NOT SPEC'D, ADDED NOTE 1.				
JRB		03025-10	3-29-76	R02

T301 P/O 30-051
F303 3A
0302 23-023
D118 23-025
BATTERY STAND-BY 3L1
R111 3.3K
D104 23-034
R110
Q104(HS) 20-006
(HS) 20-006
R108 0.1, 5W WW
R112 390
R120 0.2 5W WW
R123 47K
R122 15K
R121 1K 1%
R118 10K 1%
R119 10
Q101
Q106 20-023
Q111 20-023
Q110 20-023
Q107 20-023
P12/2A 12B-2-130-2 22B-2-230-2
R107 6.99K 1%
C102 150 16V
C104 150 16V
C106 150 16V
C138 4800 50V
SEE NOTE 1
D121 23-034
Q109 20-013
R101 10K
Q108 20-038
D103 23-041F02 6.2V 5%
R116 20K 1%
C112 2.2 20V
R117 200K
R115 10K 1%
R114 23.7K 1%
R113 4.99K 1%
C101 150 16V
C103 150 16V
C105 150 16V
P12 GND 1C6
P12 GND 1E4
P12 GND
P5 GND J8
115V 230V
78301
B 1A2
A 1A1
J301
P301
8301
8302
D 1A2
C 1A2
P1 J1
R188 68 2W
R187 68 2W
SEE NOTE 1
C3 141-2
5 VAC/50 MA
C1 240-2
CHARGER INPUT 3A1
P15 BIAS
Q102 20-006
(HS)
R128 2 1W WW
R127 390
D106 23-046
C113 1000 75V
R129 10K 1%
R131 4.99K 1%
R132 10K
R130 10K 1%
C114 0.1 30V
C115 100 50V
NC 09
V_{CC} V_Z
V_4 COR. CUR LIM. SENSE
V_{OUT}
INV IN
NC 01
NC 08
NC 14
R101 19-094
V_{REF}
NON INV IN
COMP
V_-
CHARGER REF 3A4
P5 GND R5
CHARGER INPUT GND 3A5

CHASSIS ASSY P/O 11-186

HI VOLTAGE BOARD P/O 35-615

NOTES:
1. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

SCALE— ~

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	11-10-75
	CHK	
	ENGR	

TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

TASK NO. 03025
DWG NO. 34-028R02008
SHEET 2 OF 3

BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
ENCLOSED 11-186 AREA IN DOTTED LINES				
JKB		03025B	3-31-76	R01

2J6 CHARGER INPUT

2F7 CHARGER REF

2J9 CHARGER INPUT GND

R403 1W 3% WW

R402 1K

C401 0.1 100V

R401 15K

R404 10K

R405 10

Q403 20-006 (HS)

R406 390

Q404 20-023

Q401 20-023

Q402 20-023

Q405 20-023

D401 23-025

R407 12.7K 1%

R408 100K

C402 0.1 30V

Q406 20-038

R415 10K

R411 390K

R413 100

Q407 20-013

R410 100K

Q408 20-013

R409 100K

R412 100K

R414 33K

R416 1950 1%

BATTERY BOARD 35-614

1K6 CHARGER ON/OFF

HI VOLTAGE BOARD P/O 35-615

BATTERY STAND-BY → 2R1

J3

138-2 / 238-2 → TO BACK PANEL EXT BATT (+)

BAT+

18V

139-2 / 239-2 → TO BACK PANEL EXT BATT (-)

BAT-

J5

P/O 5301

J4

CHASSIS ASSY P/O 11-186

BRUNING 44-231 24538

SCALE — ~

TOLERANCE UNLESS OTHERWISE SPECIFIED: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°

NAME	TITLE	DATE
B. GRAY	DRAFT	11-8-75
	CHK	
	ENGR	

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TITLE FUNCTIONAL SCHEMATIC POWER CONDITIONER

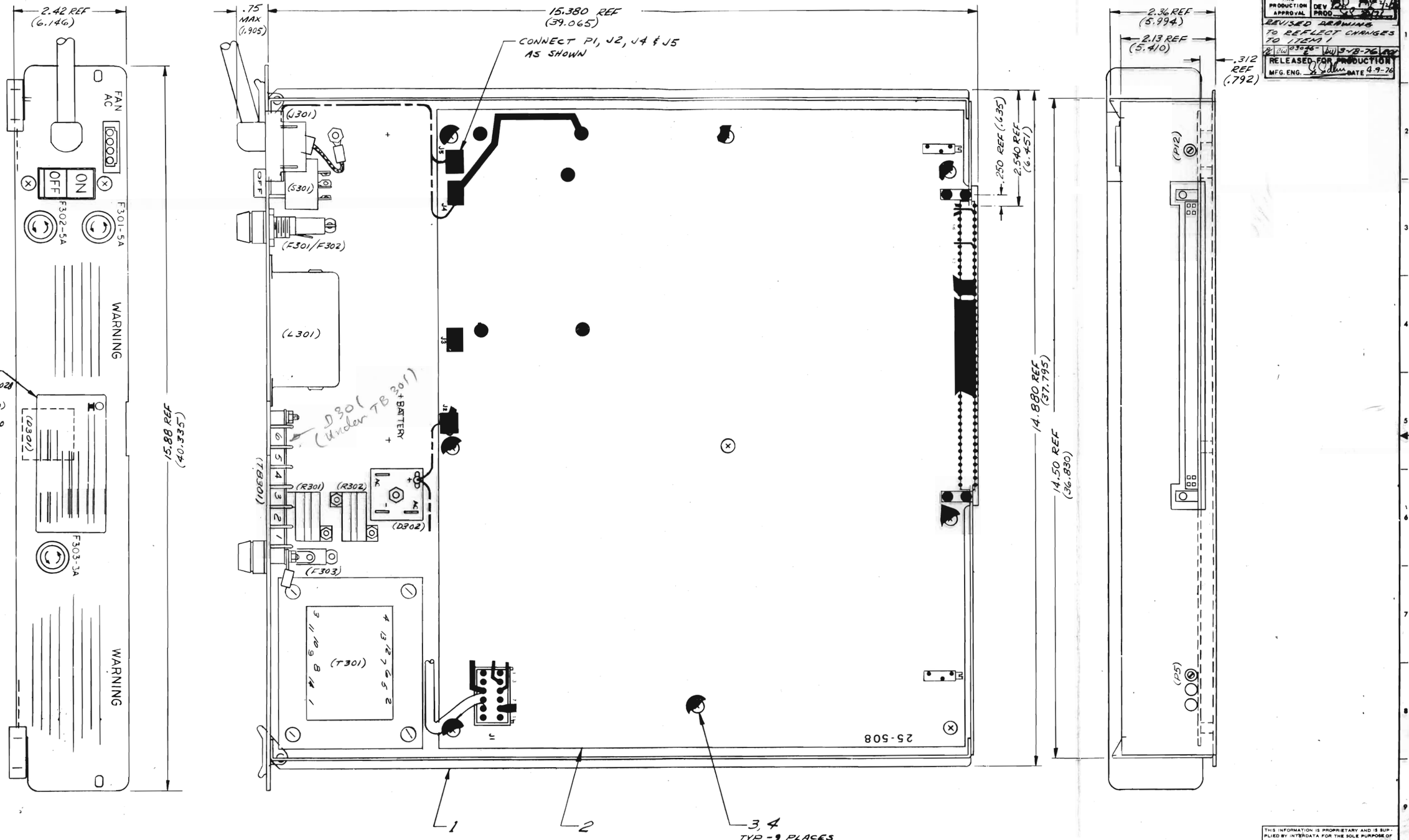
TASK NO. 03025 SHEET OF 3 — 3

DWG NO. 34-028 R01 008

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

PRE PRODUCTION APPROVAL	DEV PROD	
REVISED DRAWING TO REFLECT CHANGES TO ITEM 1		
RELEASED FOR PRODUCTION	MFG. ENG.	DATE 4-9-76



NOTE: DESIGNATIONS IN PARENTHESES ARE FOR REFERENCE ONLY; DIMENSIONS IN PARENTHESES INDICATE METRIC EQUIVALENT IN CM.

SCALE – 1-1	NAME	TITLE	DATE
TOLERANCE XXX ± .001, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	J.F. FLEMING	DRAFT	1-26-76
	H. MATTER	CHK	4-9-76
	G. WELLY/L1010	ENGR	4-9-76
	R.A. BARKER	Q.C.	4-5-76
	P. ABITANTE	MGR	4-9-76

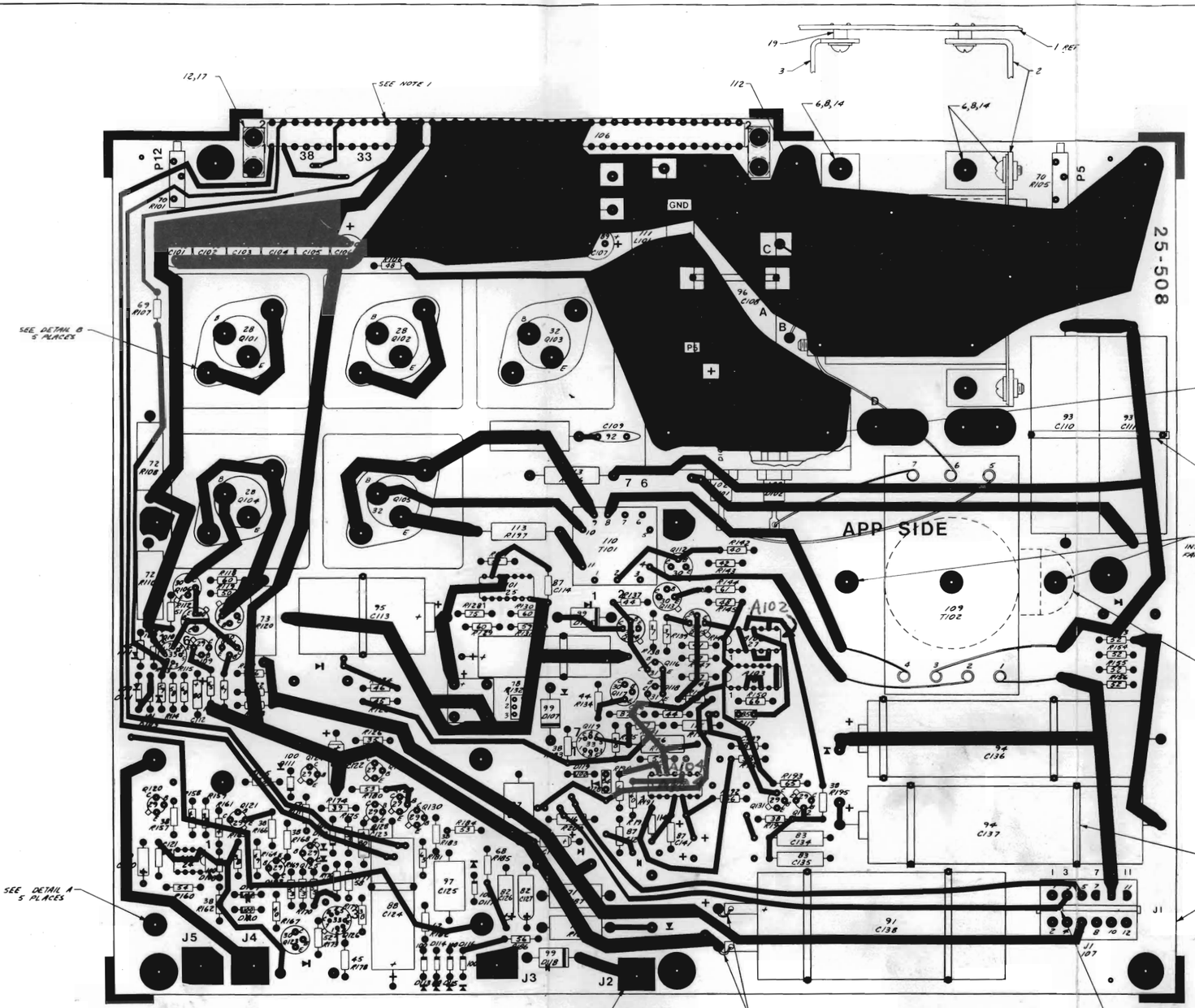
TITLE ASSEMBLY, SEMI-MEMORY POWER CONDITIONER

TASK NO. 08046 | SHEET OF 1 — 1

DWG NO. 34-028 R01 D03

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

BRUNING 44-231 24538


APP SIDE
25-508
A102
GND
SEE DETAIL B 5 PLACES
SEE DETAIL A 5 PLACES
SEE NOTE 1
12,17
112
6,8,14
19
3
1 REF
2
P12
P5
P3
J5
J4
J3
J2
J1
16,105
23
4
21
6,15
19 INSTALL FROM FAR SIDE
SEE DETAIL C FOR OPTIONAL MOUNTING
NOTE ORIENTATION OF CONNECTOR
1
J1 J07
1 3 7 11
2 4 8 10 12
T101
T102
L101
L102
C109
C110
C111
C136
C137
C138
Q101
Q102
Q103
Q104
R101
R105
R108
R197
R134
R135
R136
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D140

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

PRE PRODUCTION APPROVAL	DEV	DATE

REVISED SHEETS 1, 2, & 3 FOR PREVIOUS REVISION SEE ROO MICROFILM IN FILE, AREA K9, 35-614 WAS R00 & 35-615 WAS R02

JRB	03025B	3-19-76	R01

REVISED SHEETS 1 & 2 AREA K9, 35-615 WAS R04 AREAS F1, B7 DIODES SHOWN DOTTED WERE NOT SPEC'D, ADDED NOTE 3. AREA D5, C122 WAS 4.7/50V; AREA B5, C140 WAS 0.1/30V & WAS CONNECTED TO R140; AREA A6, ADDED R199; AREA F4, ADDED R200 & CR2; AREA J6, CHARGER ON/OFF WAS WAS CONNECTED TO D103 CATH.

JRB	03025M	3-30-76	R02

RELEASED FOR PRODUCTION
ENG [illegible] DATE 4/9/76

P/O 5301 F301 5A 24-069 L301 F302 5A P/O 5301 — 2B3 A, 2A3 B, 2B6 C, 2A6 D — P/O 11-186

D301 23-023 — P301 1.0 25W — P1 — J1 — R302 1.0 25W

SEE NOTE 3 — C136 475 200V — C137 475 200V — R156 100K — R155 100K — R154 100K — R153 100K — C110 15 200V — C111 15 200V

30-048 T102 — D101 23-042 — D102 23-042 — L102 40uH 30-023 — L101 30-050 3uH — C107 330 6.3V — C108 16500 6V — PS+L 100-2-113-2 / 200-2-212-2 — E103 5.0 10W 2(5Ω)in Para — PSGND/LGND 114-2-127-2 / 213-2-227-2

R104 21-075 .006 WHT WHT — YEL YEL — C B — A

T101 30-049 — C109 540 PF 1000V — R196 .12,5W — R197 .12,5W — E104 450 N.I. 1uH MAX 5W WW — 20-030 Q103 — 20-030 Q105

P15 BIAS — P/O 11-186

A102 19-192 CLK2 — A102 19-192 CLK1 — A103 19-191 — R150 17.2K 1% — C117 330PF 2% — R195 10K

Q115 20-023 — Q113 — Q112 20-023 — R145 2K — R144 100 1% — R143 3.3K — R134 33 — R138 4.7K — R139 4.7K — R148 4.7K — R147 4.7K — Q117 — Q118 20-027 — Q114 — Q116 20-027 — R146 22 — R137 33 — D107 23-025 — D105 23-025 — E142 6.8K

D134 — D136 — NO DIODES

P15 BIAS — R194 10K — C135 .0039 — C134 .0039 — R193 5.1K — Q132 20-013 — Q131 20-013 — 2R4 — P12 GND — C142 15 25V — R200 100 1/2W

D119 23-034 — R135 10K — R133 10K — R136 1% 1K,1W — Q119 20-038 — R141 13.3 1% — R199 1 1W — R140 33 — C116 0.1 30V

P15 BIAS — C140 0.47 150V 140-2 — C4 — P12 GND 2R4 — R165 1.5K — R124 160K — R125 15K — Q124 20-013 — D111 23-034 — Q127 20-013 — R126 100 — C122 15 25V — E184 68K — R183 10K — Q130 20-013 — R180 68K — Q129 20-013 — R149 6.8K — R174 47K — Q128 20-013 — R171 100K — C123 2.2 20V — R131 6.8K — C128 150 PF — R190 5.1K — C129 0.1 30V

U104 19-094 — Vcc V+ CUR LIM SENSE INV IN — V2 — VOUT — VREF NON INV IN — COMP — NC NC NC

R198 68 — C139 0.1,30V — R151 4.99K 1% — E152 20K 1% — C141 0.1 30V — R105 10K — R192 1K 1%

CHARGER ON/OFF → 3E7

P15 BIAS — R159 10K — P15 BIAS — R106 2K — PFDTO (POWER FAIL) 135-2

U105 TRIGGER 19-085 — Vcc RESET OUTPUT — DISCHARGE — THRESHOLD — CONT. VOL. GND — R160 820K — R161 47 — D108 23-034 — C120 2.2 20V — C121 0.1 30V — R163 10K — Q121 20-013 — R162 10K — D109 23-034 — D110 23-034 — R158 3K — Q120 20-013 — R157 10K

P/O 30-051 — T301 — P1 — J1 — D113 23-034 — D114 23-034 — D115 23-034 — D116 23-034 — D117 23-034 — SEE NOTE 3 — P/O 11-186

R186 1K 1% — R182 357K 1% — R178 15K — R173 100K — R179 10K — Q126 20-038 — R176 2K 1% — R175 68K — R172 20K 1% — Q125 20-013 — D112 23-043 F02 6.2V, 1% — Q123 20-023 — R167 6.8K — R170 68K — R169 68K — R168 10K — R166 10K — Q122 20-013 — R164 3K

C124 100 50V — C126 4.7 50V — C127 4.7 50V — R185 681 1% — C125 0.47 150V — R181 150K 1% — R177 23.7K 1%

PWR FAIL GND 235-2

OB 09 13 12 — A103 19-191 — 10 NC — 11 NC

COMPONENT NUMBERING	
101-299	HI VOLTAGE BOARD
301-399	CHASSIS
401-499	BATTERY OPTION BD

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-614 R01	BATTERY OPTION
35-615 R06	HI VOLTAGE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET	1	2	3
REV LEVEL	2	2	1
INDEX SHT. NO.	1	2	3

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
: ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
: ALL CAPACITORS ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE PART OF 35-615.
3. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

BRUNING 44-231 24538

SCALE — NONE
TOLERANCE: XXX ±.010, XX ±.03, X ±.1, ANGLES ±1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	11-10-75
H. MATTER	CHK	4-9-76
P. LIONO	ENGR	4-9-76
J. JAMATS	SYS TEST	4-9-76
S. MESSINA	MGR	4-9-76

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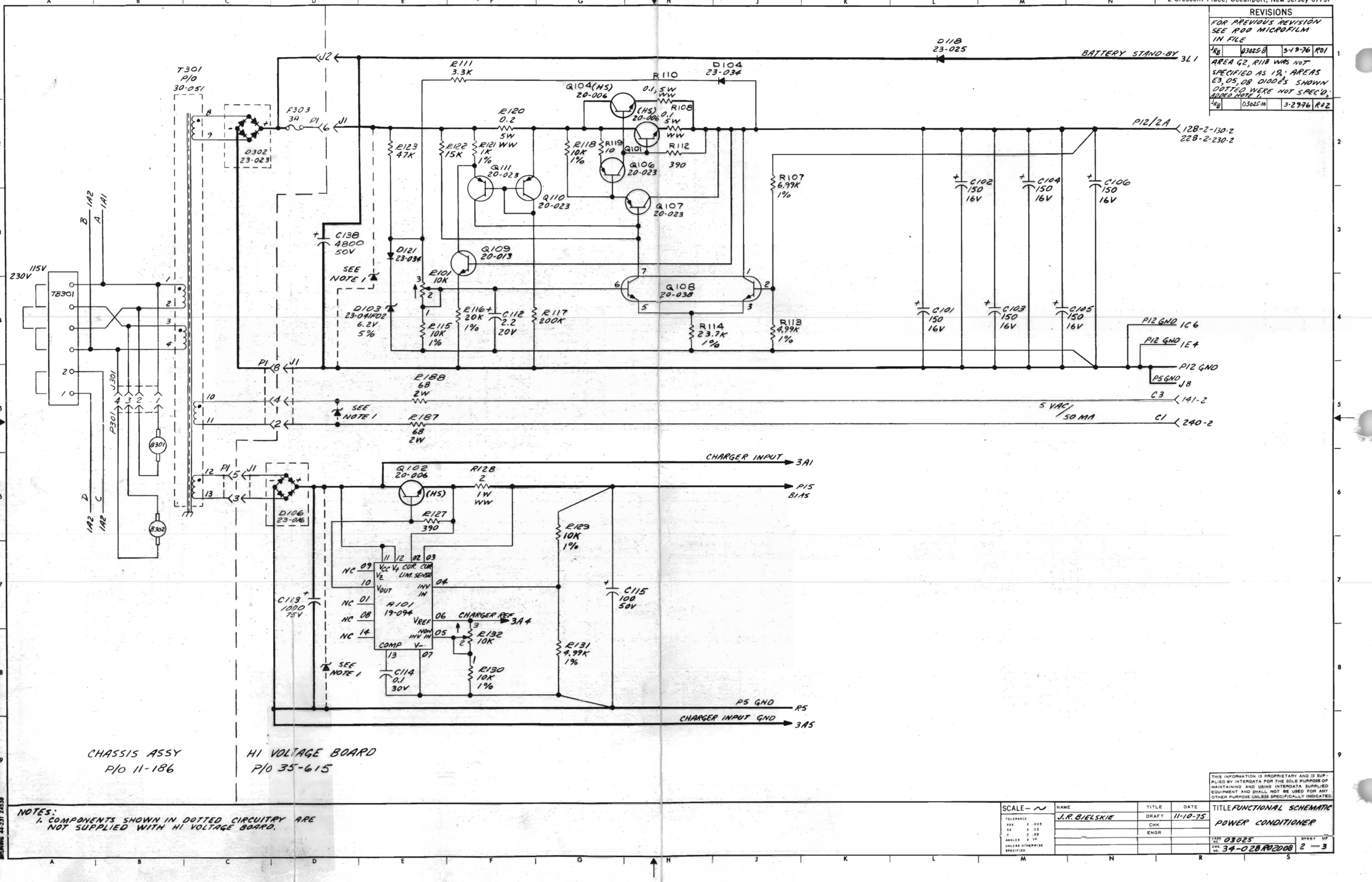
TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

TASK NO 03025 — SHEET OF 1 — 3
DWG NO 34-028 R02008

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
FOR PREVIOUS REVISION SEE R00 MICROFILM IN FILE
JRB 03025-B 3-19-76 R01
AREA G2, R118 WAS NOT SPECIFIED AS 1%; AREAS E3, D5, D8 DIODES SHOWN DOTTED WERE NOT SPEC'D; ADDED NOTE 1.
JRB 03025-10 3-29-76 R02



CHASSIS ASSY
P/O 11-186

HI VOLTAGE BOARD
P/O 35-615

NOTES:
1. COMPONENTS SHOWN IN DOTTED CIRCUITRY ARE NOT SUPPLIED WITH HI VOLTAGE BOARD.

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SCALE – ~	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1/2°, UNLESS OTHERWISE SPECIFIED	J.R. BIELSKIE	DRAFT	11-10-75
		CHK	
		ENGR	

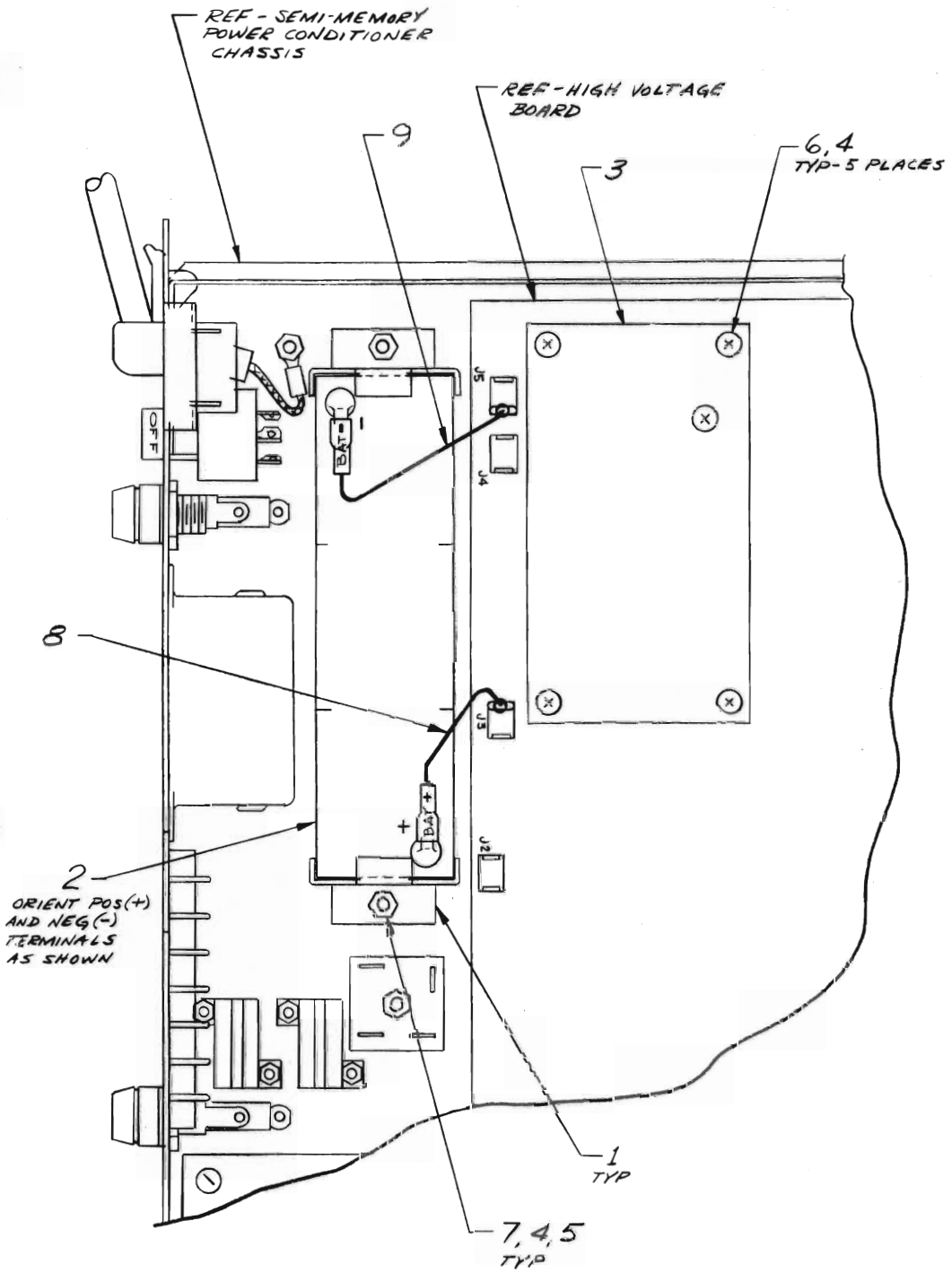
TITLE FUNCTIONAL SCHEMATIC
POWER CONDITIONER

TASK NO. 03025
DWG. NO. 34-028A02008
SHEET OF 2 — 3

BRUNING 44-231 24538

INTERDATA

REVISIONS		
PRE PRODUCTION APPROVAL	INIT.	DATE
DEV		
PROD		4/9/76
RELEASED FOR PRODUCTION		
MFG. ENG.		DATE 4-9-76



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SCALE - 1-1

TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J.F.FLEMING	DRAFT	1-29-76
H.MATTER	CHK	4-9-76
P.LIOIO/G.WELLY	ENGR	4-9-76
R.A.BARKER	QC	4-9-76
S.MESSINA	MGR	4-9-76

TITLE ASSEMBLY, BATTERY OPTION, SEMI-MEMORY POWER CONDITIONER

TASK NO. 03025

DWG NO. 02-423 C03

SHEET 1 — 1

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INTERDATA

REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DEV	DATE 1/11/76
		PROD	1-7-76

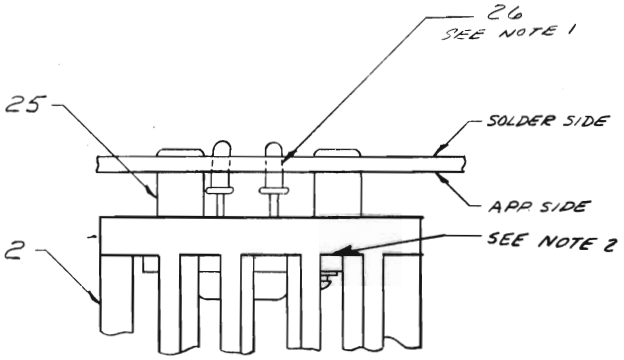
FOR PREVIOUS REV LEVEL SEE VOIDED R00 IN FILE

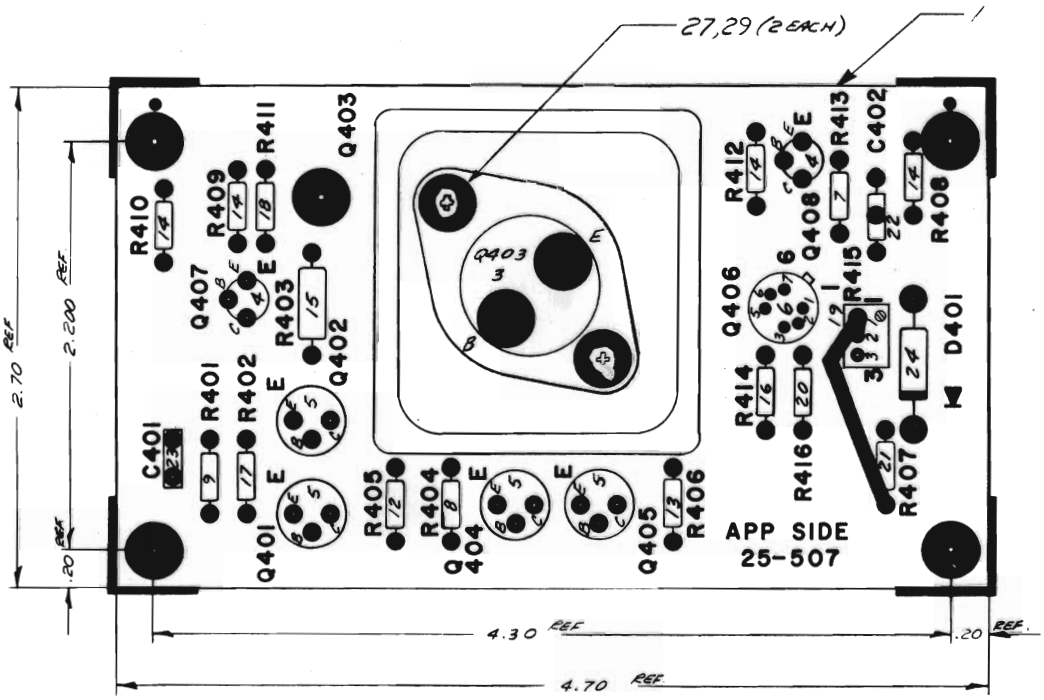
JRB	03025-8		3-8-76	R01

NOTE 1 READ "RECEPTACLE (ITEM 26) MUST BE FLUSH WITH S/S OF BOARD, INTERIOR PORTION TO BE FREE OF SOLDER." ADDED NOTE 2. AREA G7, ITEM 26 WAS FLUSH WITH BOARD.

JRB	03025-9		3-8-76	R02

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 4-9-76





ALL DIMENSIONS ARE IN INCHES.

NOTES:
1. BEFORE SOLDERING ADJUST SOCKET FOR MAXIMUM TRANSISTOR PIN ENGAGEMENT.
2. APPLY THERMAL COMPOUND BETWEEN HEAT SINK AND TRANSISTOR.

SCALE –

TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J. HELVATY	DRAFT	1-6-76
R. F. CERO	CHK	4-6-76
P. LIOIO	ENGR	4-6-76
ER BARKER	Q.C.	4-6-76
S. MESSINA	MGR.	4-6-76

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TITLE ASSEMBLY, PRT. CKT. BATTERY OPTION BOARD

TASK NO. 03025 | SHEET OF 1 — 1

DWG. NO. 35-614.R02C03

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