How an Electronic Brain Works

Part XI—Beginning the timing and control circuits

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IN the last three articles, we discussed series of pulses representing information traveling along lines (conductors) in an electronic brain (electronic digital computer). In Part VIII, we told how a series of pulses could be stored in a delay line until they were wanted somewhere else in the computer. In Part IX, we added two series of pulses or binary numbers, 0101 and 1011, in an adder (see Fig. 9 of Part IX). In Part X, we multiplied 1101 by 1011 in a multiplier. To do so we made use of (1) six machine cycles of eight pulse-times each, and (2) five different sets of control pulses.

The questions that arise now are:

1. Where do those series of control pulses for controlling the multiplier come from?

2. How can we obtain them and any other control pulses that we may need or want?

3. If we have two registers storing numbers, how can we take numbers out of those registers, put them into an adder or multiplier, and then store the results?

In this article, we begin the study of the answers to these questions; in other words the study of the timing and control of an electronic computer.

*Author: *Giant Brains*, John Wiley and Sons, 1949.

Timing pulse selector

In the operation of the multiplier one of the sets of control pulses which we used was the following:

Cycle	*Pulse Series*
1	0000 0000
2	0000 0001
3	0000 0001
4	0000 0001
5	0000 0001
6	0000 0000

The name of this particular set was the Multiplier Digit Timing Pulse, since it enabled us to select the desired successive digits of the multiplier at the time we wanted each one. Each of the eight-digit binary numbers in the pulse series is read from *right to left*, and the 1 indicates a pulse at the pulse-time corresponding to the position of the 1 and the 0 indicates no pulse at that pulse-time.

We obtain this series of pulses (and also any desired series of timing pulses) with a *Timing Pulse Selector*, an assembly of delay lines, flip-flops, and a single initial pulse. See Fig. 1, a diagram of a Timing Pulse Selector.

In the Timing Pulse Selector, the loop at the left side of Fig. 1 containing the seven-pulse delay line repeats a pulse pattern every eight pulses. If this loop were divided into eight 1-pulse delays, we could choose in every cycle a desired pulse in any one of the eight binary digit positions that we might be interested in. In our particular case, we are interested only in selecting the eight pulse-time in each cycle. So instead of installing seven 1-pulse-time delays (as would be more general), we have installed a single 7-pulse-time delay. A lead from the output of this delay gives us the pulse series for the Reset Timing Pulse for F-F1 and F-F2 in the multiplier of Part IX.

The six 8-pulse-time delay lines (marked 8P) in the loop across the top of the diagram of Fig. 1, enable us to choose the first pulse-time in any one of the six multiplier cycles that we may be interested in. At the start of each successive cycle No. 1, 7, 13, and so on, a pulse appears on line L1. At the start of each cycle No. 2, 8, 14, and so on, a pulse appears on line L2. At the start of each cycle No. 3, 9, 15, and so on, a pulse appears on line L3, and so on.

To construct the desired series of control pulses for the Multiplier Digit Timing Pulse we connect output lines L2, L3, L4, L5 from this loop (through crystal diodes to prevent back signals) to the outgoing line T3. The only times when a pulse is allowed out on L2, L3, L4, and L5 is at the start of cycles 2, 3, 4, and 5, so that we obtain just the timing pulses which we desire, the Multiplier Digit Timing Pulse. Similarly, we can obtain the Readout Digit Timing Pulse on line T4.

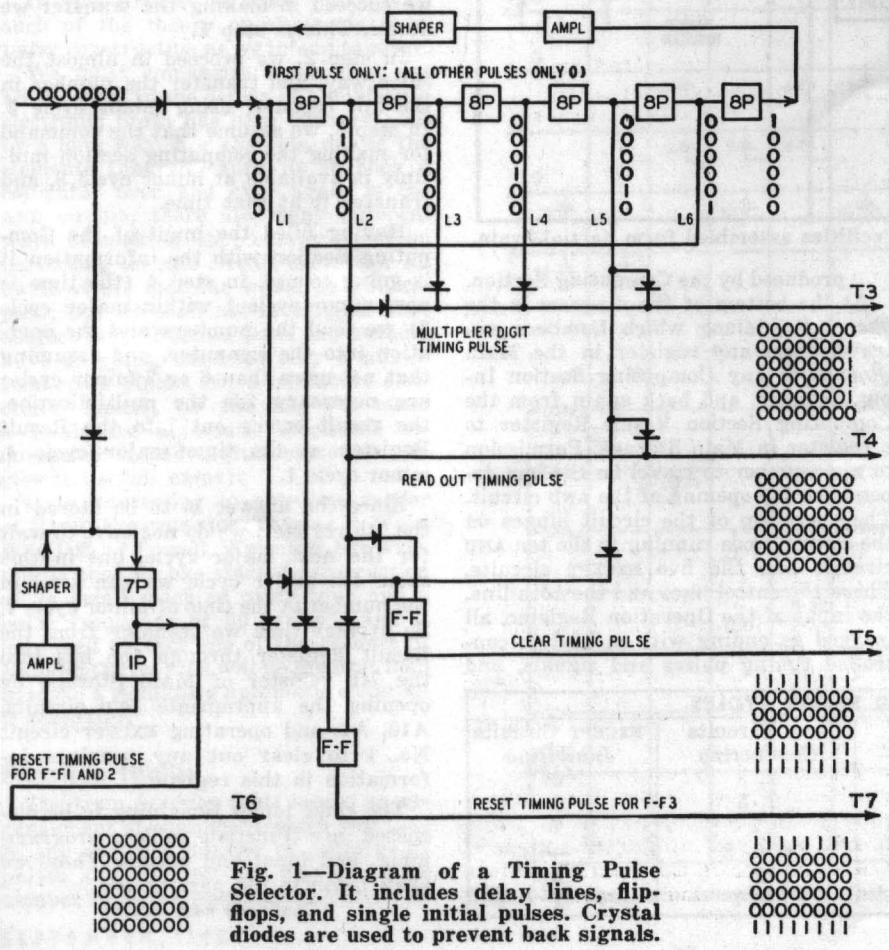

Fig. 1—Diagram of a Timing Pulse Selector. It includes delay lines, flip-flops, and single initial pulses. Crystal diodes are used to prevent back signals.

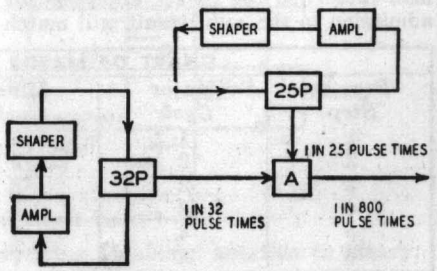

Fig. 2—Two circulating delay line loops.