sign of the number, whether *plus* or *minus.* For example, in decimal notation, with a five-column calculator, we would stop using the fifth column from the right for showing digits. Instead we would say: "If it holds 0, the other four digits are a positive number; if it holds 9, the other four digits are the complement of a negative number." For example, 09136 would mean +9136, but 99136 would mean –864. As a result, the machine would be unable to express any number greater than +9999 or less than –9999.

In binary notation we can do almost the same thing. We say, "If the extreme left-hand digit is 0, the remaining digits make a positive number. If that digit is 1, the remaining digits are the complement of a negative number."

We need to adjust our calculating circuits for adding two numbers which are both positive, or both negative, or one positive and one negative. We also need to adjust our calculator to ring an alarm in cases where the result is beyond the capacity of the calculator—that is, beyond +9999 or –9999 in terms of the example given above. A third consideration is the decimal point or, in binary notation, the "binal" point. In fact, there are a number of little adjustments needed. But it is probably better to neglect them at this stage, and go on to the next main process, multiplication.

Multiplication

In binary notation, the multiplication table becomes simply:

	0	1
0	0	0
1	0	1

or, in other words, 0 times 0 is 0, 0 times 1 is 0, and 1 times 1 is 1. Multiplication becomes either adding or not adding, and shifting.

For example, let us multiply two binary numbers, 1101 (one-one-oh-one: 8 plus 4 plus 1, or 13) and 1011 (one-oh-one-one: 8 plus 2 plus 1, or 11):

```
      1101
      1011
    ------
      1101
     1101
    0000
   1101
  --------
  10001111
```

The result is 10001111 (one-oh-oh-oh-one-one-one-one, or, one 128 plus no 64's plus no 32's plus no 16's plus one 8 plus one 4 plus one 2 plus one 1, or 143), which is of course what we would expect from ordinary multiplication of 13 and 11.

Fig. 2 shows circuits with energized relay contacts in red. Fig. 3 is the timing chart, showing how the circuits are to operate one after another, and over again, for successive digits of the multiplier. These circuits are preliminary, and not final.

We have assumed that the multiplicand (the number to be multiplied) is the four-digit binary number 1101, and the multiplier is the four-digit binary number 1011. They are stored in the A register (see part 1) and the B register (see part 2).

The general method we have used for obtaining their product is: choose multiples of the multiplicand, either 1101 or 0000, according to the successive digits of the multiplier 1011 taken from right to left 1, 1, 0, 1 (see parts 3, 4, 5); shift these multiples over to the left (see part 6) according to the successive positions of the multiplier digits (0, 1, 2, 3, or in relay language, 00, 01, 10, 11); with an addition circuit and storage register, add successively the shifted multiples (see parts 7, 8).

Proceeding now to examination of the parts of the circuit in detail, let us begin with a look at part 4. The select-multiple circuit (controlling relay C1 in part 4) operates on the multiplier 1011. This circuit yields at different times the successive digits 1, 1, 0, 1 that select the multiple of the multiplicand. How is this made to happen? In part 3, the K relays are energized in the pattern 00, 01, 10, 11, (0, 1, 2, 3 in binary) at successive times.

In part 5, the multiple of the multiplicand is selected. Its successive values are 1101; 1101; 0000; 1101. The contacts used are a contact of the C relay (see part 4) and four contacts of the A relays (see part 1); the multiple is recorded in the D relays.

In part 6, the selected multiple, recorded in the D relays, is shifted 0, 1, 2, or 3 spaces over, according to the position of the multiplier digit, recorded in the K relays (see part 3). The numbers produced by the E relays accordingly are:

0 0 0 1 1 0 1,
0 0 1 1 0 1 0,
0 0 0 0 0 0 0, and
1 1 0 1 0 0 0.

In Part 7, the addition circuit is indicated in block diagram, since it was treated in full in Part II, of this series. The storage register (part 8) is needed to transfer the result of the addition from the output of the addition circuit back into one of its inputs. Using these two circuits, the shifted multiples are added one after another as indicated in Table I.

The timing of the circuits is shown in the timing chart of Fig. 3. A good deal of useful information is summarized in this chart.

Successive time intervals, 1, 2, 3, 4, etc., are shown from left to right. The different terminals are shown from top to bottom, together with the relays they energize.

Opposite each terminal, the horizontal line begins at the time when the terminal is energized and stops when the terminal ceases to be energized. For example, the three terminals that energize the K relays T3.1, T3.2, and T3.3 are energized from time 6 to 9, from time 11 to time 14, and from time 16 to time 19, respectively. The following parts then complete the multiplication in four similar cycles.

Sections of different horizontal lines are connected by vertical lines showing X's and O's. These vertical lines with their marks summarize the functional relation of circuits. X marks the relays that are energized at a certain time, and O's mark the relay contacts through which these relays are energized. For example, at times 3, 8, 13, and 18, the D relays of circuit 5 are energized by current flowing from terminal T5 through contacts of the A relays and the C relay. For another example, at time 2, terminal T4 is energized, and the C relay is picked up, reading through B relay and K relay contacts. The K contacts at this time have not been energized; but this is correct, because the first multiplier digit has the position 0.

Table I — Multiplication Sequence

Name	Number	Relays
Partial sum	0000000	H to J
1st multiple	0001101	D
New partial sum	0001101	H to J
2nd multiple	0011010	D
New partial sum	0100111	H to J
3rd multiple	0000000	D
New partial sum	0100111	H to J
4th multiple	1101000	D
Final sum	10001111	H to J

It should be emphasized once more that there are many ways of condensing and improving these circuits. For example, parts 4, 5, and 6 can be combined, and the C and D relays eliminated. But the resulting circuit would have been harder to understand than the separate circuits here shown.

(*To be continued*)

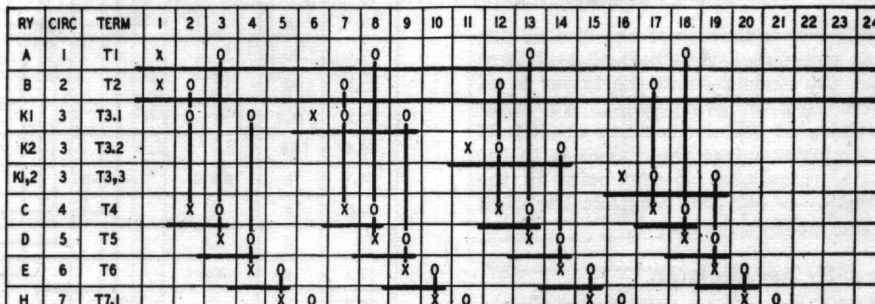

Fig. 3—Multiplying circuit timing chart which shows the sequence of operation.