

Hardware Interface

The interface between the host computer and the Audio Precision System One is a byte-wide bidirectional link with multiplexed address and data information. This allows interfacing with any computer which has two available I/O ports. It consists of eight data/address lines, four host driven control lines and three open collector lines driven from Audio Precision equipment. All information is sent and received over these lines under the control of the host computer. Direction of information flow and timing is controlled by the host.

The interface allows for "daisy chaining" of several pieces of equipment to the same host without additional interface cards. The drive capability of the lines is up to 24 receivers, depending on the cable lengths involved. The interface allows for up to 256 addresses, normally allocated in groups of 16 per functional device on the bus. This gives a maximum of 16 devices.

TABLE 1.4.1 lists the connector pin assignments. Brief functional descriptions are given below.

E0 - E7 are the bidirectional lines which handle address and data information. They have a controlled rise and fall time to minimize emitted RFI and to eliminate coupling into the control lines.

EA is the address strobe line. The host places the desired address on the bus and, after it is settled, pulses the address strobe line high. The address information is latched in each receiver on the falling edge of the strobe.

EW is the data write strobe line. The host places the desired data on the bus and, after it is settled, pulses this line high. The data is latched on the falling edge of the strobe.

ER is the data read strobe line. The host pulls this line high and the addressed device will place the data to be sent on the bus. The host then inputs the data and pulls the data read strobe low again.

ERST forces a power-on reset. This places all devices on the bus into a known state and places generator outputs and analyzer inputs into safe disconnected states. The normal state of the line is low, a high will force reset. This line has been designed to force a reset if the interface cable is disconnected.

/ATT is an open collector line driven by the receiving devices. If the address currently latched into the receivers is used by any of the devices this line will be pulled low. This serves two purposes. First, the buffer on the System One interface card uses this line to know that it should be active. Secondly, the host computer

can tell if a card is present by writing its address and looking for the "/ATT" line to go low.

/EIRQ is an open collector line driven by the receiving devices. If any device wants to signal the host that a task is completed or that attention is requested, this line is pulsed low. The PCI card is designed to latch the low pulse or to be interrupted by the pulse.

PWR indicates the state of all devices on the interface. If any unit loses power, this line will be pulled low.

/AUX is a general purpose line reserved for future use.

TABLE 1.4.1
INTERFACE PIN ASSIGNMENTS

<u>NAME</u>	<u>INTERFACE PIN</u>	<u>DESCRIPTION</u>	<u>POLARITY</u>
GROUND	1	Ground	
E0	2	Data/Address Bit 0	
E1	3	Data/Address Bit 1	
E2	4	Data/Address Bit 2	
E3	5	Data/Address Bit 3	
E4	6	Data/Address Bit 4	
E5	7	Data/Address Bit 5	
E6	8	Data/Address Bit 6	
E7	9	Data/Address Bit 7	
ER	10	Read Strobe	Active high
EW	11	Write Strobe	Active high
EA	12	Address Strobe	Active high
/EIRQ	13	Interrupt Request	Active low
/ATT	14	Valid Address	Active low
/AUX	15	Auxiliary Signal	Active low
ERST	16	Reset Drive	Active high
PWR	17	Power Good	Active high
GROUND	18-25	Ground	

Software Interface

All I/O is performed through four locations in the computer. Data is read and written at the base address plus 3. The System One module port address is written to the base address plus 2. Reads from base address plus 2 access the status lines /AUX, PWR, /ATT, and a latched version of the interrupt line /EIRQ.

For DMA from the System One to the computer the interface will delay data by one byte. This is due to an inconsistency in the IBM PC of the I/O channel not ready protocol. If for example the DMA controller is set to transfer a block of 100 points, the first point will be the