PROBLEM SOLVER SYSTEMS, INC.
20834 LASSEN ST. • CHATSWORTH, CA 91311
CABLE-PROBSOLVE

MODEL RAM16 16K Static RAM INSTRUCTIONS

The RAM16 is an S100 compatible 16,384 x 8 static memory board. It features:

* 250 or 450 nanosecond versions.
* Addressable in 4K steps by easily accessible DIP switch.
* Memory protection in 1K increments defined by an easily accessible DIP switch. Protection may be from the bottom board address up or from the top down.
* Memory protection activated/deactivated by a large, easily accessed switch.
* May deactivate up to six 1K segments of the board to create "holes" for other devices. Accomplished with jumpers.
* Wait states selected by DIP switch.
* SOL Phantom line DIP Switch.
* 8 bank select lines provided for expansion into ½ million byte systems.
* All data, address, and control lines input buffered.
* Ignores I/O commands at board address.
* Assembled, tested, and burned-in at factory.
* 1.3 A typical current consumption.

INSTALLATION & OPERATION

Prior to installing the RAM16 into an S100 chassis, power

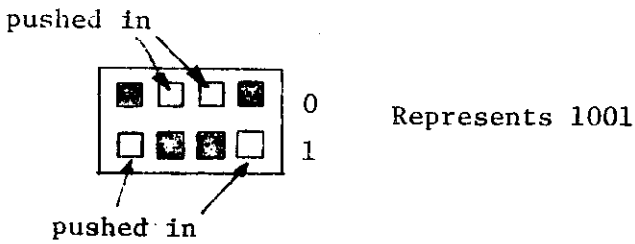
must be removed from the bus. Note that this precaution should be followed for any card on the S100 bus due to the close proximity of various power signals on the bus.

The only other operating instructions involve setting up the switches as described in the following paragraphs.

SWITCHES

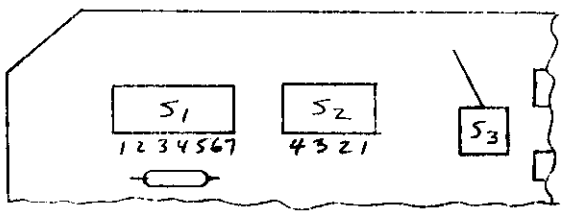
The RAM16 is supplied with two DIP Switches. When setting these switches, it is recommended that a pencil or other small pointed object be used to push the switch lever, thus ensuring that the switch lever is firmly snapped into position. A relatively small amount of positional offset could cause the switch to be off when it should be on.

In the following tables of switch settings, a "one" means that the bottom of the switch is pushed in toward the board (it also means that the top of the switch is protruding). An example:



NOTE: (Some switches are marked ON/OFF; ON corresponds to a logic 0 and OFF to a logic 1.)

The top left switch is labeled S1 and controls board address (4K steps), wait states (0, 1, or 2) and phantom line selection. S2 is to the right of S1 and selects the memory protection boundary address. S3 is a single large switch which activates the memory protect feature.



ADDRESSING

Address selection is accomplished using switch S1, positions 1 thru 4. The board address can be placed on any 4K boundary:

Addressing	Switch 1 1 2 3 4
0-3FFF	0 0 0 0
1000-4FFF	0 0 0 1
2000-5FFF	0 0 1 0
3000-6FFF	0 0 1 1
4000-7FFF	0 1 0 0
5000-8FFF	0 1 0 1
6000-9FFF	0 1 1 0
7000-AFFF	0 1 1 1
8000-BFFF	1 0 0 0
9000-CFFF	1 0 0 1
A000-DFFF	1 0 1 0
B000-EFFF	1 0 1 1
C000-FFFF	1 1 0 0
D000-0FFF	1 1 0 1
E000-1FFF	1 1 1 0
F000-2FFF	1 1 1 1

MEMORY PROTECT

Memory protection is controlled by switches 2 and 3. Switch 2 is a four position switch, which represents the protection boundary address relative to the board address. Switch 3 enables or disables the total protect function. When S3 is on, data will be protected up to and including the boundary 1K bank. Protection occurs in 1K steps:

Switch 2 Pos. 4 3 2 1	Addresses relative to Board Address: Protected	Unprotected	Amount Protected
0 0 0 0	0-3FF	400-3FFF	1K
0 0 0 1	0-7FF	800-3FFF	2K
0 0 1 0	0-BFF	C00-3FFF	3K
0 0 1 1	0-FFF	1000-3FFF	4K
0 1 0 0	0-13FF	1400-3FFF	5K
0 1 0 1	0-17FF	1800-3FFF	6K
0 1 1 0	0-1BFF	1C00-3FFF	7K
0 1 1 1	0-1FFF	2000-3FFF	8K
1 0 0 0	0-23FF	2400-3FFF	9K
1 0 0 1	0-27FF	2800-3FFF	10K
1 0 1 0	0-2BFF	2C00-3FFF	11K
1 0 1 1	0-2FFF	3000-3FFF	12K
1 1 0 0	0-33FF	3400-3FFF	13K
1 1 0 1	0-37FF	3800-3FFF	14K
1 1 1 0	0-3BFF	3C00-3FFF	15K
1 1 1 1	0-3FFF	none	16K

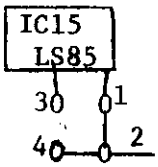
NOTE: An easy way to keep track of the protect address is to observe that switch 2, position 4, corresponds to A13, position 3 to A12, position 2 to A11, position 1 to A10.

Furthermore, A13 and A12 are the LSB's of the MSB hex address digit and ALL and A10 are the MSB's of the 2nd MSB hex address digit. For example, if the switches are 1001, this corresponds to hex address 2400 (xx10 01xx xxxx xxxx). Since all addresses with MSB's $\leq$ 2400 plus board address will be protected:

* protected data=board address
  to board address + 27FF
* unprotected data=board address + 2800
  to board address + 3FFF

A table at the end of this instruction manual shows all combinations of board addresses and protection.

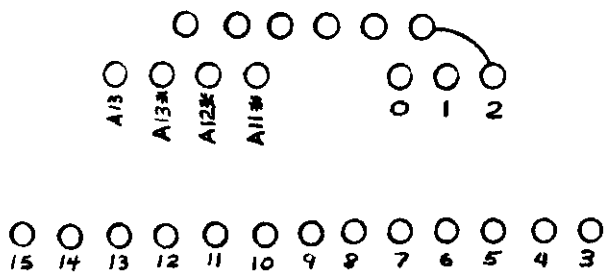
A jumper option allows for the protection of data from the boundary address to the end of the 16K board address (ie. protection from the top down):



Break 1-2 and jump 3-4 for top down memory protection

SEGMENT DISABLE

Provision is made for the installation of up to six jumpers between memory addressing logic and board disable inputs. This disables sections of the memory so that the RAM16 board stays off of the S100 bus during computer access of the disabled section. The six disable inputs may be connected to any of the 16 1K chip enables, or to address lines which allow for disabling 2K, 4K, or 8K segments. To disable a 1K segment, a jumper should be added from one of the pads labeled 0-15 to one of the 6 pads labeled segment disables. For example, to disable segment 2:



* *

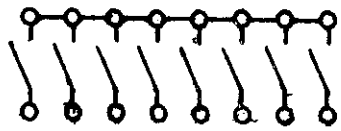
Note that on some early boards the segment disables are incorrectly labeled 1-16 instead of 0-15.

Four more pads are provided for jumping A11*, A12*, A13* or A13.

If one is not using all of the memory chips possible, then the ones to leave out are CS0 for segment 0, CS1 for segment 1, etc. as marked on the board. For example if one is disabling a segment at F800-FBFF, then a jumper should be added from CS14 to the disables; the 2 memory chips at CS14 could then be removed. A table is attached which shows the chip select signal corresponding to a given address. Note that the segment disable jumper does not change even if the board address is changed.

BANK SELECT

Provision is made for 8 bank select signals on S100 pins 14, 15, and 61-66. Either an 8 position DIP switch or jumpers may be used to define the active bank.



BANK 0 1 2 3 4 5 6 7

These lines directly define the active bank(s) by their DC state (rather than by pulses). These lines may be controlled directly from switches or from the forthcoming Problem Solver memory management feature.

WAIT CYCLES

In the event that your computer is capable of operation at a faster rate than the Problem Solver board you have chosen, provision is made to synchronize the memory to the computer using the PREADYline of the S100 bus. Switch S1 positions 5 and 6 select the wait state by being placed in the "1" state:

	Switch 1
Provision	5 6
0 wait states	x 0
1 wait states	0 1
2 wait states	1 1

SOL "PHANTOM"

The SOL system requires that the first block of memory be disabled for the first few machine cycles after power up to allow the monitor to initialize the system.

The RAM16 is disabled by means of the "PHANTOM" signal on pin 67 of the bus. This feature may be incorporated on the RAM16 by placing Switch 1, position 7 in the "0" state. It is disabled by placing the switch in the "1" state.

TESTING

Each RAM16 memory board undergoes a thorough testing program consisting of a 40 hour burn-in with power on followed by one-hour of a propretary "Blitz test" which operates the boards at their maximum rate, and fails them if they make one error.

WARRANTY

Problem Solver Systems, Inc. offers a 120-day warranty on all parts and materials. This warranty covers every conceivable failure except for misuse or abuse of the memory system. Determination of misuse or abuse is determined solely by Problem Solver Systems, Inc. To obtain warranty repair or replacement, you may return it to the place of purchase or directly to the manufacturer, along with proof of purchase. Your memory system will be returned to you promptly, postpaid.

OUT OF WARRANTY SERVICE

Problem Solver Systems, Inc. services everything sold promptly and at a reasonable cost. If a product requires service, return it postpaid and it will be test promptly.

You will then be advised of the repair cost either by phone (if you include your number) or by postcard. The minimum repair fee is $7.50. Repair and shipping requires one working day after approval.

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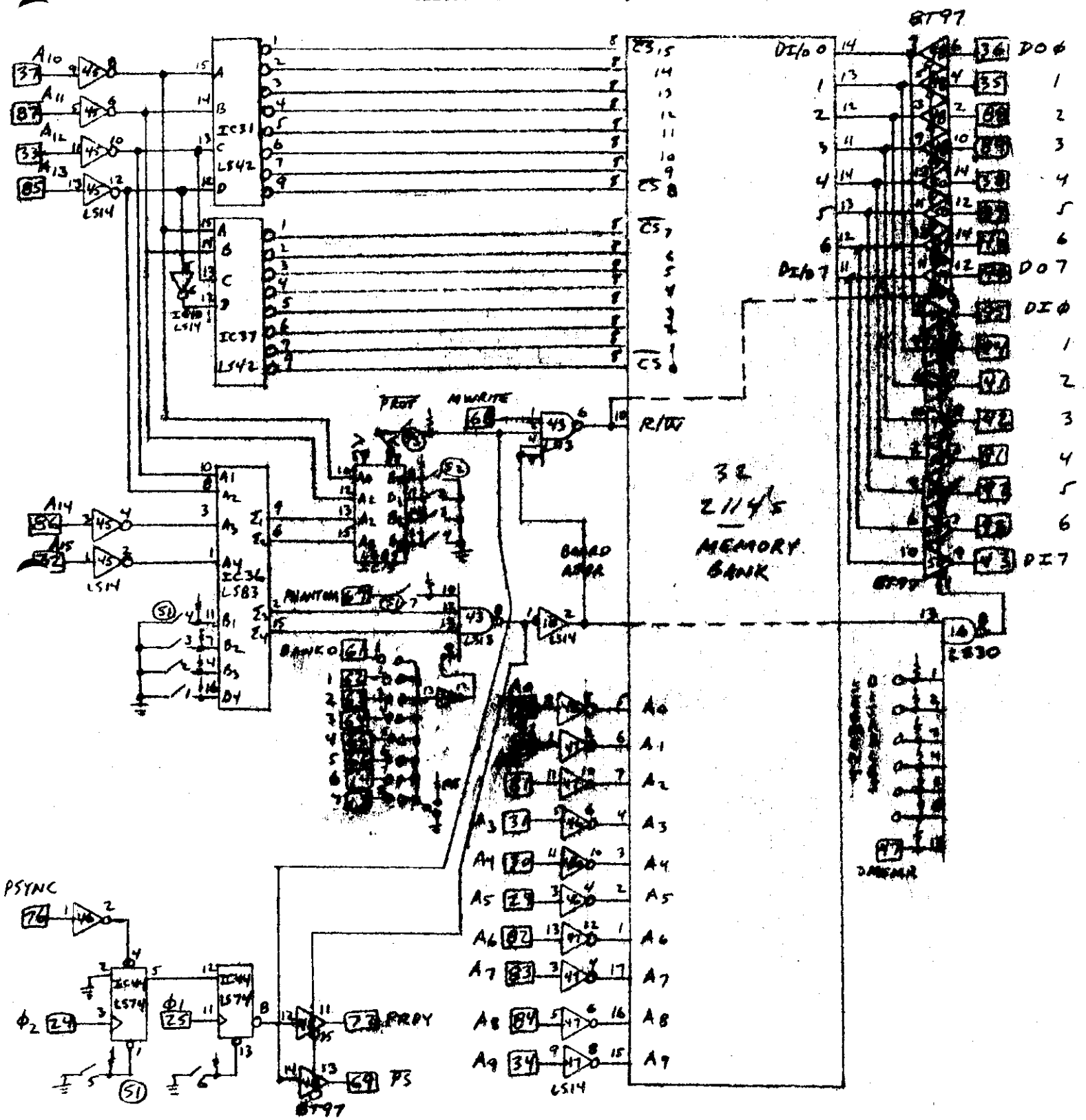
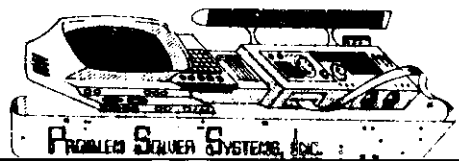
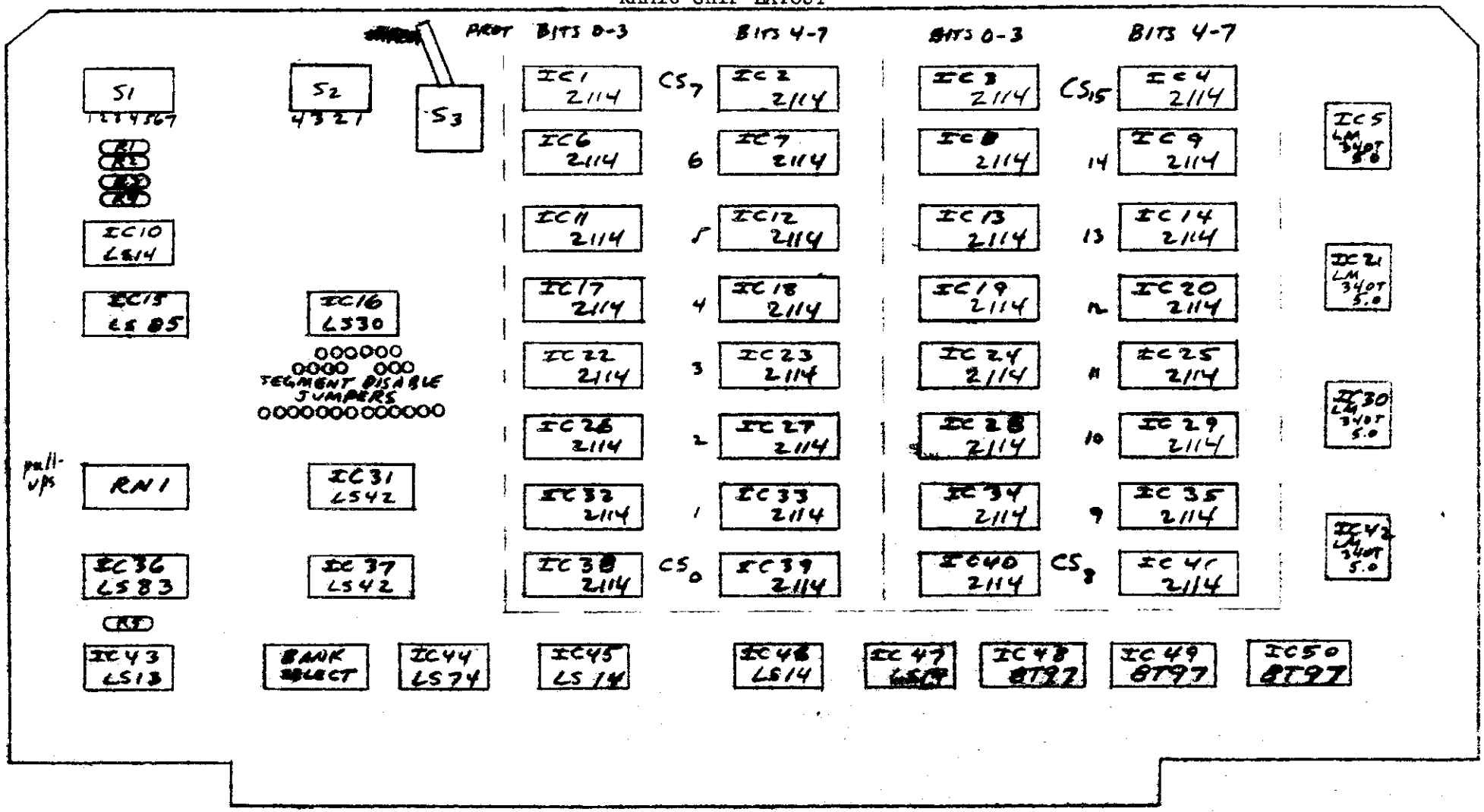
(213) 998-5100

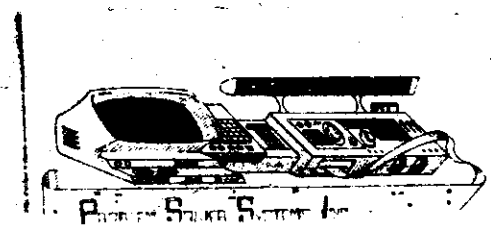
RAM16 16K x 8 SCHEMATIC





RAM16 CHIP LAYOUT





CHIP SELECT VS. ADDRE

Board Address

Chip	Addr. Lines															
elect	13-10	0000	1000	2000	3000	4000	5000	6000	7000	8000	9000	A000	B000	C000	D000	E000	F000
0	0000	0000	4000	4000	4000	4000	8000	8000	8000	8000	C000	C000	C000	C000	0000	0000	0000
1	0001	0400	4400	4400	4400	4400	8400	8400	8400	8400	C400	C400	C400	C400	4000	4000	4000
2	0010	0800	4800	4800	4800	4800	8800	8800	8800	8800	C800	C800	C800	C800	8000	8000	8000
3	0011	0C00	4C00	4C00	4C00	4C00	8C00	8C00	8C00	8C00	CC00	CC00	CC00	CC00	C000	C000	C000
4	0100	1000	1000	5000	5000	5000	5000	9000	9000	9000	9000	D000	D000	D000	D000	1000	1000
5	0101	1400	1400	5400	5400	5400	5400	9400	9400	9400	9400	D400	D400	D400	D400	1400	1400
6	0110	1800	1800	5800	5800	5800	5800	9800	9800	9800	9800	D800	D800	D800	D800	1800	1800
7	0111	IC00	IC00	5C00	5C00	5C00	5C00	9C00	9C00	9C00	9C00	DC00	DC00	DC00	DC00	IC00	IC00
8	1000	2000	2000	2000	6000	6000	6000	6000	A000	A000	A000	A000	E000	E000	E000	E000	2000
9	1001	2400	2400	2400	6400	6400	6400	6400	A400	A400	A400	A400	E400	E400	E400	E400	2400
10	1010	2800	2800	2800	6800	6800	6800	6800	A800	A800	A800	A800	E800	E800	E800	E800	2800
11	1011	2C00	2C00	2C00	6C00	6C00	6C00	6C00	AC00	AC00	AC00	AC00	EC00	EC00	EC00	EC00	2C00
12	1100	3000	3000	3000	3000	7000	7000	7000	7000	B000	B000	B000	B000	F000	F000	F000	F000
13	1101	3400	3400	3400	3400	7400	7400	7400	7400	B400	B400	B400	B400	F400	F400	F400	F400
14	1110	3800	3800	3800	3800	7800	7800	7800	7800	B800	B800	B800	B800	F800	F800	F800	F800
15	1111	3C00	3C00	3C00	3C00	7C00	7C00	7C00	7C00	BC00	BC00	BC00	BC00	FC00	FC00	FC00	FC00

Shows the chip select that will be activated for a given address. For example, if the board address is 1000 and the actual address is between 4000 and 43FF,